

Towards a Multi-Kiloton Pixelated Liquid Argon Time Projection Chamber

CPAD 2026, University of Washington

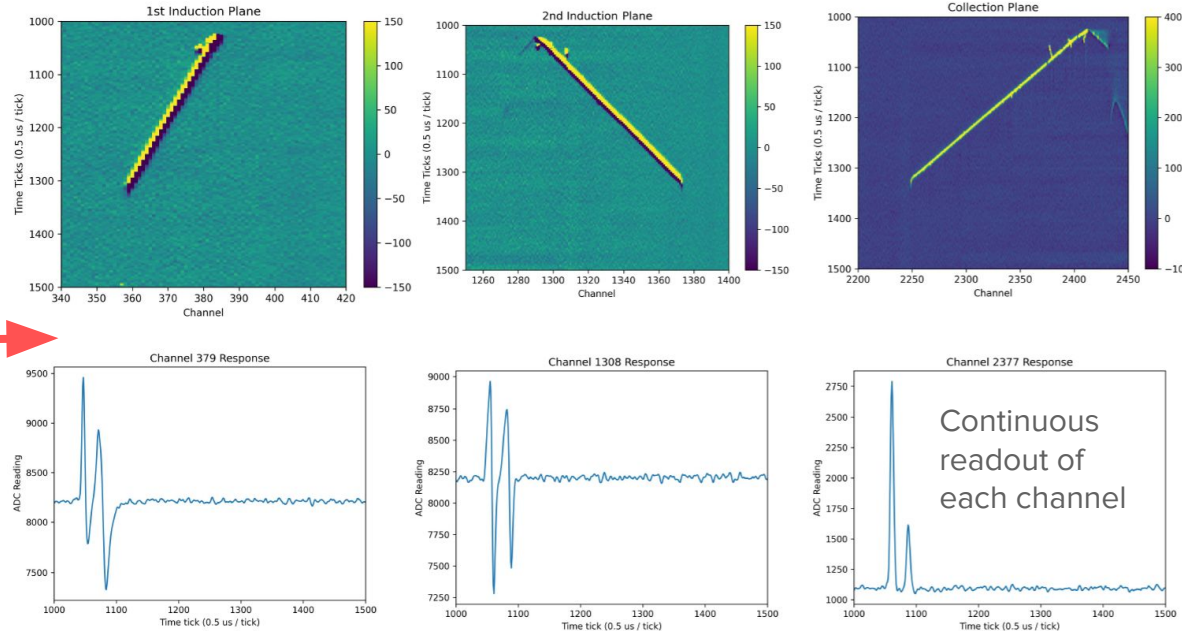
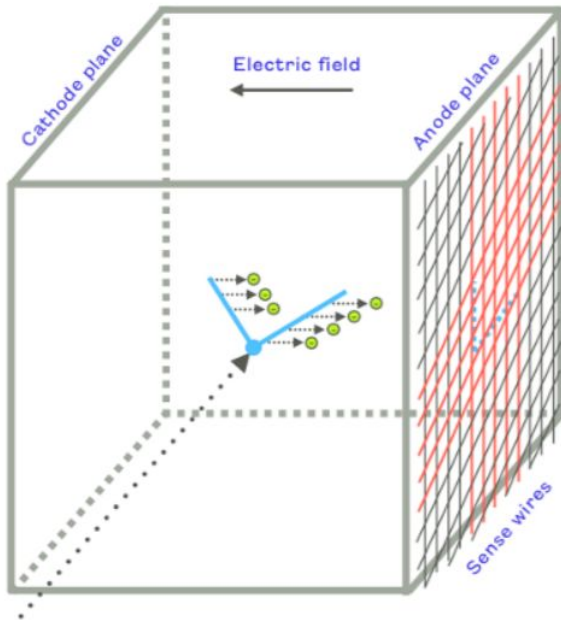
Roger Huang for the
DUNE Collaboration



Liquid Argon Time Projection Chambers

Traditional wire/strip-based LArTPCs combines 2D projections from 3 planes

- For cold electronics, typical noise requirements of **< 1000 e⁻ ENC** and power limits of **< 50 mW / channel**

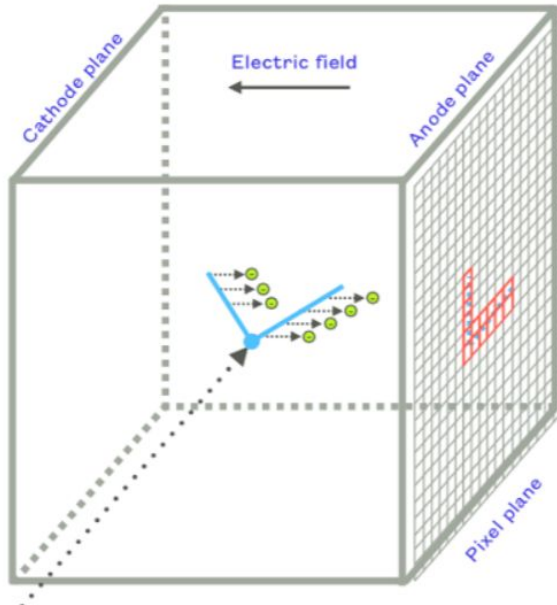


Liquid Argon Time Projection Chambers

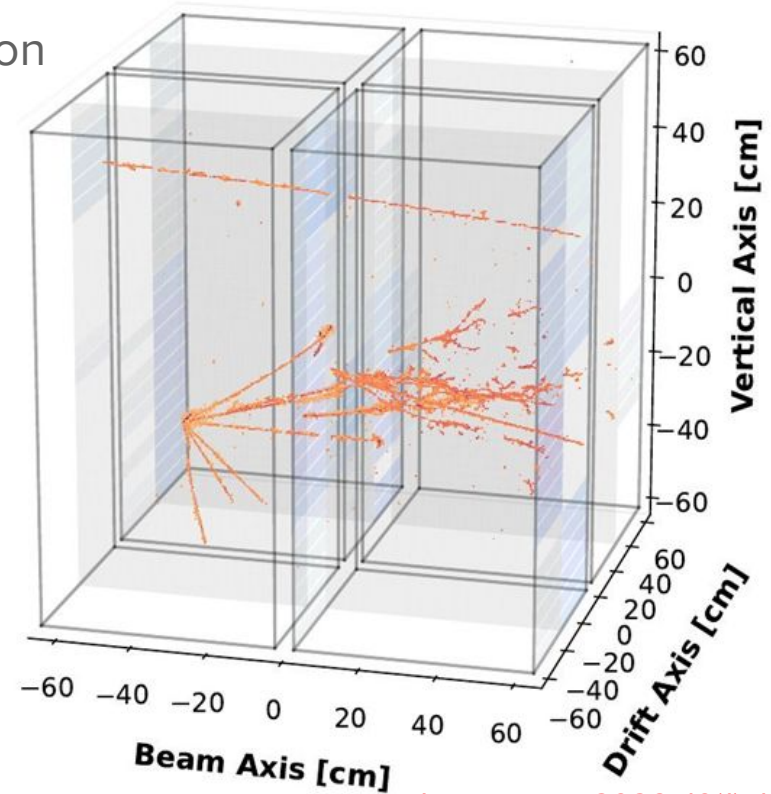
Pixel-based readout gives native 3D reconstruction

But the number of channels scales as N^2

- Power limit of **O(100s uW)** / channel



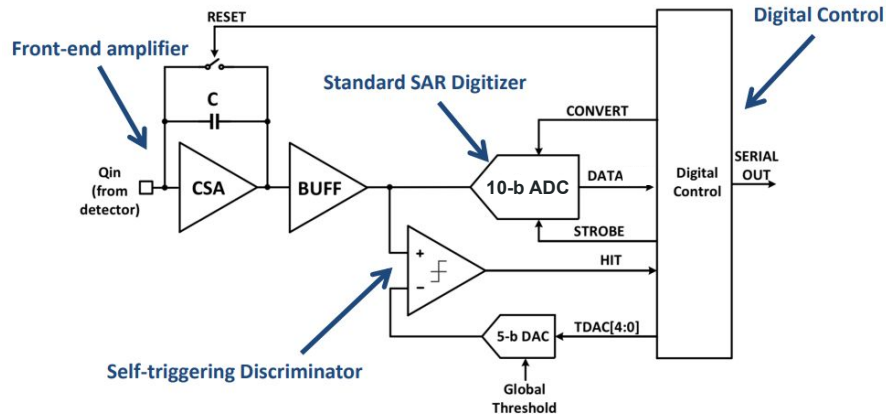
DUNE 2x2 Neutrino Data



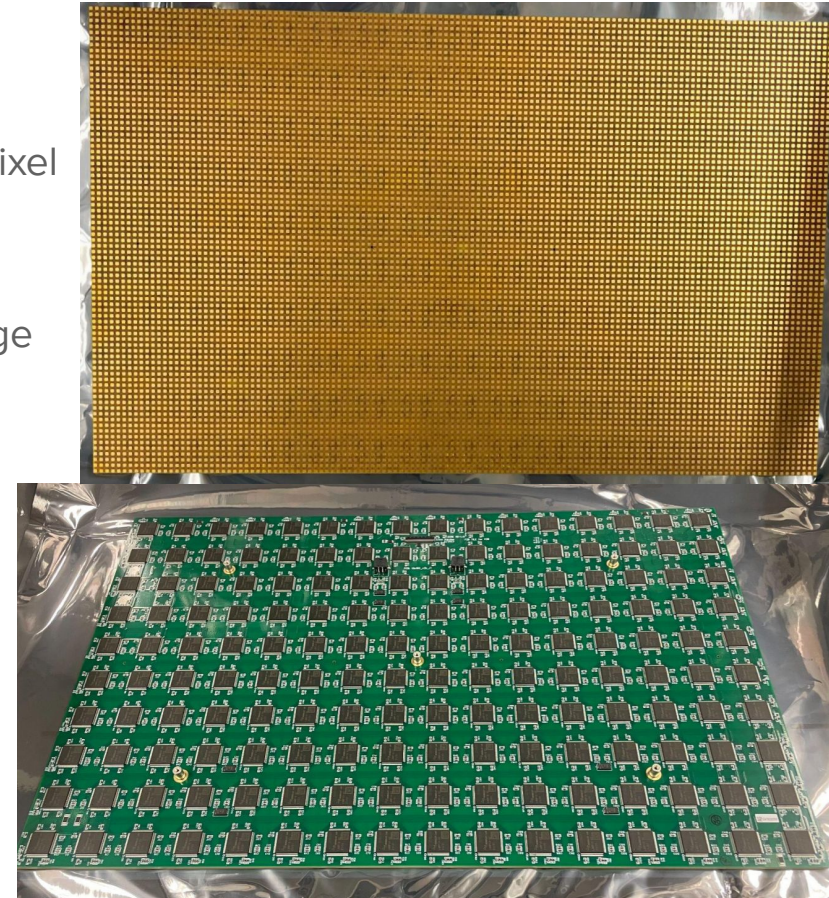
Charge Readout with LArPix

The **LArPix ASIC** exploits the intrinsic sparseness of LArTPC neutrino data to provide a scalable solution to pixel readout, using a **self-triggered** design:

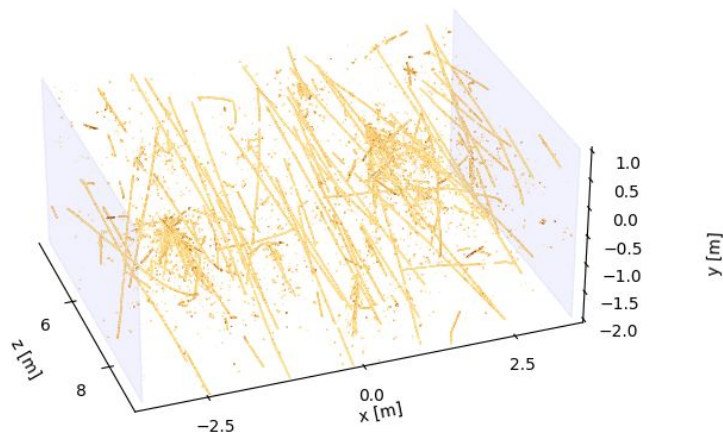
- Each pixel operated as an individual channel
- Each channel sends no output until collected charge passes threshold
 - $O(100 \text{ keV})$ trigger thresholds per pixel in LArPix



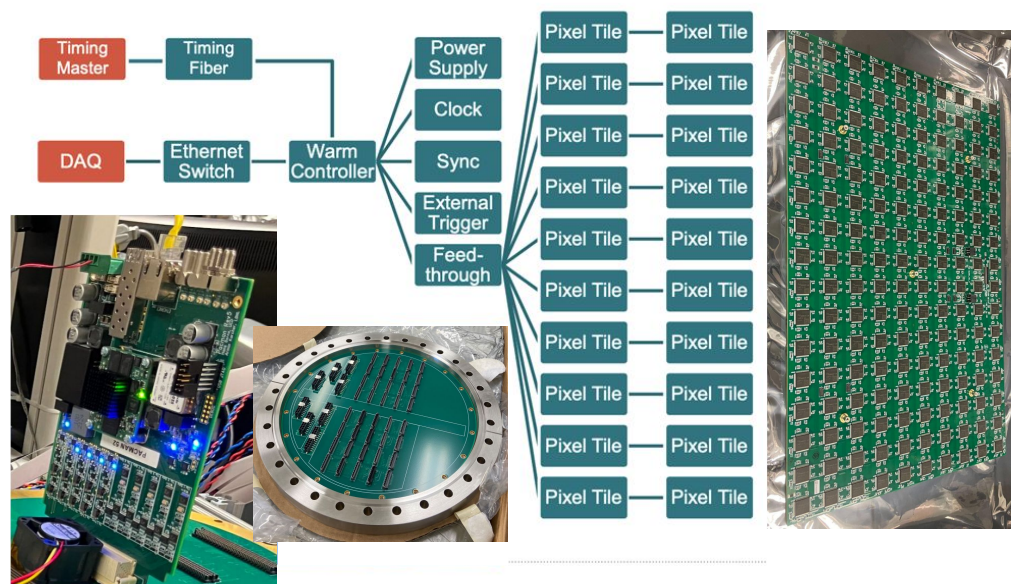
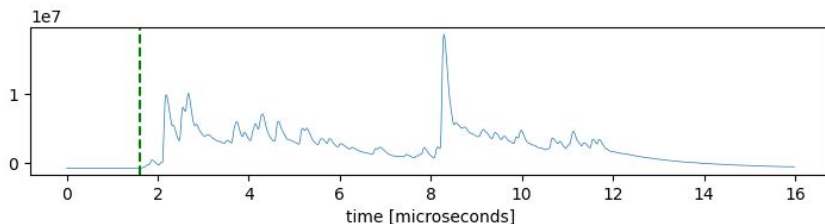
160 ASICs reading 10240
pixels in a 0.5 m x 0.3 m tile



LArPix in DUNE



DUNE Simulation



DUNE's liquid argon near detector (ND-LAr) employs pixelated readout with LArPix to handle the expected neutrino pileup

- O(100 tons) of LAr
- ~14M pixels read by ~224K ASICs

Pixelated Far Detector

The first two DUNE far detectors (FDs) are 17 kiloton LArTPCs using wire and strip based readout. The third and fourth FD designs are not yet finalized.

What could we gain by pixelating the far detector as well?

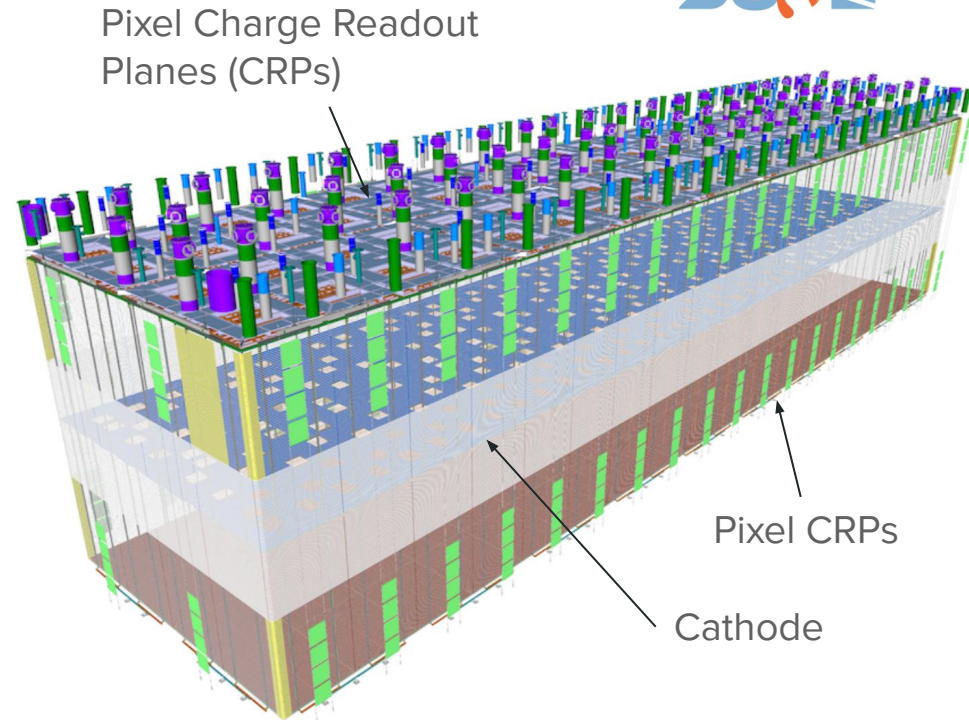
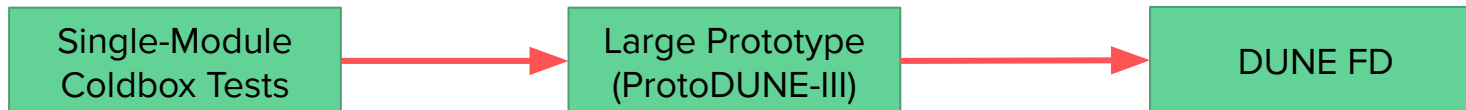
- **Native 3D reconstruction**, avoiding problems of ghost hits and ambiguities from combining 2D planes
- Improved ND to FD extrapolation by using the same detector technology, which can help **cancel detector systematics**
- Detection of unexpected low-energy physics and lightened load on DAQ with **self-triggering** capabilities and **zero-suppressed readout**

Pixelated Far Detector

What's needed to scale pixel readout to a DUNE FD (17 kiloton LArTPC)?

- New **mechanical structures** for the pixel tiles
- Compatibility with **longer power and data cables** (up to ~30 m)
- **Additional multiplexing** to reduce cable load

Follow FD prototyping plans:



In the case of 160 (top + bottom) pixel CRPs, **1.79M ASICs** reading **114M pixels**

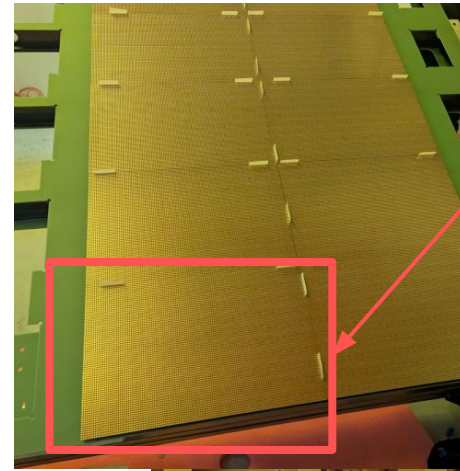
Pixel CRP Design

Re-use mechanical design of current DUNE FD CRP design, but cover with pixel tiles instead

For the first prototype, one full 3 m x 3 m CRP (2x CRUs) covered with 60 full-sized LArPix tiles

- 614.4k pixels at 3.72 mm pitch
- 40 LArPix-v2d tiles
- 20 LArPix-v3a tiles

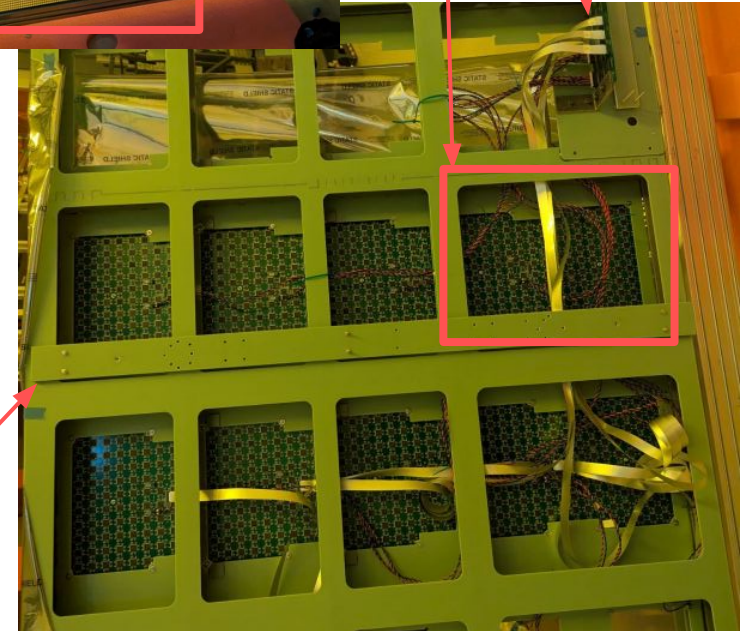
CRU Top Side



One LArPix Tile

Cable Patch Panel

CRU Bottom Side



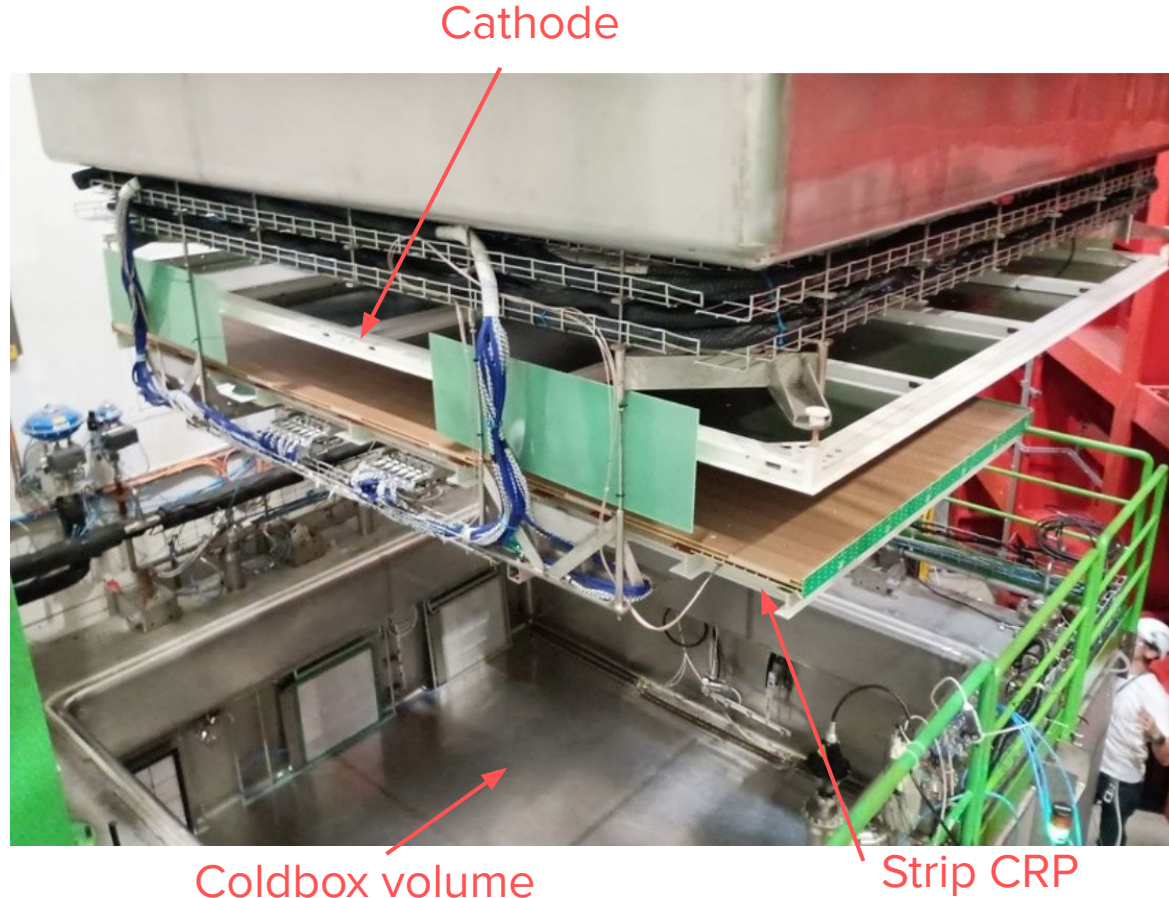
Supporting Composite Frame

CERN Coldbox Setup

Coldbox at CERN Neutrino Platform holds ~13 tons of LAr, designed to test 3m x 3m CRP modules. Fits a whole CRP + cathode

- Runs as a fully functional LArTPC with **~20 cm** drift

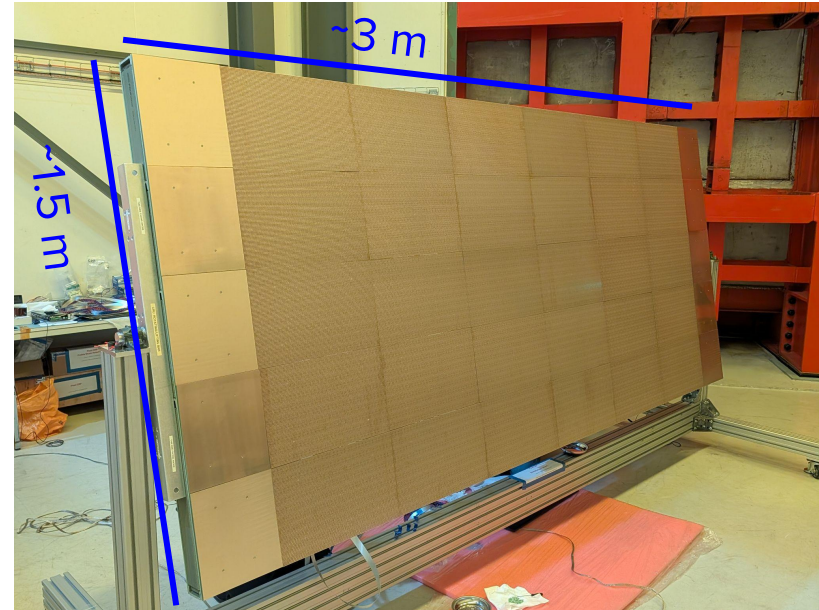
Allows for full test of system performance in a TPC environment



Pixel CRP Preparations for CERN Coldbox

Assembly of 60-tile LArPix CRP now complete at CERN

LAr coldbox test planned for end of the month



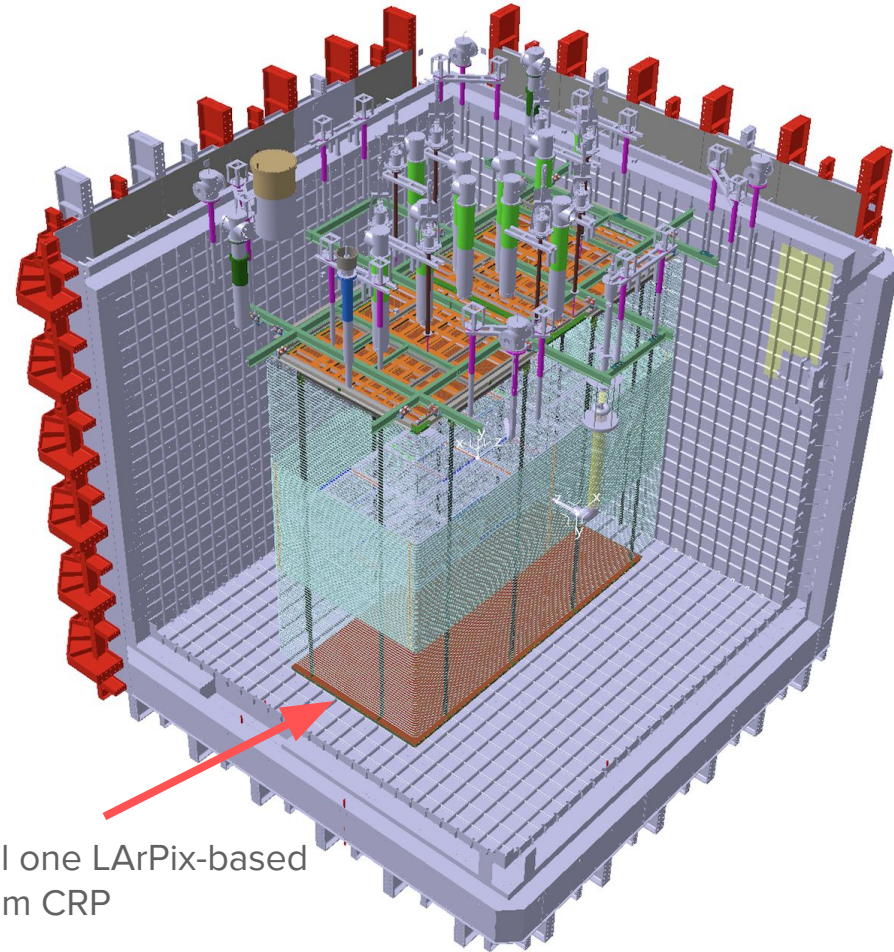
ProtoDUNE-III LArPix Module

The ProtoDUNE cryostats at CERN each hold ~800 tons of LAr, and are used for large-scale LArTPC prototypes

[ProtoDUNE-III proposal](#) targets 2028, including other potential technologies for DUNE FD upgrades

Would contain **one LArPix-based CRP** that other new components too:

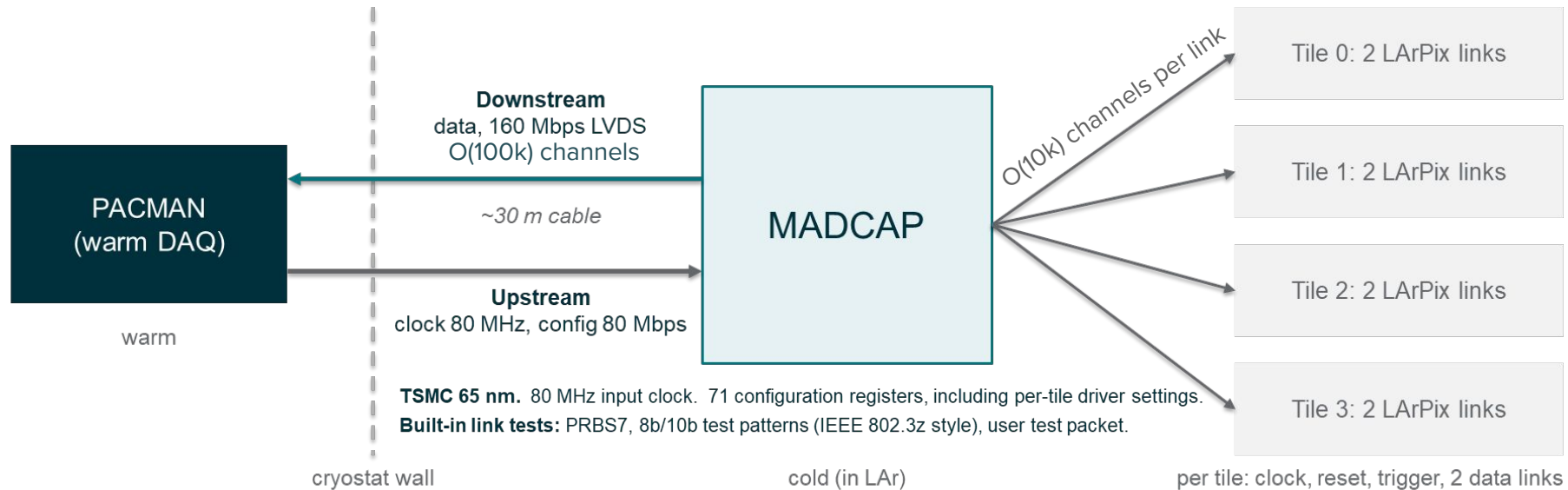
- Longer power and data cables
- New data concentrator ASIC:
MADCAP



Install one LArPix-based
bottom CRP

MADCAP: Multiplexer ASIC for Data and Clock Aggregation and Propagation

One cold ASIC carries clock, control, and data for 4 LArPix tiles over one LVDS link



8 : 1

LArPix links per MADCAP link

80 MHz input clock $\Rightarrow$ 10 MHz clock per tile
160 Mbps data link has headroom to handle sustained maximum 10 Mbps rates from every LArPix link

Inside MADCAP

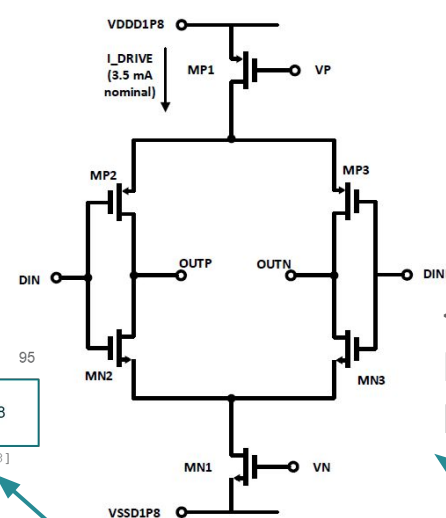
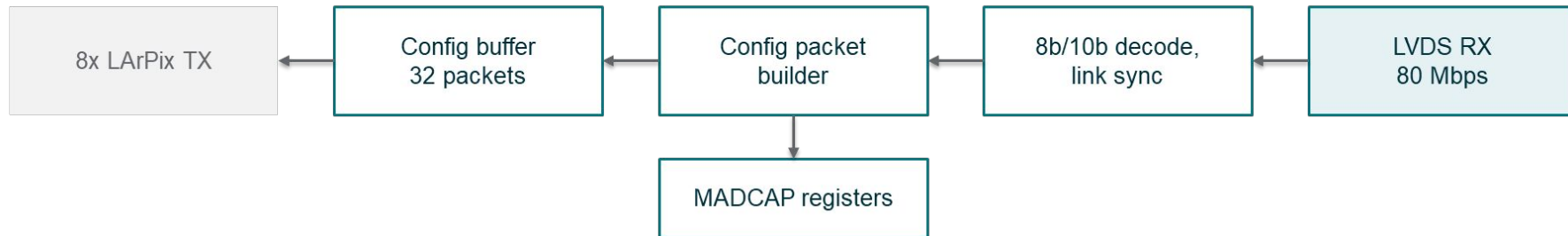
96-bit superpackets, 8b/10b-encoded to 120 bits
K-codes add flow control and commands



Downstream: LArPix data to PACMAN



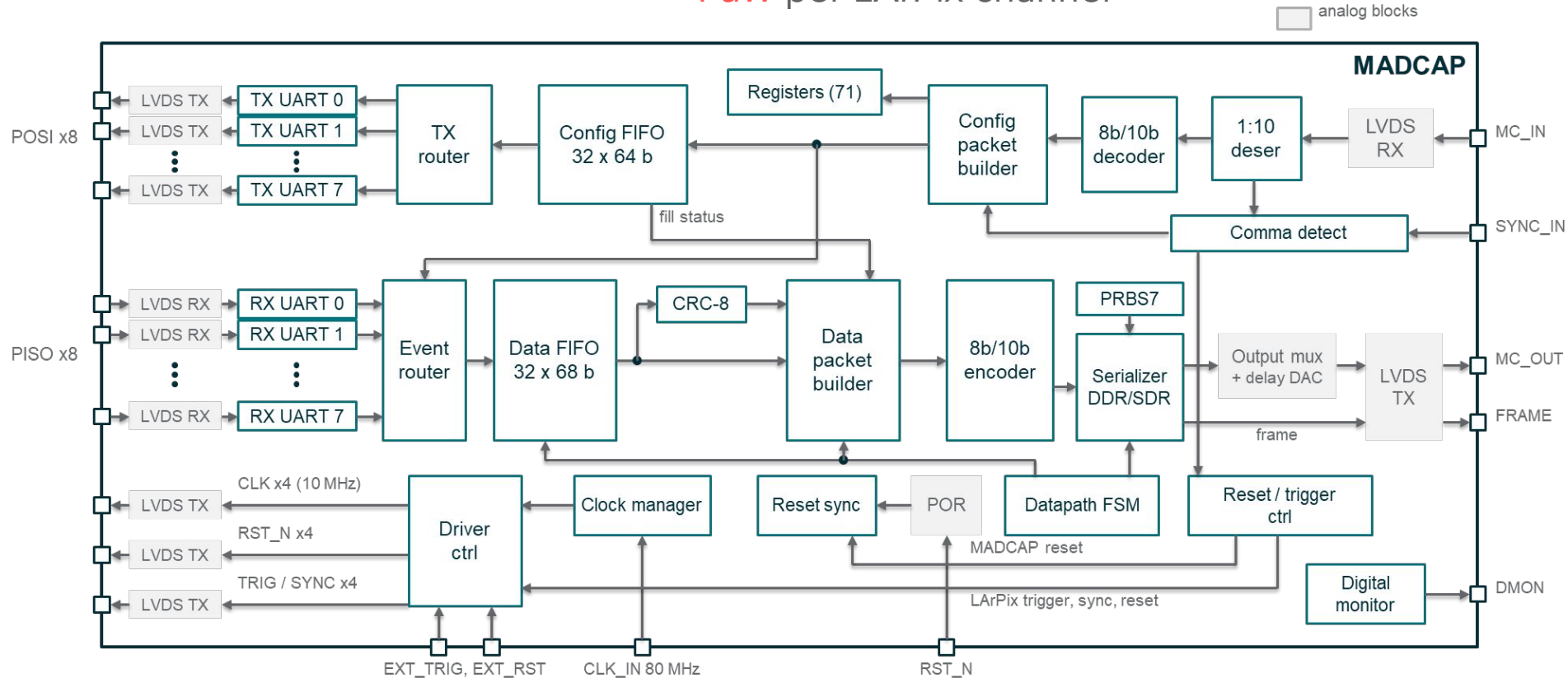
Upstream: configuration from PACMAN to LArPix and MADCAP



< 3.5 mW for
MADCAP => Warm
line driver

Inside MADCAP

Estimated ~ 40 mW for cold operation
 $\Rightarrow \sim 4$ μ W per LArPix channel



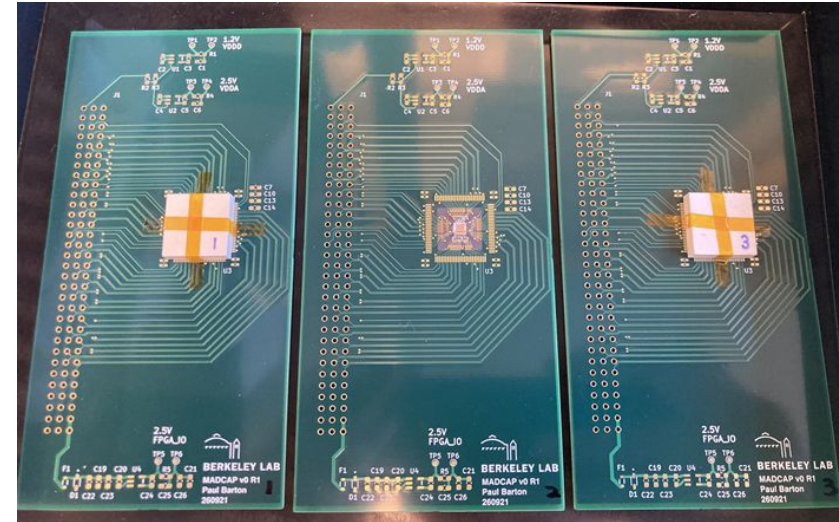
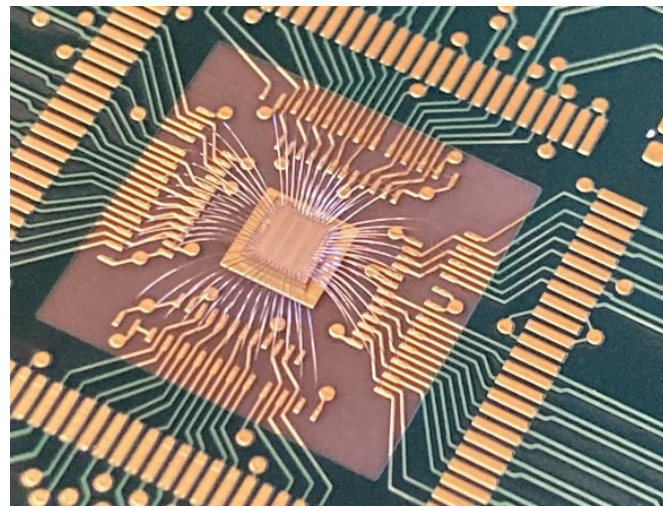
Current MADCAP Status

Chips taped out in June 2026

First dies bonded on smoke test board (MADCAP to FPGA) this month

- Power up tests, current checks, configuration read/write checks, test patterns through serial links

MADCAP-LArPix test boards are designed. Will fabricate and test with real LArPix tiles after smoke tests completed



Summary and Next Steps

LArPix is already a mature technology for pixel readout of LArTPCs, which will be used in DUNE's ND-LAr

Combining existing DUNE FD designs with LArPix offers a **scalable, technically ready** path to a multi-kiloton pixelated LArTPC

First major step is testing a full-size pixel CRP module. Assembly is completed, and the LAr run is planned for **October-November** this year

- Next major addition: **integration of MADCAP chip**. Tests of v1 beginning now
- Final milestone before DUNE FD is operation in a ProtoDUNE-III run, including every new component

LArPix Development Team



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