Thin-film detector R&D status overview

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CPAD Workshop 2026, Seattle, WA

October 22, 2026

Collaborators

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Argonne National Laboratory: Jessica Metcalfe, Sungjoon Kim

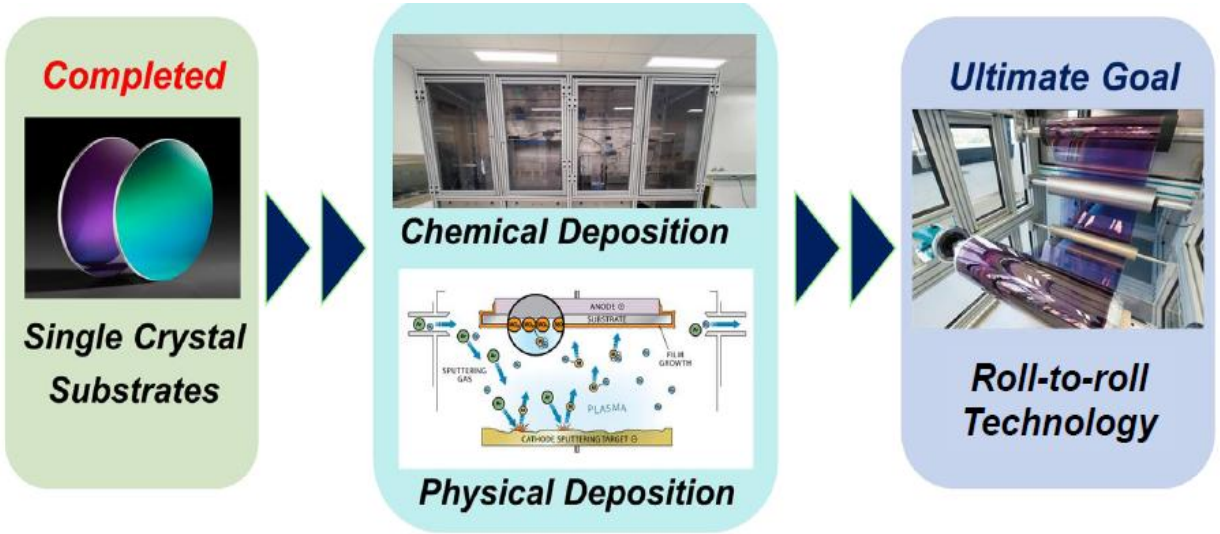
Lawrence Berkeley National Laboratory: Luc Le Pottier, Maria Mironova, Timon Heim, Maurice Garcia-Sciveres

Funding for this work was provided in part by the Department of Energy HEP IC Design Apprenticeship Program, grant number DE-SC0022296,
and Department of Energy Office of Science grant number DE-SC0021975, as well as Berkeley Lab LDRD

Motivation for thin-film detectors

Motivation and potential:

- Low mass
- Low material budget
- Large scale manufacturing
- ‘3D integration’ or monolithic detector: avoid hybridization for small pixels, keep low interconnect capacitance
- Access to different semiconductor materials



Thin film technology is already being utilized in HEP detectors:

- *High-resistivity epitaxial Si on low-res substrate, e.g. for LGADs: deposition is done as a thin film onto a substrate (of identical material and crystal structure), but result is a ‘thick’ substrate for hybrid detector*
- *CVD polycrystalline diamond: used for ‘bulk’ material deposition*

*S. Kim, V. Berry, J. Metcalfe, A.V. Sumant, Thin film charged particle detectors. JINST **18** (2023)*

Motivation (and outline)

Indium Phosphide (InP)

- Very high electron mobility
- Crystalline thick wafers purchased commercially, single- and multi-pad sensors fabricated as prototypes and references for future CVD InP layers
- *Photonic IC platform*

Amorphous Selenium (a-Se)

- Successfully used in direct conversion flat-panel X-ray detectors
- Photoabsorption in the UV-vis range for scintillating light detection
- Low-temperature evaporation: integration directly on CMOS

Some related talks at this workshop!

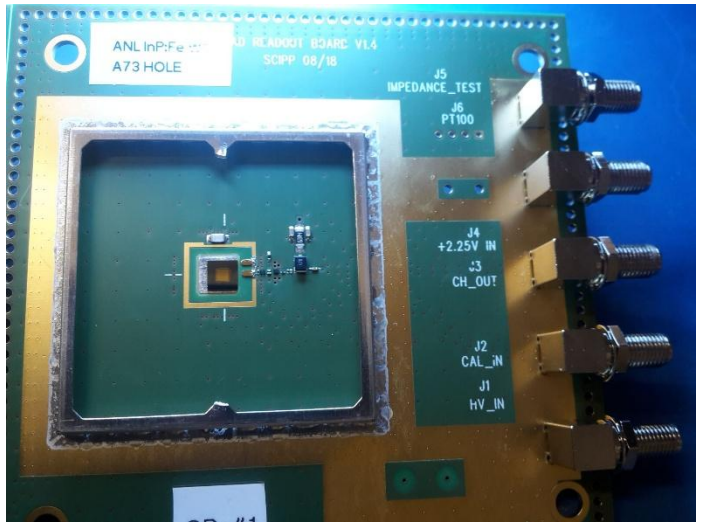
Amorphous Silicon (a-Si)

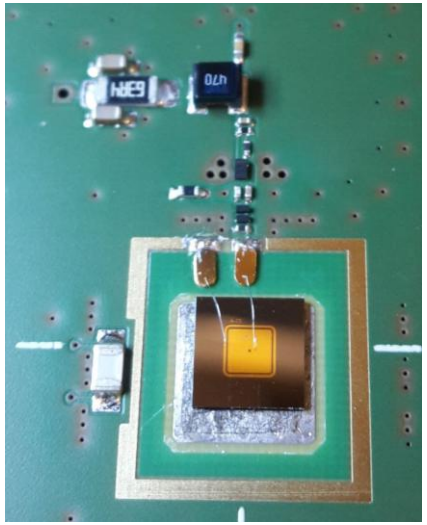
- Previously studied detector material
- Silicon properties well understood, deposition processes available

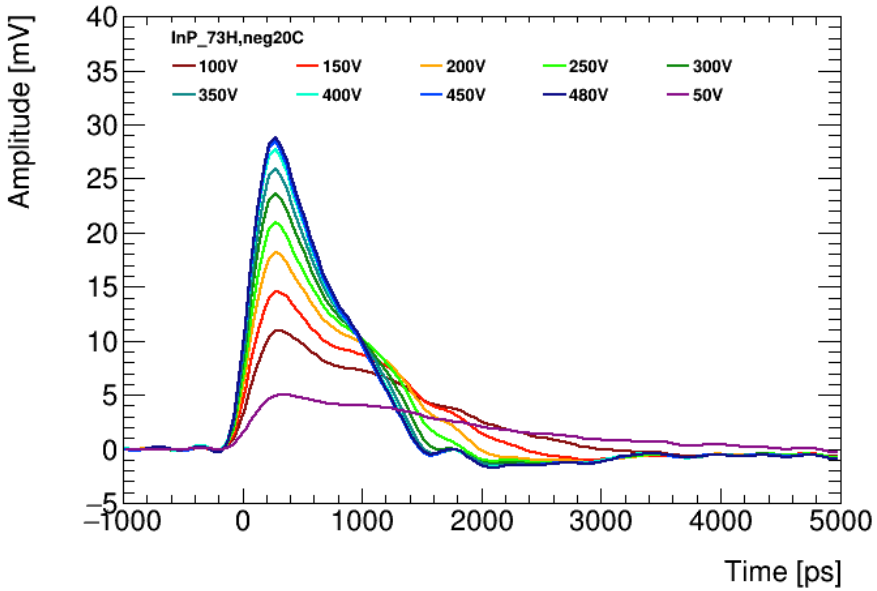
Not covering SiC and diamond detectors here!

Displayed examples biased towards own and UH work

InP sensor studies: single-pad devices

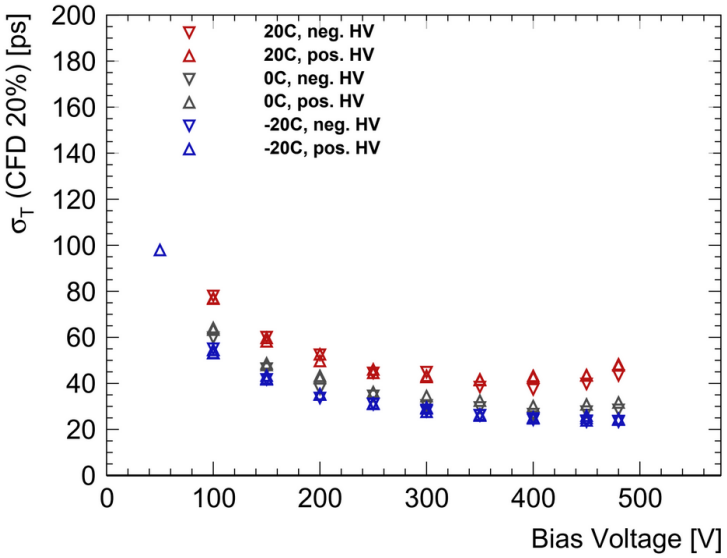




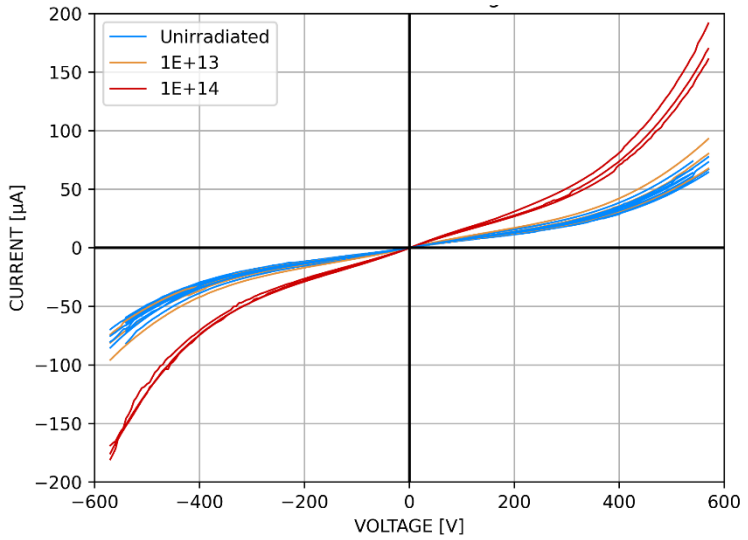


- **350 µm single-pad sensor with or without optical opening**
- **Bonded to 1-ch UCSC fast readout board, characterized with laser and Sr-90 source**
  - Small signal: 15-30 meV
  - Rise time down to 250 ps after 150 V
  - Excellent timing resolution: 33 ps reached between 300 and 400 V

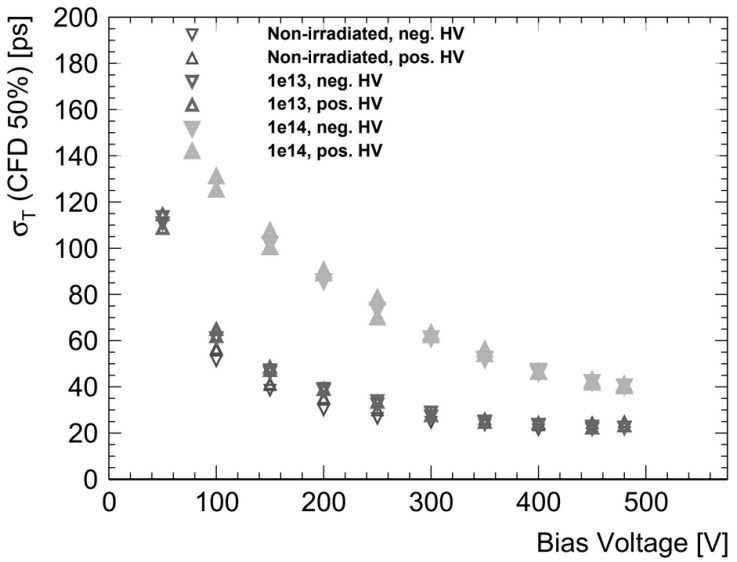
InP sensor studies: single-pad devices



I-V at room temperature



Sr-90 source, 0 C



- **Sensors irradiated to 1e13, 1e14, 1e15, 1e16 n/cm² at JSI/Ljubljana with 1 MeV neutrons**
  - High activation with In-114m in higher fluences
  - Leakage current increases; collected charge, pmax decrease
  - Timing resolution can be retained below 60 ps by cooling

InP sensor studies: single-pad devices

- **Modeling of signal formation and drift: study in upcoming publication**

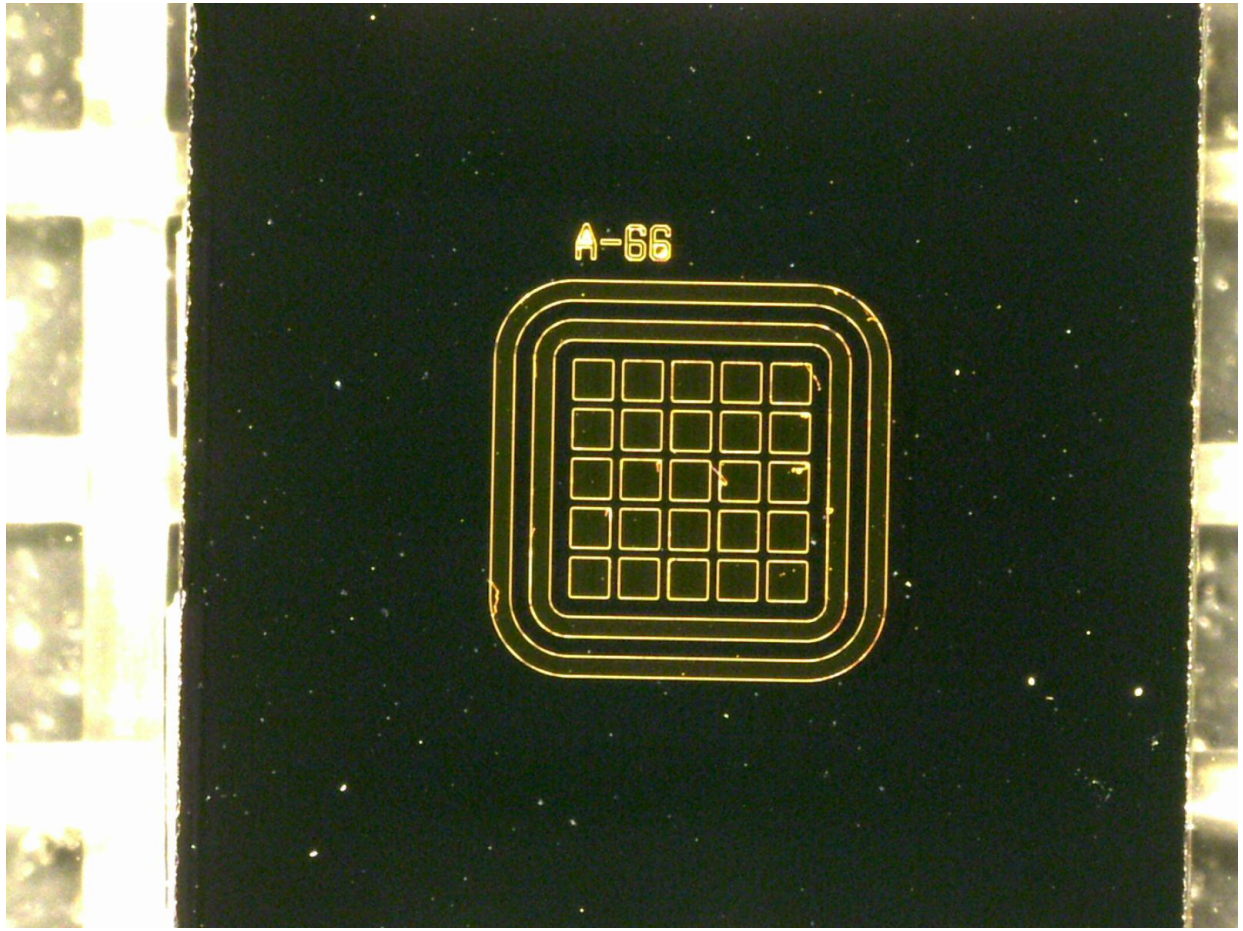
- **Studied at DLS / CLS x-ray beamlines**
  - In DC, not pulse mode: measuring leakage currents, mapping response as function of beam position
  - Deconvolution of temperature-dependent generation current vs beam-induced photocurrent, in Geant4 + TCAD simulations

InP sensor studies: multi-pad devices

5x5 pad array, fabricated on the same substrates as single-pad sensors

- **200 µm pixel size, 50 µm gap**

- **Red laser TCT scan**
- **TCAD simulation of electric field / weighting field**
- **Charge injection simulation by Heavylon model**

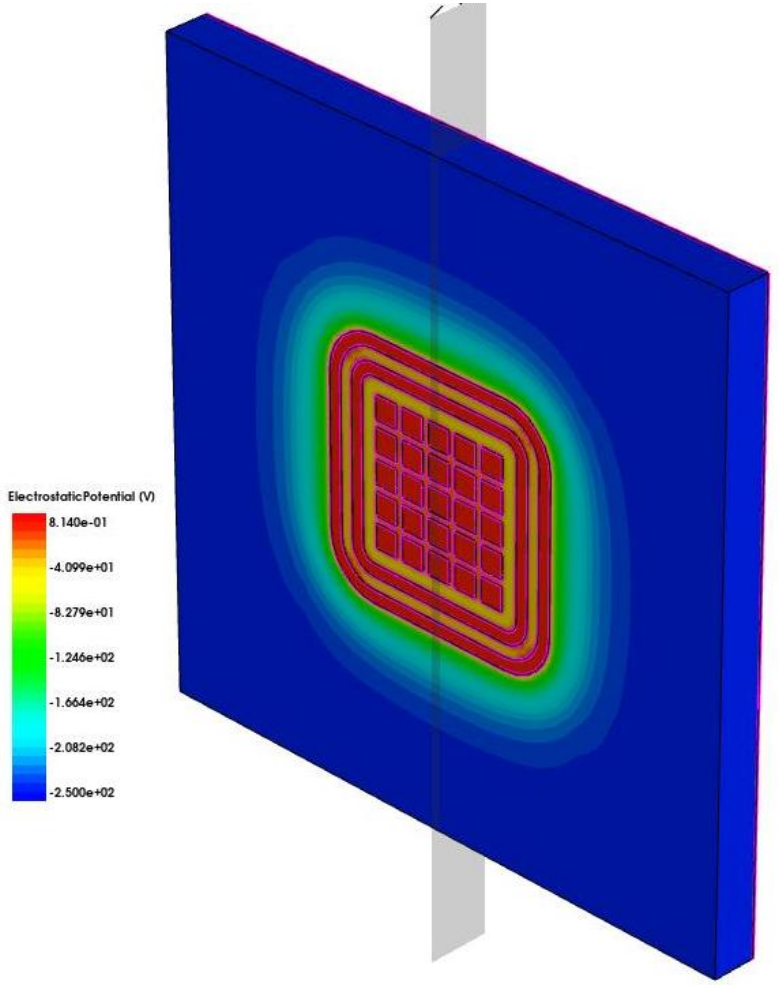


InP sensor studies: multi-pad devices

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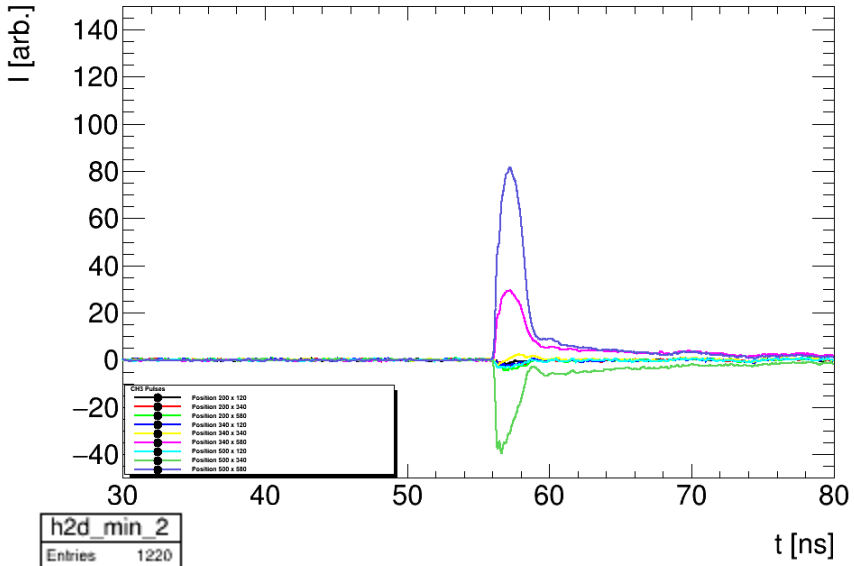
- ➢ **Red laser TCT scan**
- ➢ **TCAD simulation of electric field / weighting field**
- ➢ **Charge injection simulation by Heavylon model**



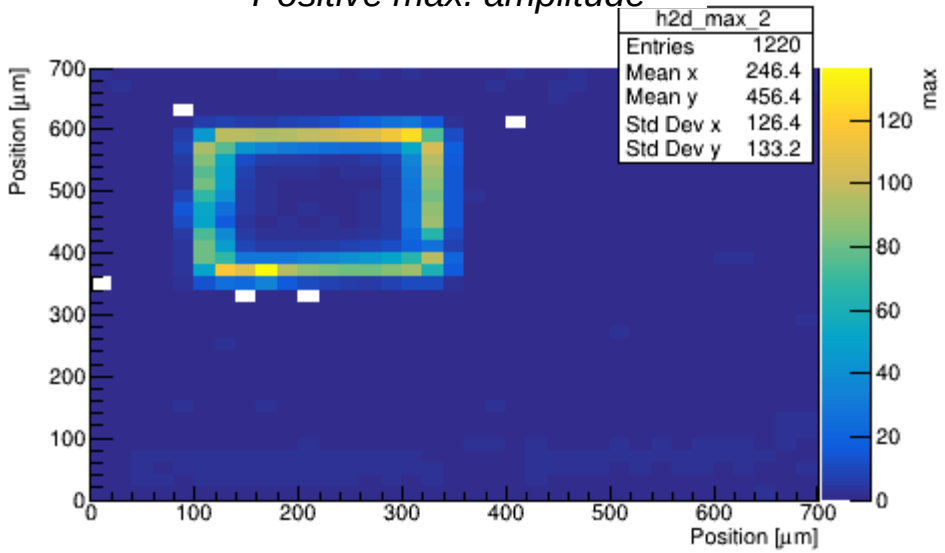
InP sensor studies: multi-pad devices

Red laser injection on segmented side: large cross-talk observed on next neighboring pad

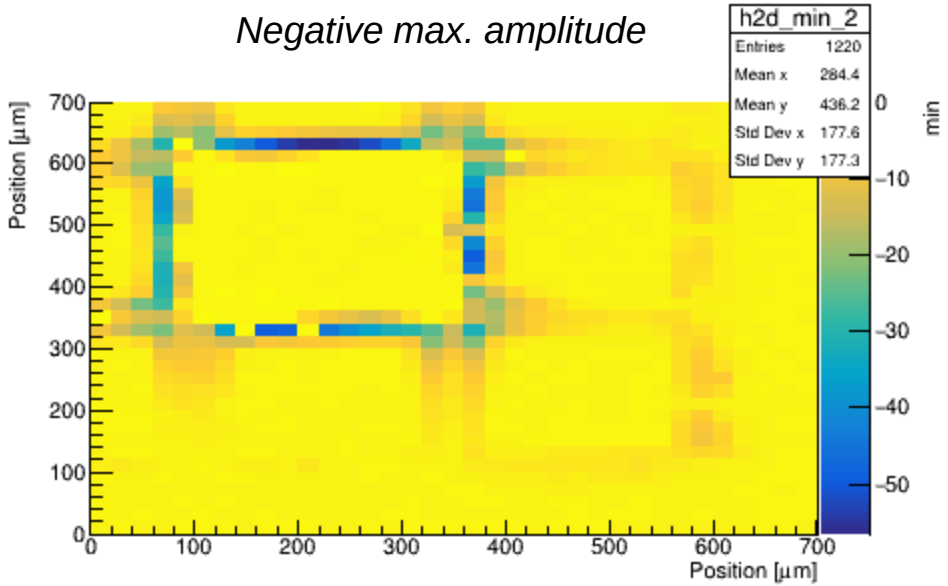
- Utilize for position reconstruction?



Positive max. amplitude



Negative max. amplitude

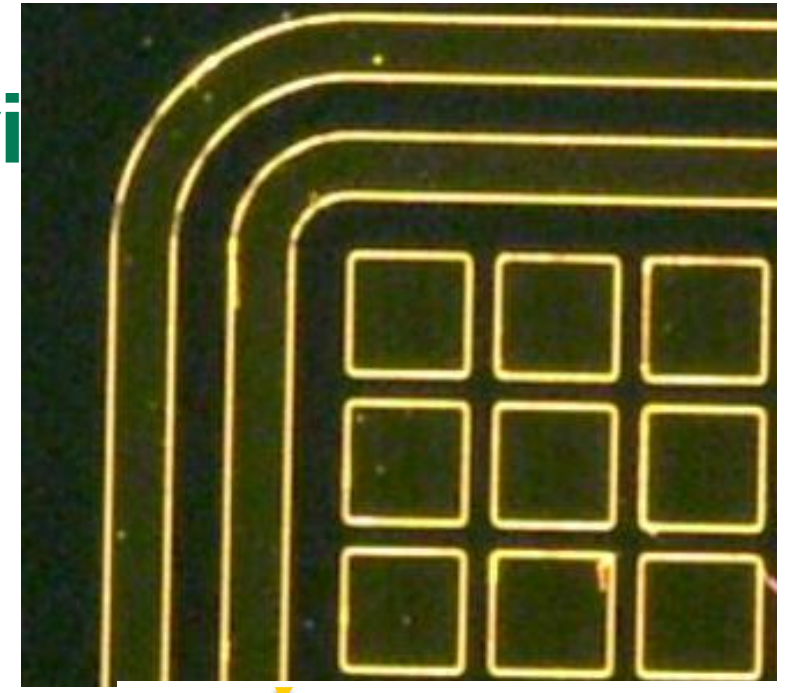


InP sensor studies: multi-pad devi

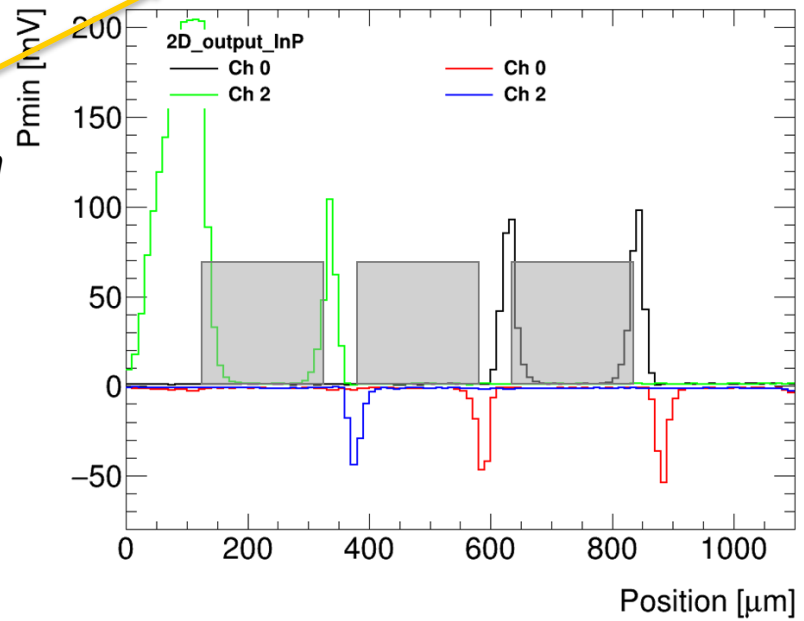
Red laser injection on segmented side: large cross-talk observed on next neighboring pad

- Utilize for position reconstruction?

- Initial TCAD simulations do not confirm this observation for injected MIP – effect due to laser absorption close to the surface, as opposed to bulk charge generation?



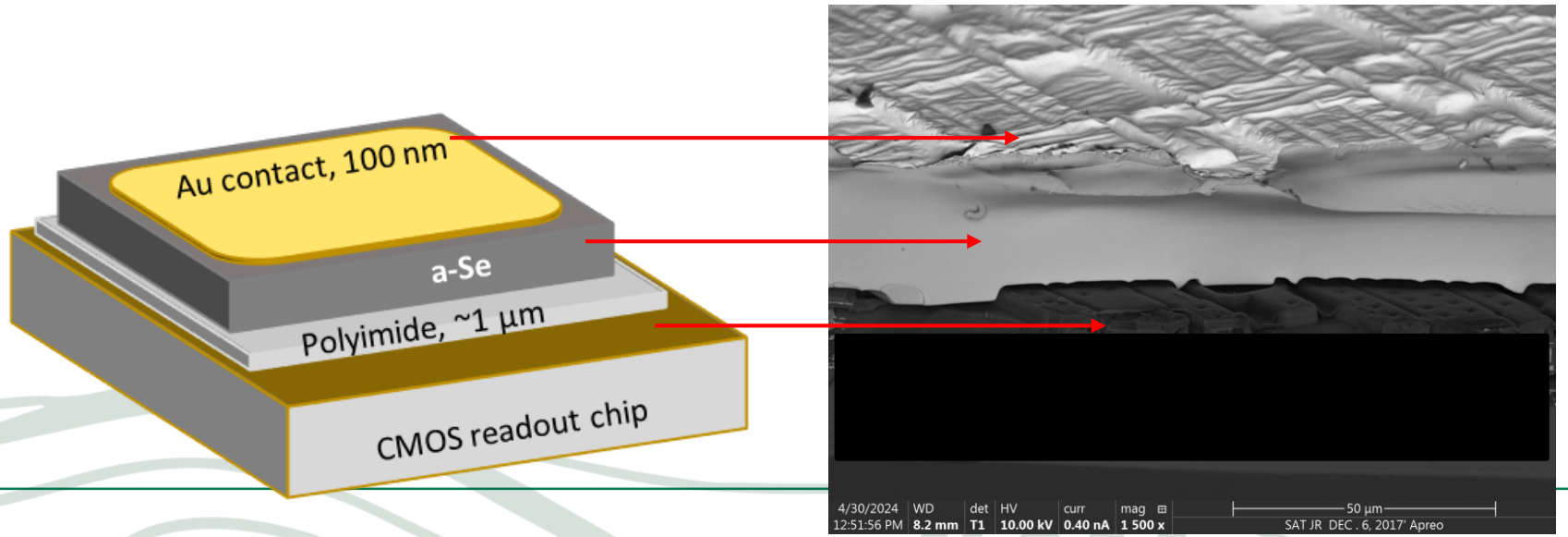
Larger signal between pad and guard ring



aSe on CMOS device fabrication

Fully processed and diced single ITKpix v2 chip

- Spin coating of polyimide hole-blocking layer, 1-1.5 µm, bake at 300-350 C
- Stabilized amorphous selenium (0.2% As, 10 ppm Cl) deposited via thermal evaporation in a dedicated selenium evaporator at 100 Å/s
- Gold top electrode deposited by electron beam evaporation



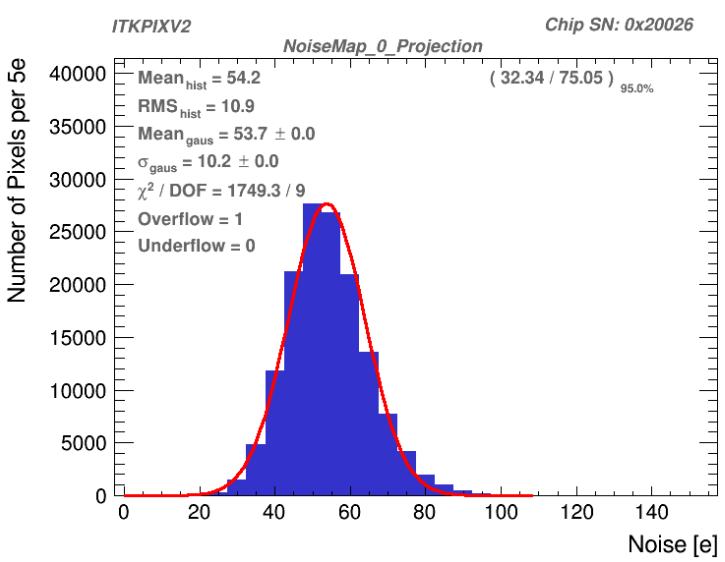
SEM cross-section of an a-Se / CMOS sensor, here with 25 µm a-Se

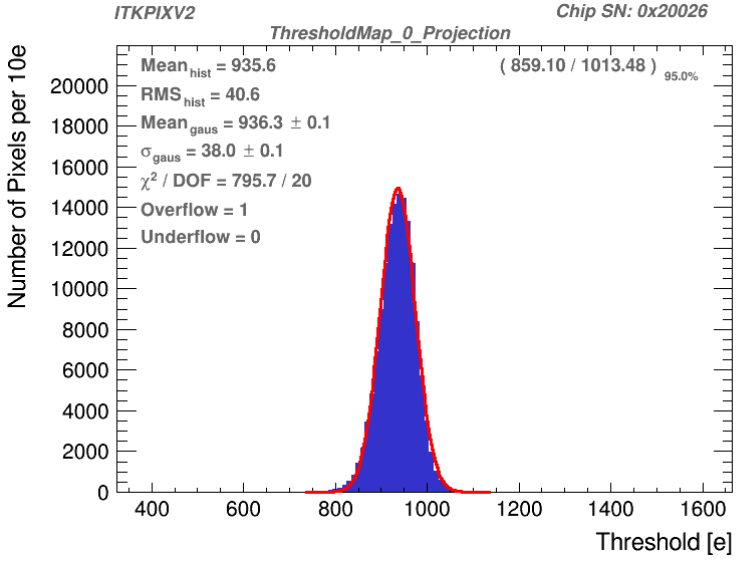
J. Ott, L. Le Pottier, K. Hellier, A. Swaby, M. Mironova, T. Heim, C. Hultquist, M. Garcia-Sciveres, S. Abbaszadeh, *A-Se thin film detector on ITkpix CMOS readout: time-over-threshold tuning and pixel performance analysis*, Proceedings of SPIE Medical Imaging (2025), 13405, 134050D, https://doi.org/10.1117/12.3049041

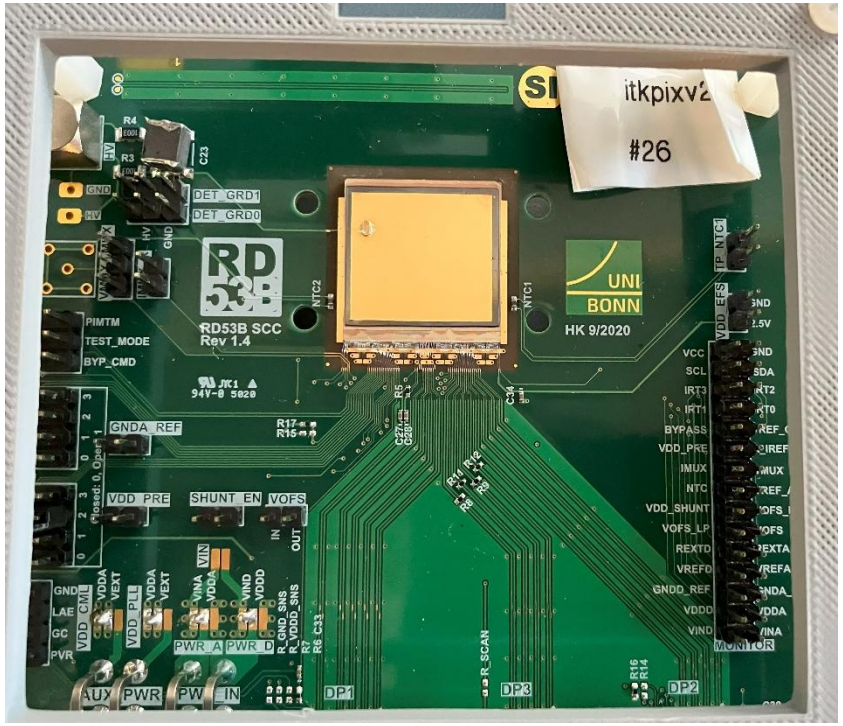
Sensor testing

ITkpix v2 chip with a-Se layer is mounted on a single-chip readout daughter board, tuning and data acquisition with YARR firmware/software framework

- Tuning of thresholds to 800-1000 e^-
- Noise 45-55 e^-





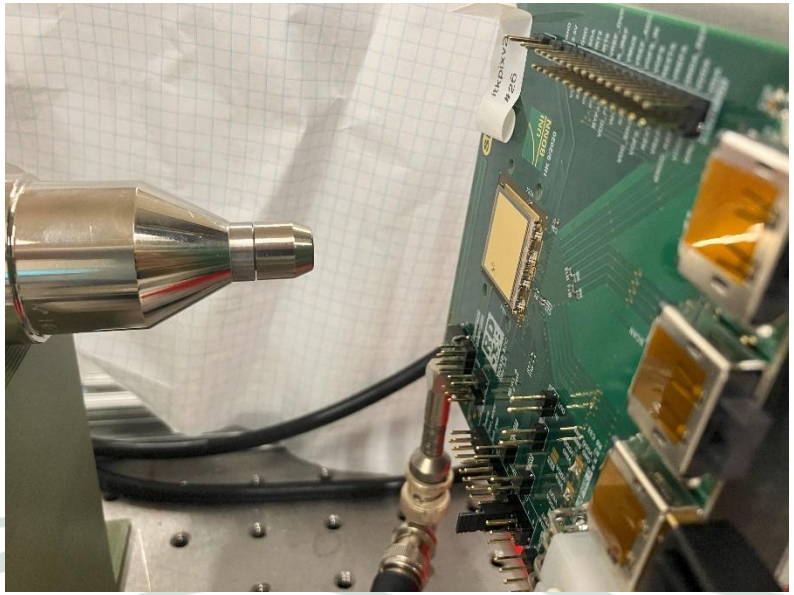


https://yarr.web.cern.ch/yarr/

Sensor testing

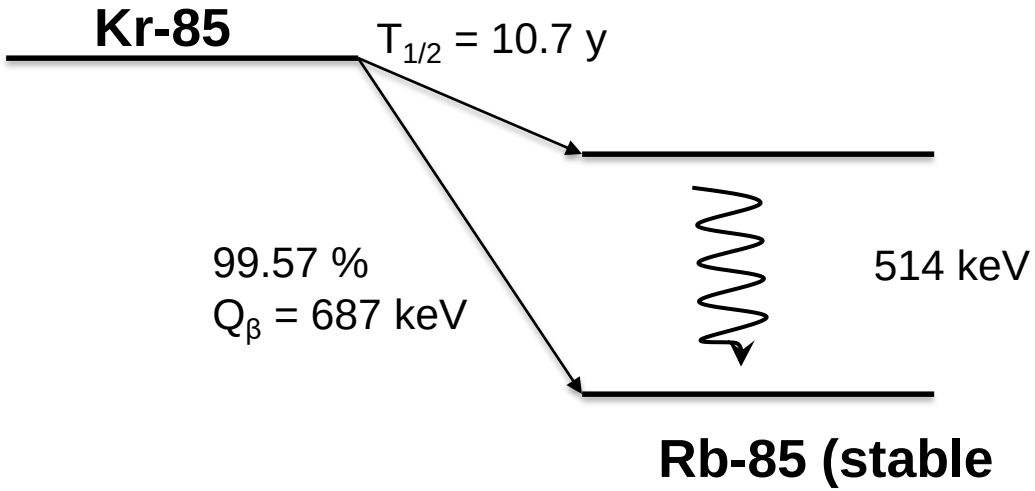
X-rays

Amptek Mini-X2 tabletop X-ray gun, max. 50 kV



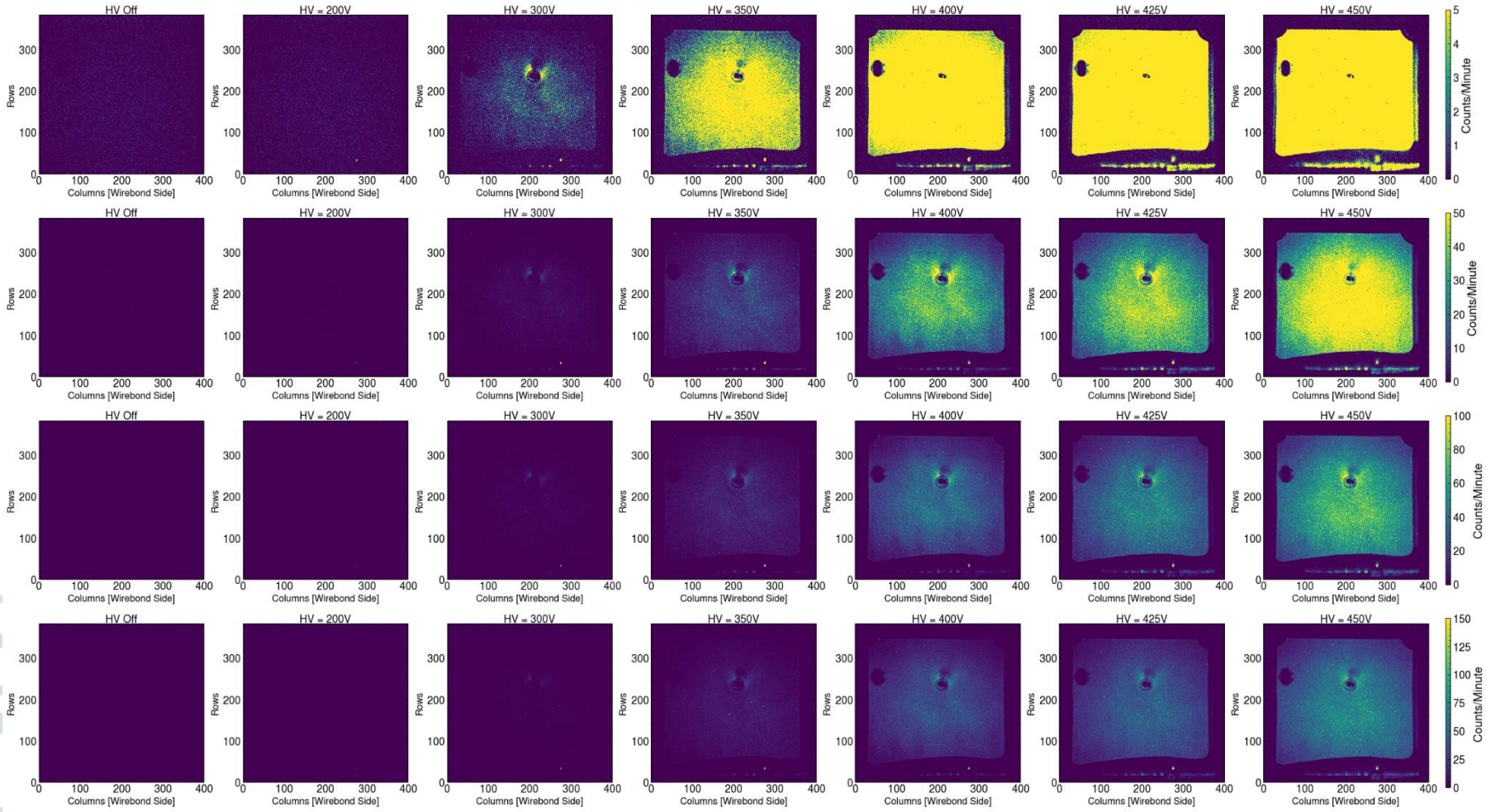
Kr-85

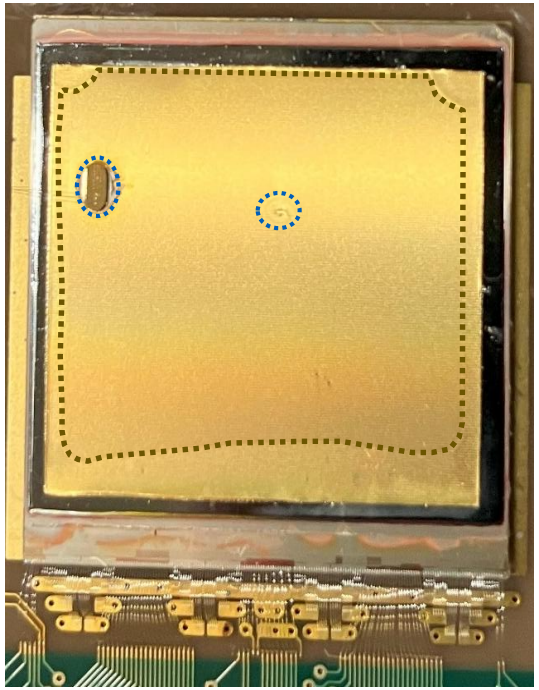
Low-energy beta particles (electrons), average energy 251 keV



Hit maps

Studying the response of a-Se as function of applied bias voltage:

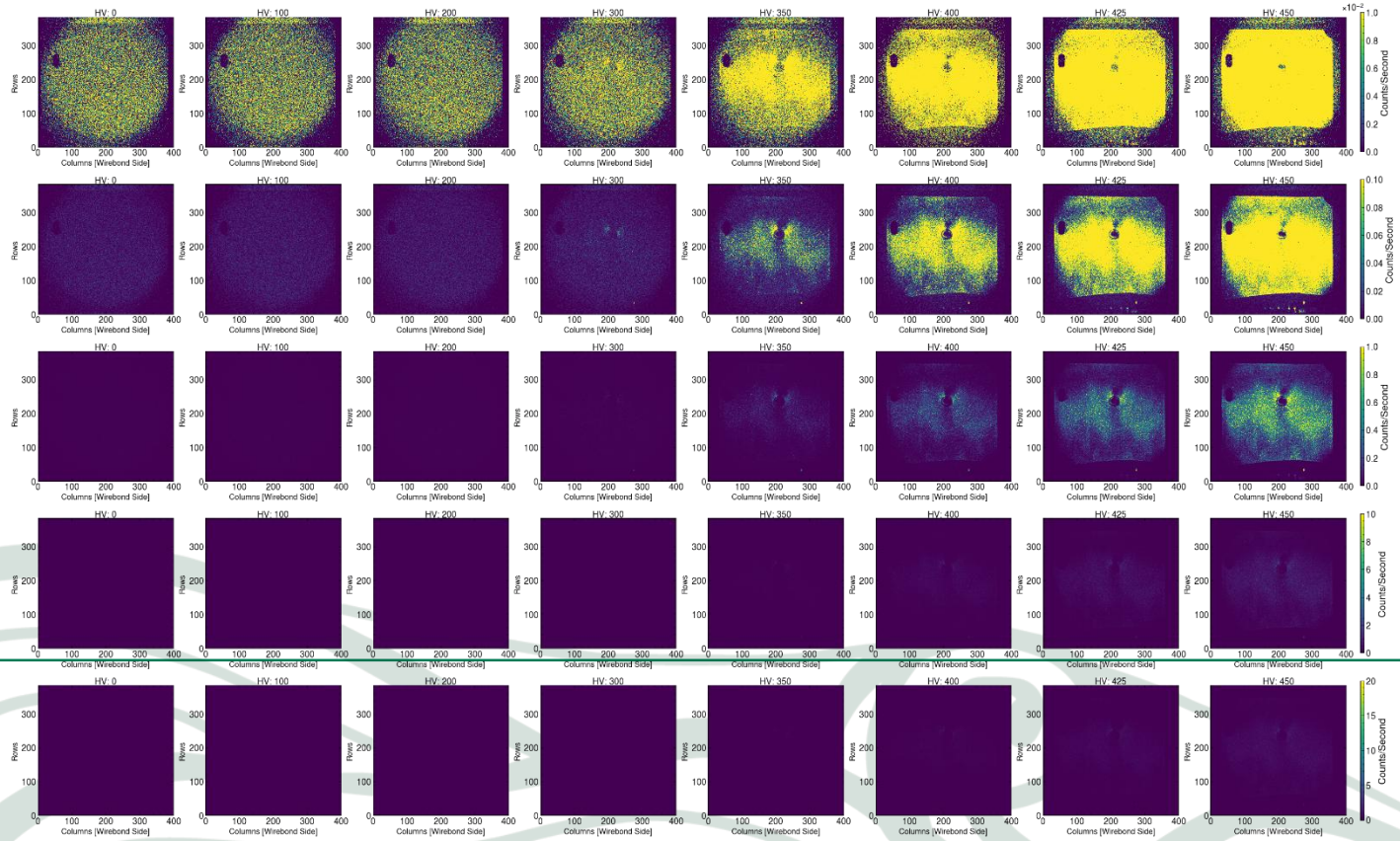




55 µm a-Se, Kr-85 source

Hit maps

Response of a-Se to X-rays, as function of bias voltage: similar as for Kr-85, hits in chip better visible

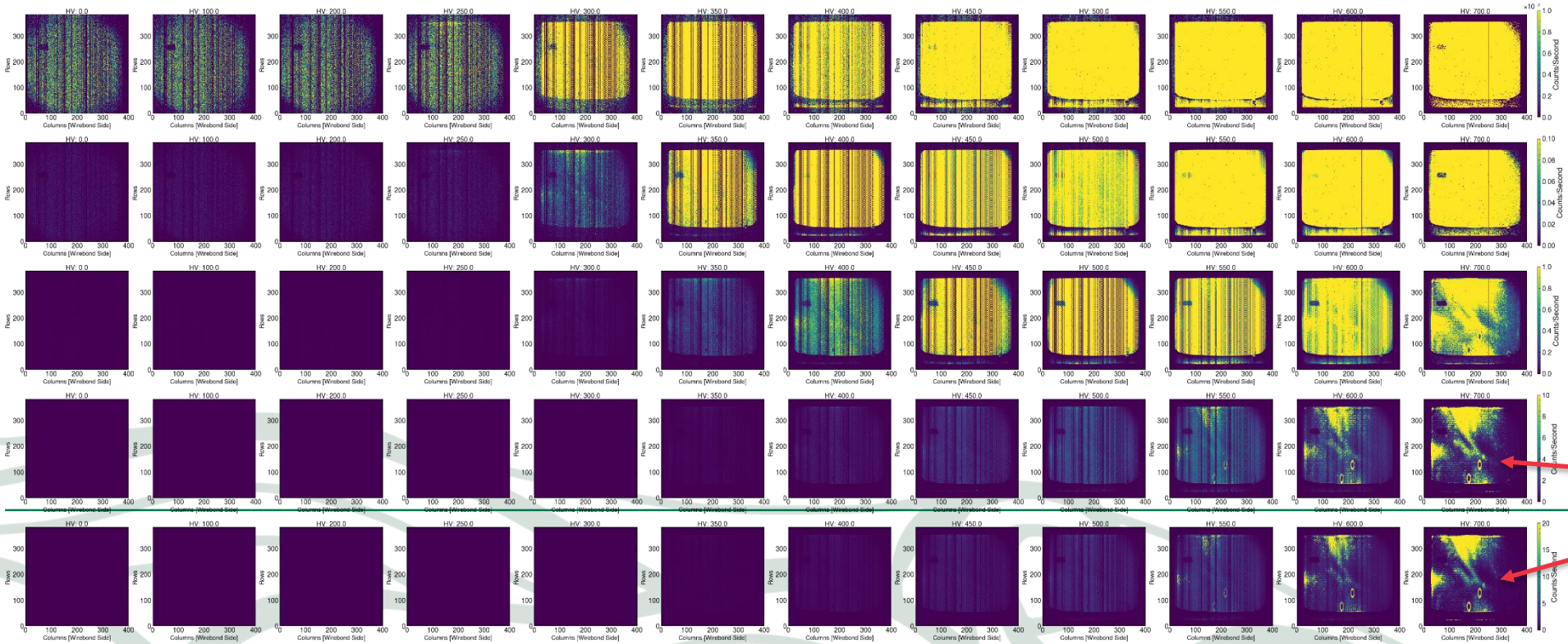


55 µm a-Se, X-ray tube

Hit maps

Response of a-Se to X-rays, as function of bias voltage: similar as for Kr-85, hits in chip better visible

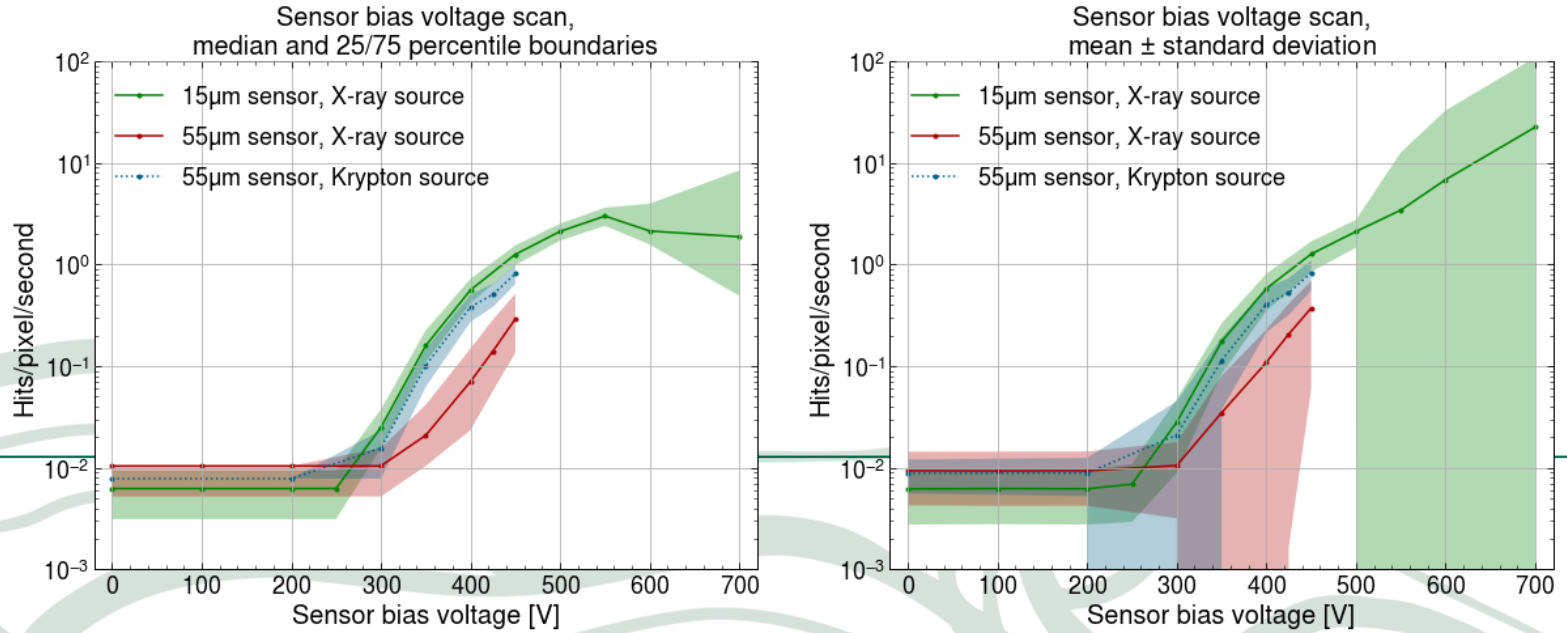
- Sample with 15 µm a-Se: at highest bias voltage < 600 V, erratic hit rates indicate higher local fields



15 µm a-Se, X-ray tube

Hit rates

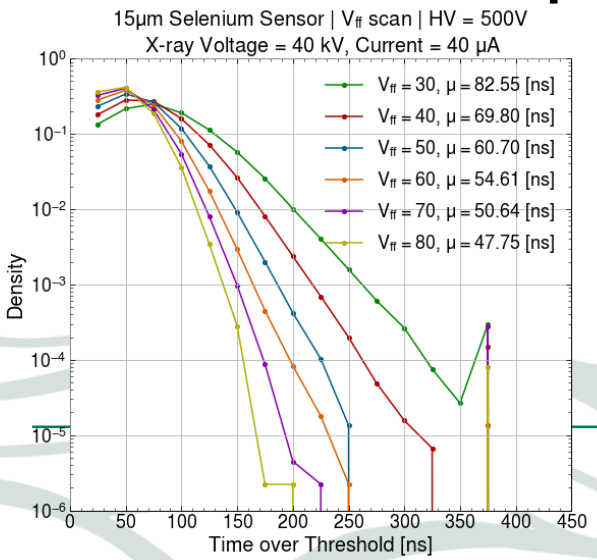
- As seen in previous images, an applied bias voltage of ~300 V or above is required for detectable hit efficiencies
- This point is very similar in all test series: also includes voltage drop across the polyimide layer
- Hit rates are higher in 15 µm layer than in 55 µm
- *If examined as function of V/µm, the 15 µm layer would show increase in efficiency only at higher fields: favorable weighting field counteracted by lower absorption efficiency*

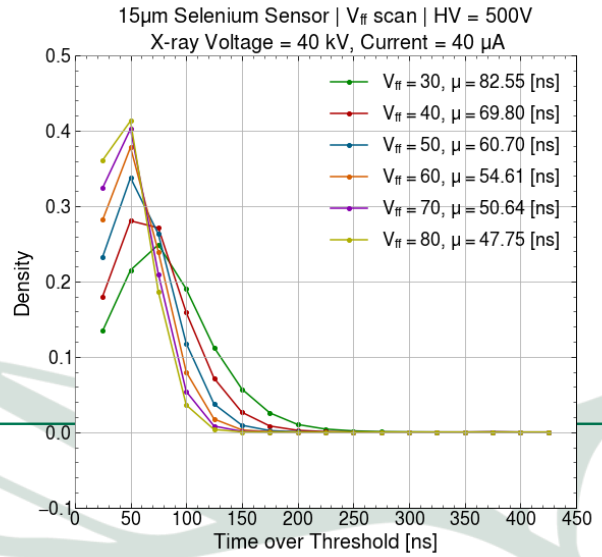


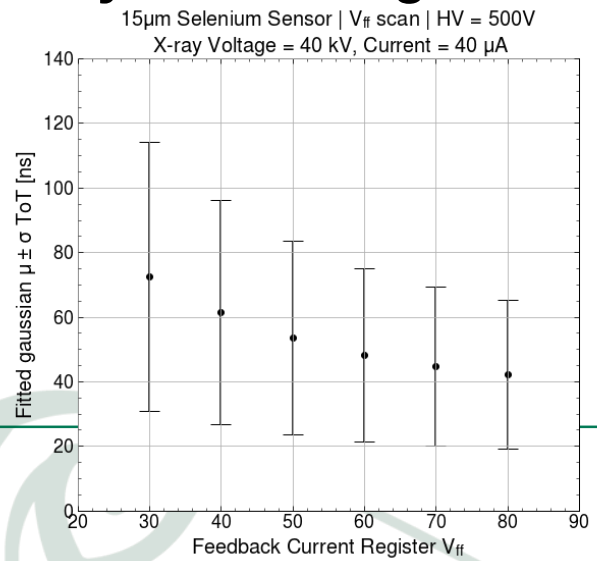
Feedback current register V_{ff}

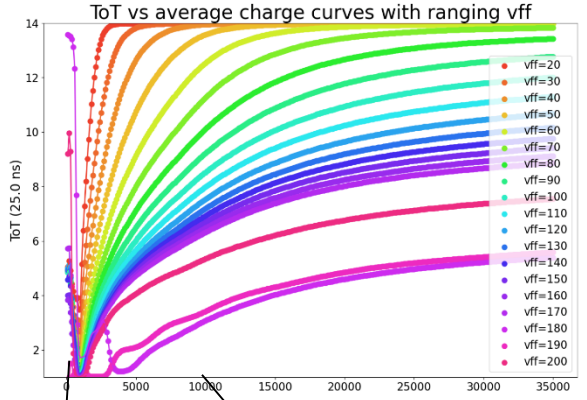
For tests with 55 µm a-Se sample, the ToT mean remained low even at higher electric fields – in X-ray test series on the 15 µm sensor, adjustment of the preamplifier feedback current was studied systematically

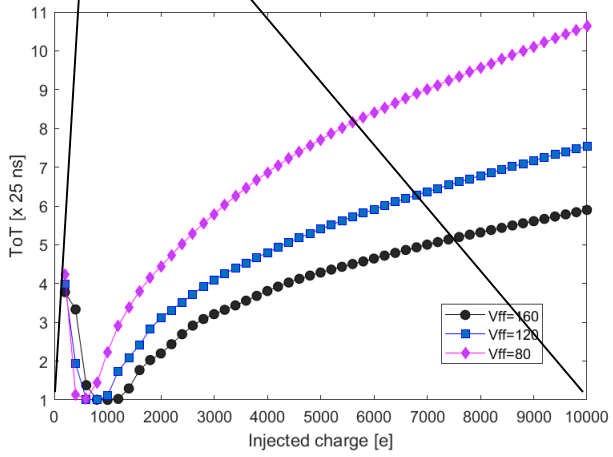
- **Clear increase in ToT as Vff is lowered, in otherwise identical conditions**
- **Mean value of the ToT distribution still remains < 4 (100 ns), does not make optimal use of the available dynamic range**







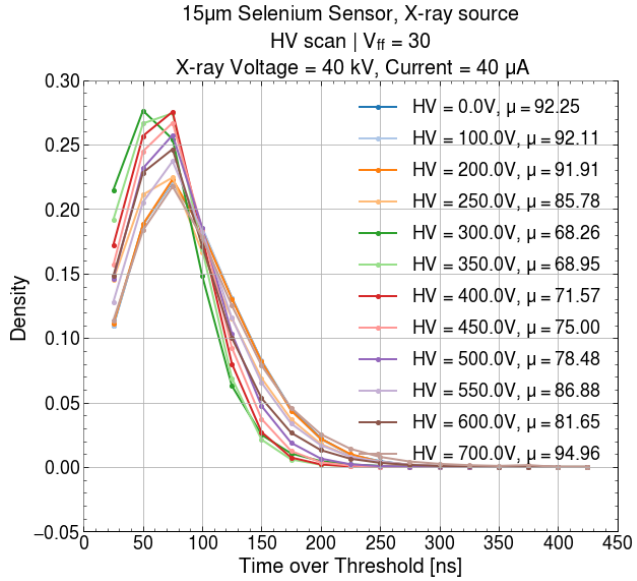


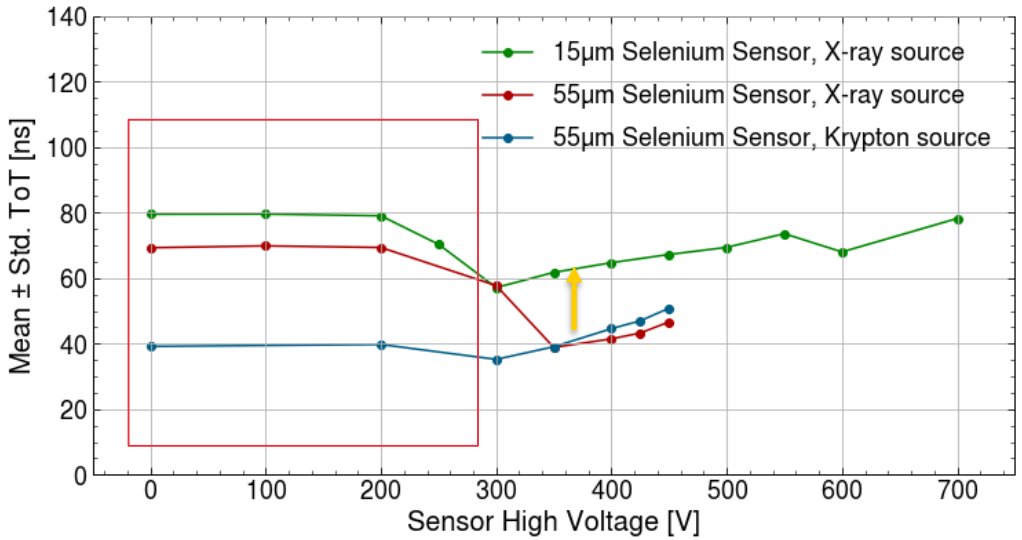


Time-over-Threshold

- **Time-over-Threshold distribution shifts to higher values as bias voltage is increased**
  - ➢ *More signal charge collected*

- Lower feedback current improves utilization of ToT dynamic range: maximum of distribution now extends towards 8-10 (x 25 ns)
- Broad distribution over all pixels, mean remains below 50% of dynamic range; resolution between different voltages is not very high
- *At lower voltages, limited by statistics of active pixels (most hits will not be registered, as they do not pass the pixel hit threshold)*





CMOS+X

https://nw-ai-hub.org/collaboration/cxr-pilot-run

CMOS+X: integration of standard Si CMOS processing + *other process*

X: RAM, MEMS, CNFET, photonics, …

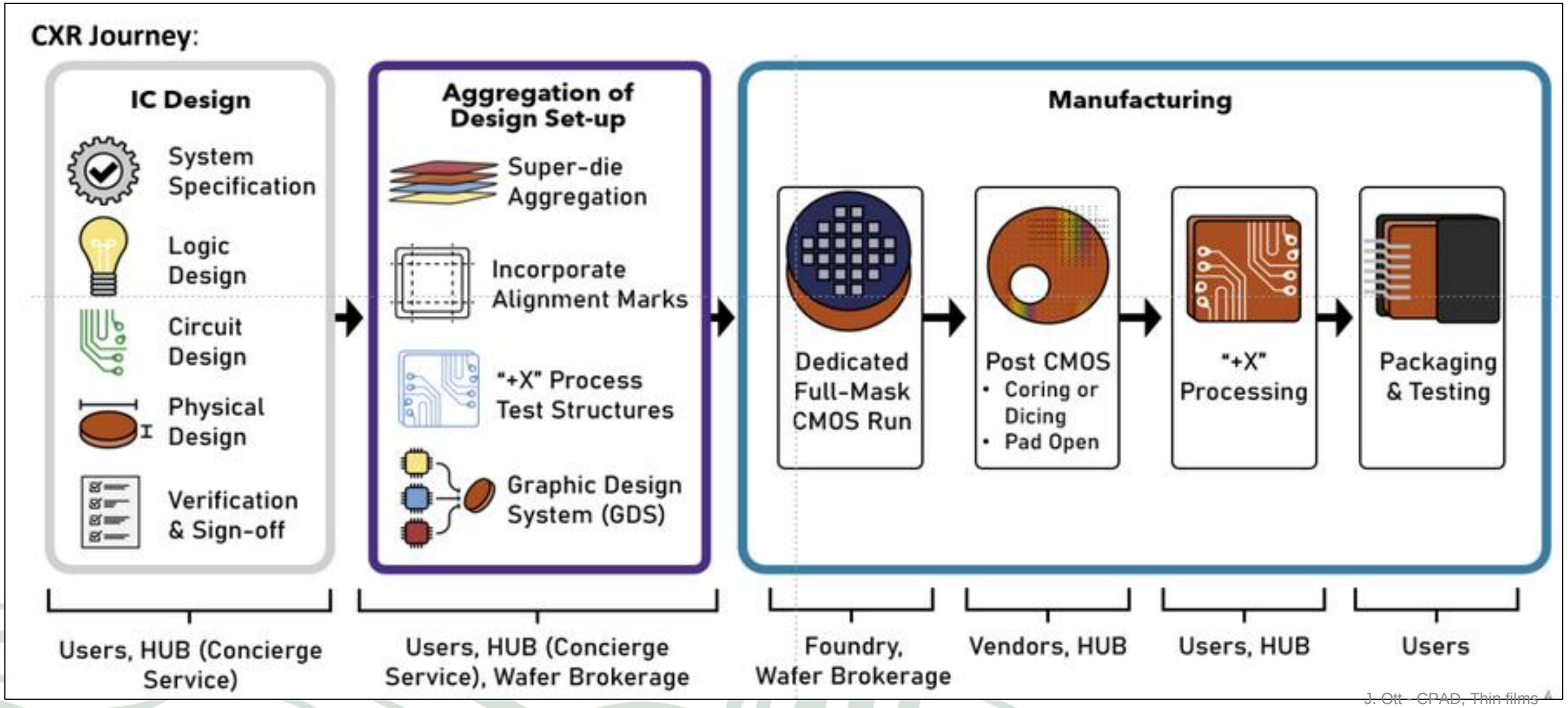
Here, at the metal level – eventually, pathways down to adaptation during CMOS process or even on transistor level

- Pilot run through Pacific Northwest AI Hub: improve ‘lab to fab’ pipeline for integration of standard CMOS process with commercial foundry with custom post-processing; provide a demonstration case for the microelectronics community
- Shared run of 10 (20) users, Hub coordinates with wafer brokerage (MUSE) and provides full mask set
- **First shuttle in 2025/2026: TSMC 40 nm, second in 2026: TSMC 28 nm**
- *User is responsible for both design and post-processing*

Targeting a contribution to LBNL submission slot

Cf. Timon’s talk: https://indico.global/event/17230/contributions/169739/

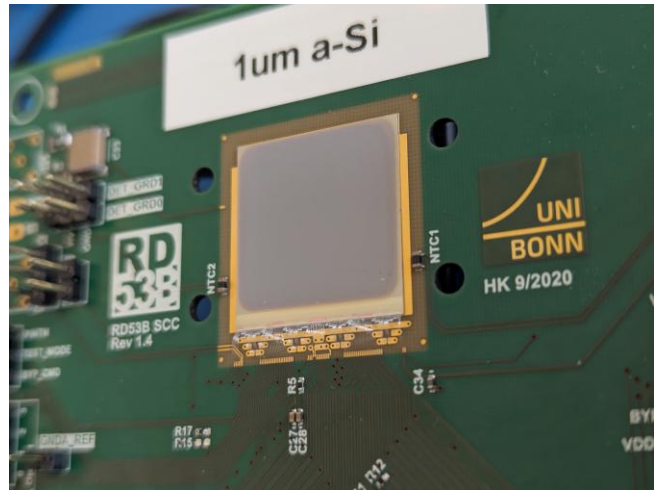
CMOS+X

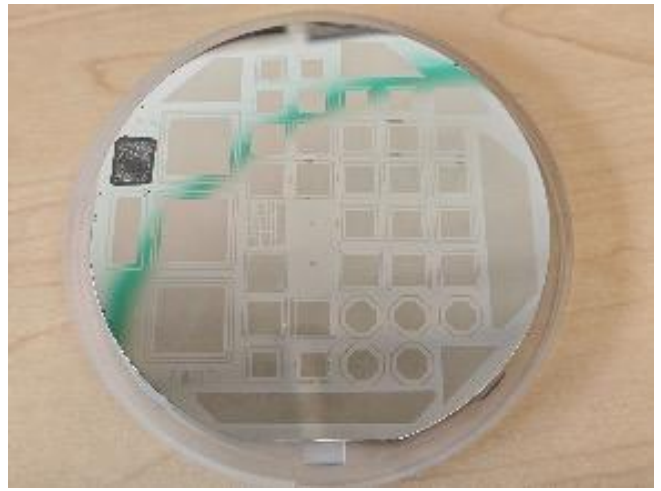


CXR one-page flyer

Other ongoing and future work

- **aSe / Te superlattices at UCSC: presentation by T. Schnell https://indico.global/event/17230/contributions/169765/**
- **CVD setup commissioning at ANL: pending safety reviews**
- **a-Si at LBNL**
  - Wafer with test devices fabricated: challenges with leakage current, solution with temporary metal?
  - Deposition on CMOS, similar to a-Se
- **a-Si through UH**
  - Collaboration with University of Siegen, Germany: deposition of doped a-Si onto CMOS, planned to start early next year
- ***Exfoliation of solar absorbers, transfer onto pixelated CMOS chip: cf. next slides, taken from Nico Gaillard / UH***

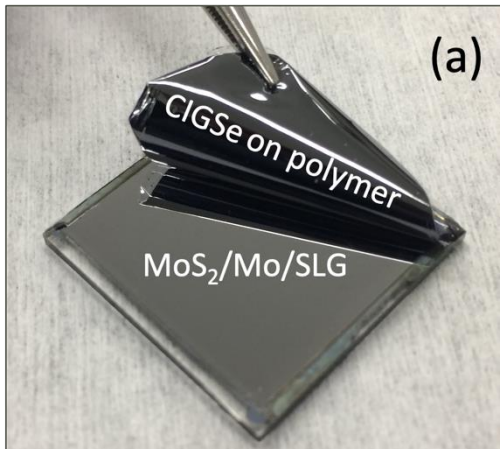




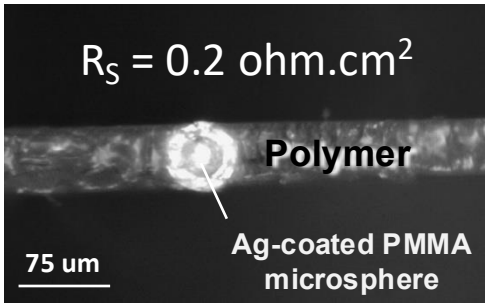
Multi-junction chalcopyrites

→ Mechanically weak **2D $Mo(S,Se)_2$** interlayers naturally form when chalcopyrite thin films are deposited on Mo, which serves as the separation layer for **exfoliation**.

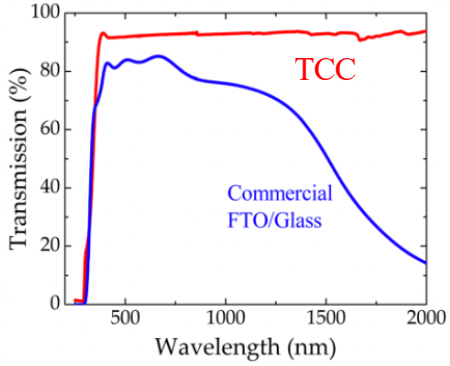
→ Transparent conductive composite **(TCC)** to **bond** new host substrates (i.e., FTO) to chalcopyrite devices and maintain electrical access to top contact of PV device.

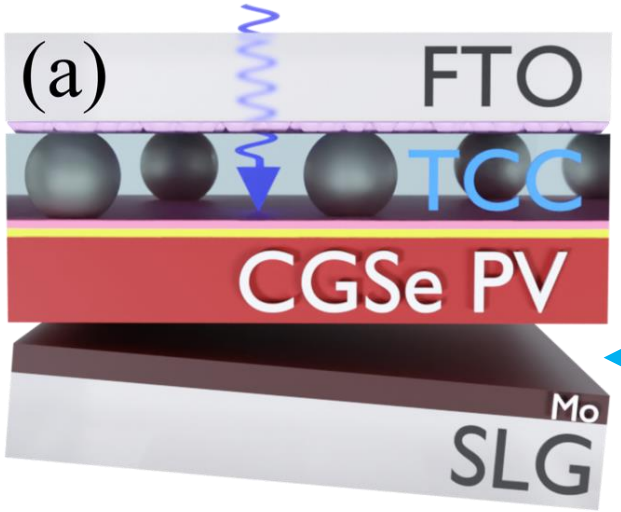








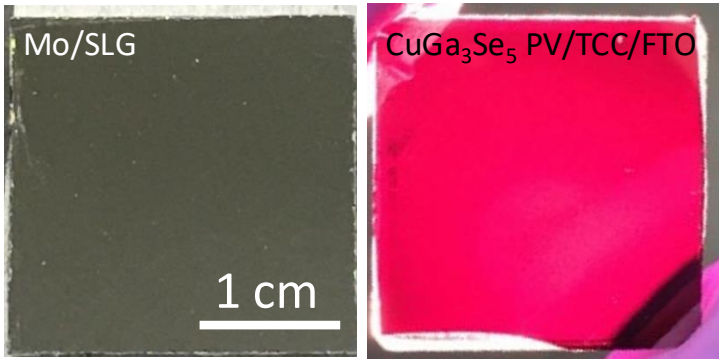




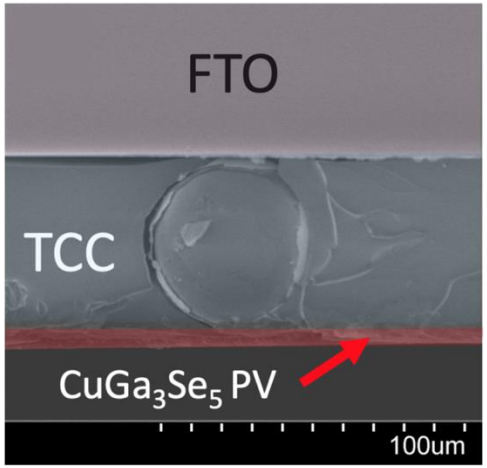
Multi-junction chalcopyrites

→ **Exfoliation and transfer of fully processed grid-less $CuGa_3Se_5$ PV (with CdS/ZnO/AZO)**

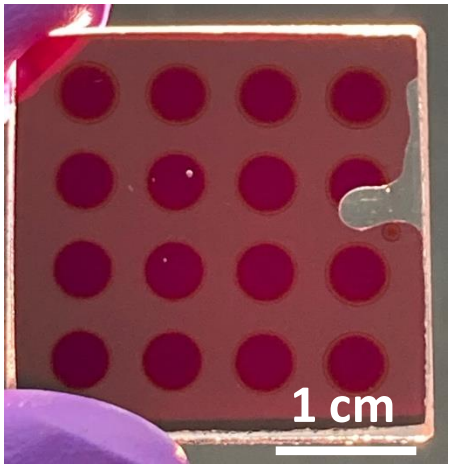


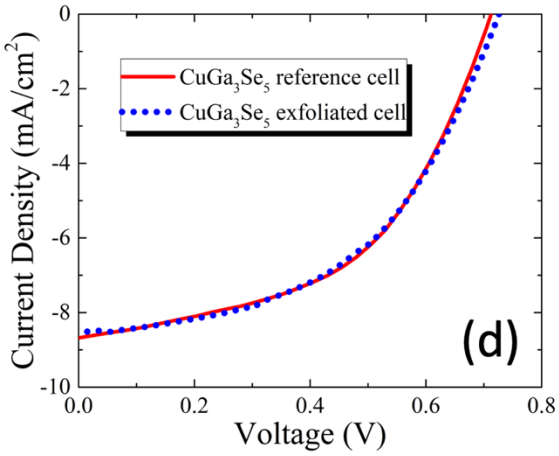


→ Controlled exfoliation of chalcopyrite PV as large as 1” x 1”.

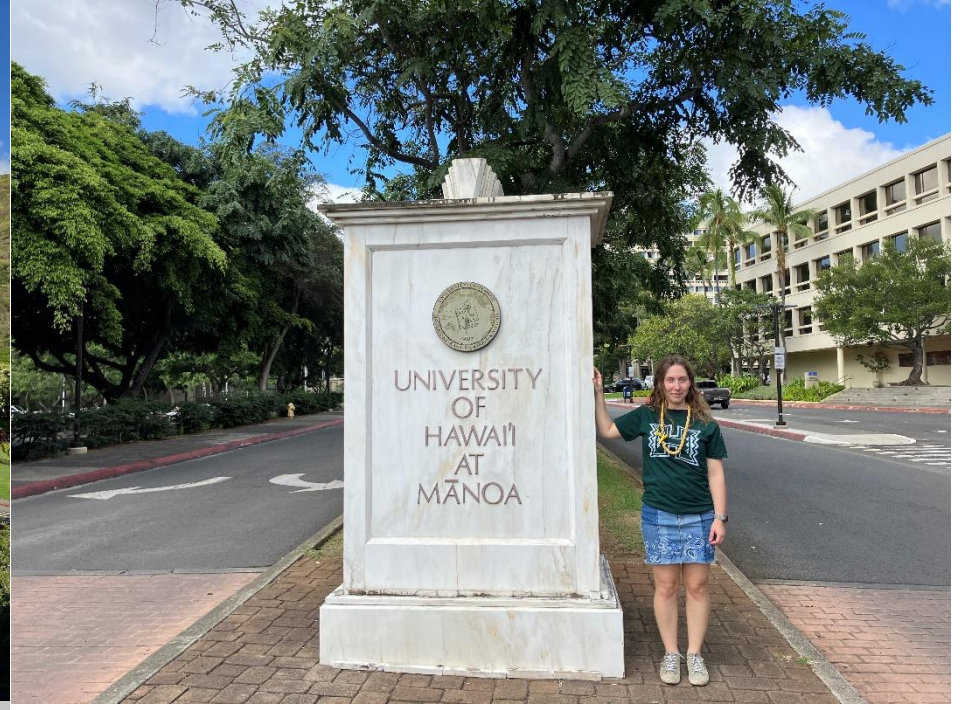


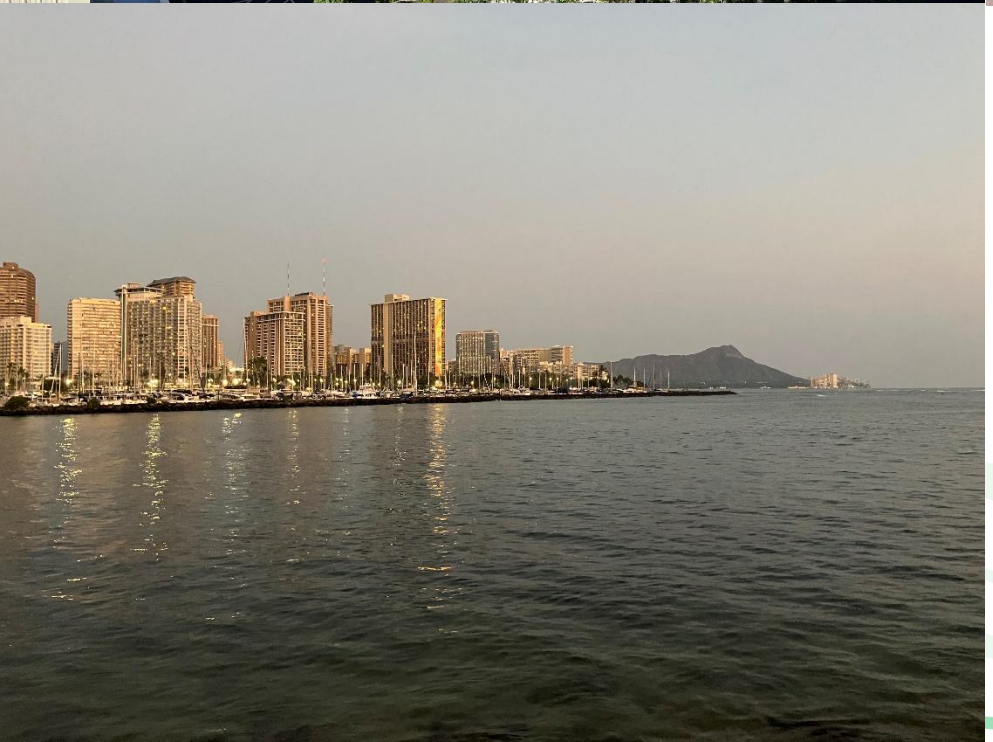
RT-ITO back contact











Thank you!
Mahalo!