Development and Characterization of Power, Bias and Slow-Control Management ASIC for the ePIC Silicon Vertex Tracker

Shirsendu Nanda (LBNL)

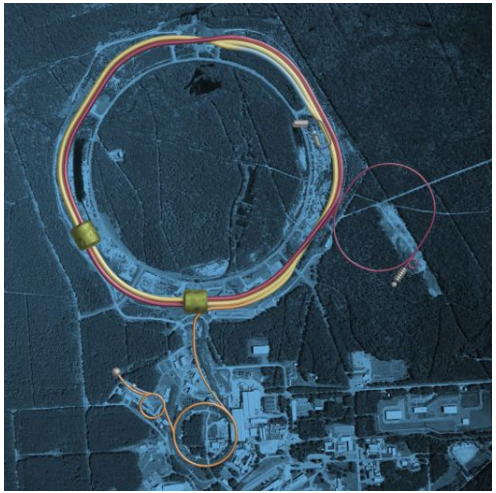
On the behalf of ePIC Collaboration



CPAD 2026
Seattle, WA

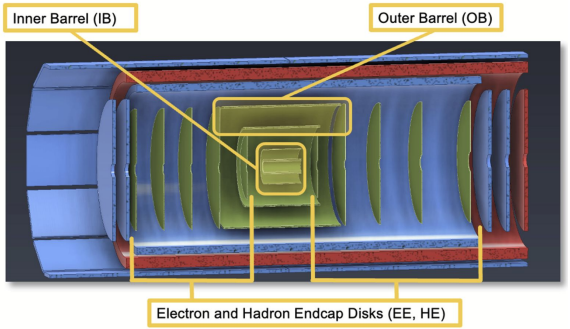
Introduction

EIC, ePIC and MOSAIX





- EIC is currently under construction at BNL
- First beams expected ~ 2037
- Detector is called the electron-Proton/Ion Collider (ePIC). The innermost tracker is called the Silicon Vertex Tracker (SVT).
- SVT plans to use MOSAIX for IB, and EIC-Large Area Sensor for OB and Disks. EIC-LAS will be modified from MOSAIX:

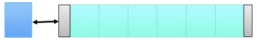


Inner Barrel



Thinned silicon bent around beampipe
Use wafer-scale MOSAIX from ITS3

Outer Barrel and Discs



Smaller version of MOSAIX, EIC-LAS
Supporting AncASIC

➔ Reduce number of RSUs from 12 to 5-6

➔ Reduce number of high-speed data links from 8 to 1

➔ Reduce the clock frequency and high-speed data rate by ≥2x

Introduction

AncASIC Overview

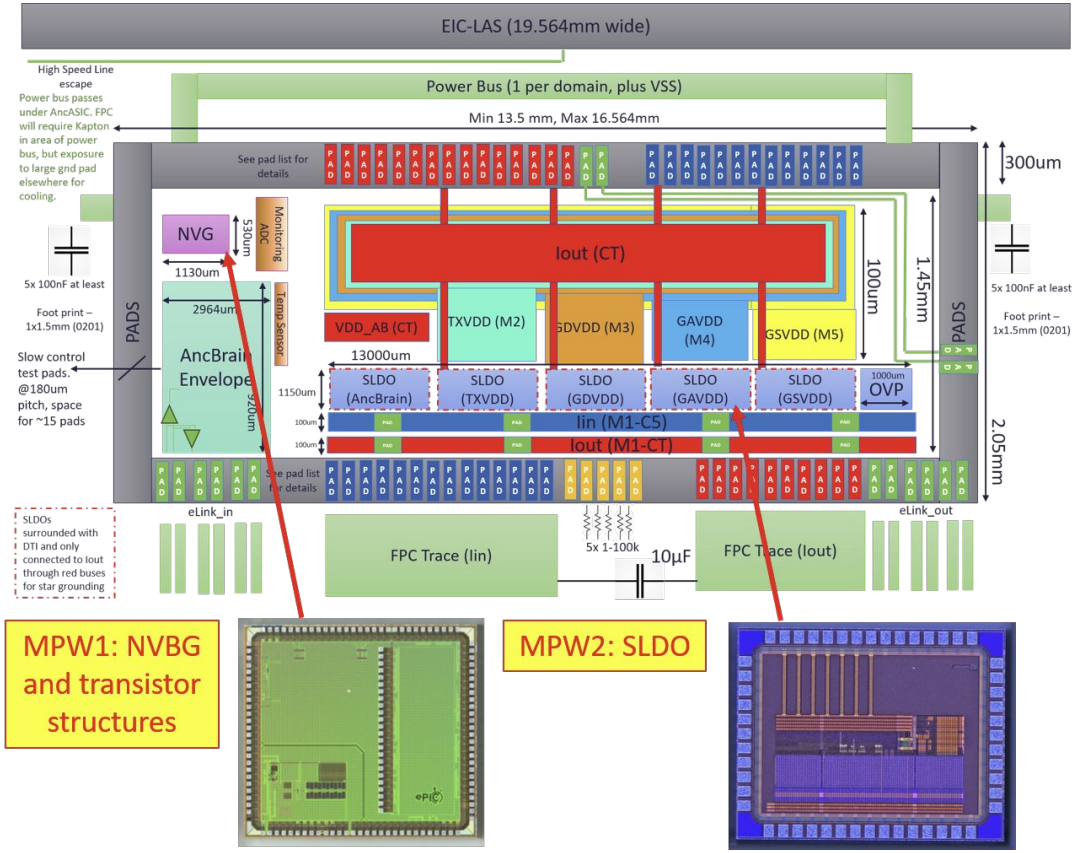
- Provides features required to adapt to stave operation:

➔ **Negative bias generation:** frequency-controlled charge pumps

➔ **Shunt-LDO:** serial power with direct current through multiple AncASICs

➔ **Slow control (AncBrain):** Daisy-chained connection among multiple AncASICs to reduce the number of traces/cables

- 110nm PD-SOI process

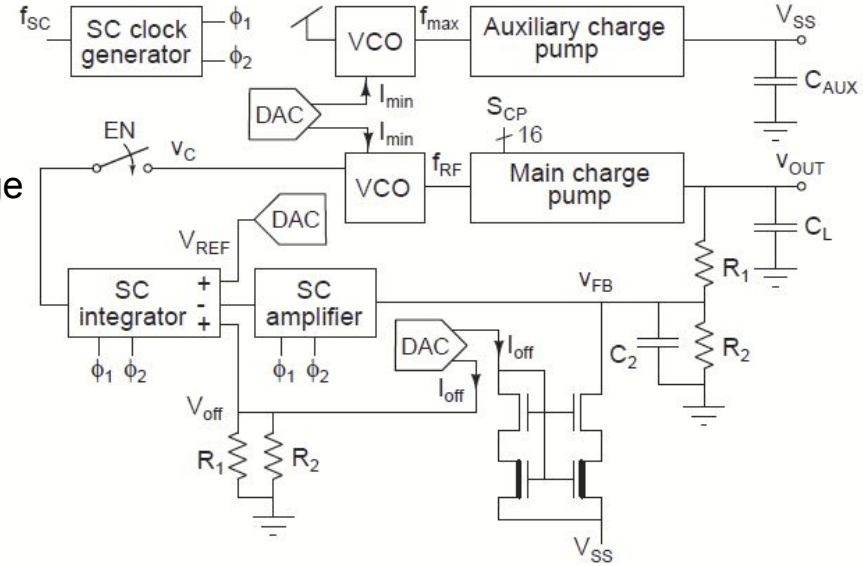


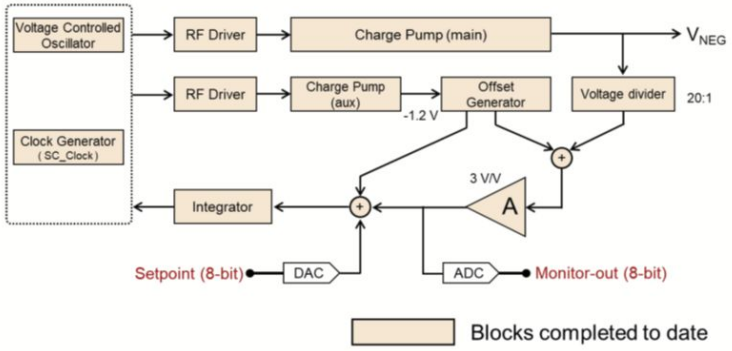
MPW1: NVBG

DOI:10.1109/MWSCAS53549.2025.11244383

Circuit Overview

- Dickson charge pump for on-chip negative-voltage generation
- Clock-driven switched-capacitor architecture
- Programmable negative output ~ (-20/3)VREF for sensor back-bias





Programmable control parameters

Parameter	Description
Iinteg	bias current for the SC integrator
Ivco	bias current for the VCO
Ioff	bias current for the offset generator
EN_{CP}	enable branches of the main charge pump and RF driver
EN<2>	selects VCO control voltage (Vc) - 0 = external control voltage **Open loop** - 1 = output of the SC integrator **Closed loop**
EN<1>	Enable RF clock for main charge pump
EN<0>	Enable RF clock for aux. charge pump

MPW1: NVBG

Specifications

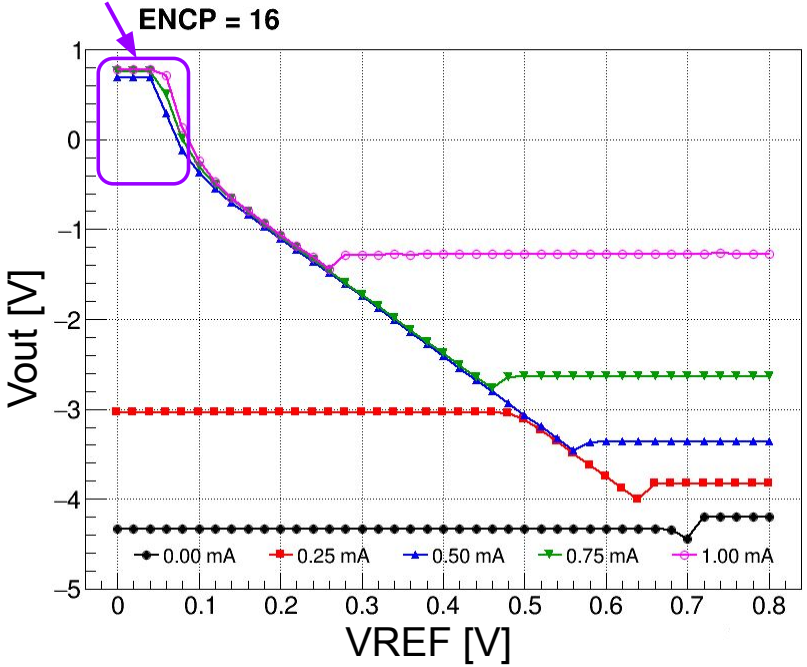
- Specifications driven by the MOSAIX, extrapolated to EIC-LAS back-bias requirements
- Wide programmable negative-voltage range to accommodate different sensor operating conditions
- Parallel charge-pump architecture to scale the available output current
- Designed for low-ripple, low-power operation to minimize impact on sensor performance

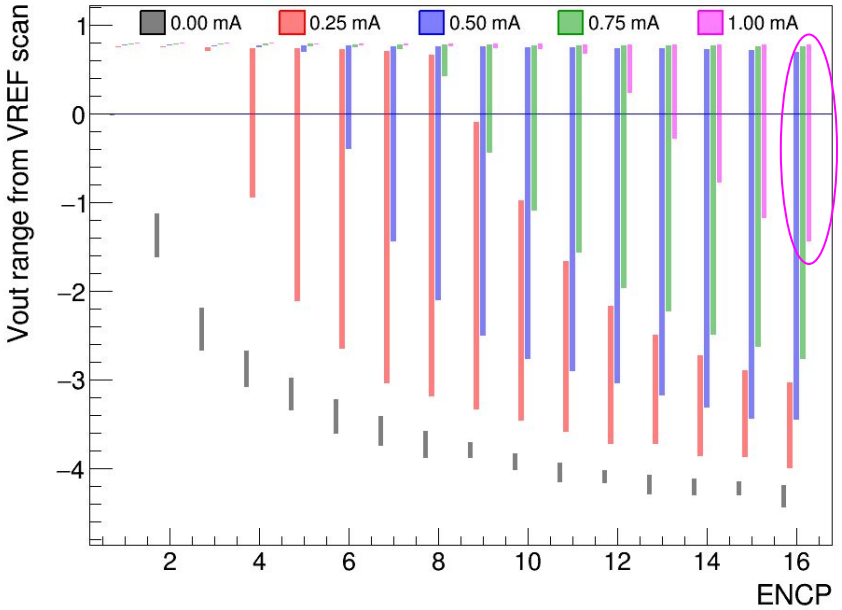
Parameter	Value reported in the draft
Supply	1.2 V ±10% (provided by 1st SLDO)
Output range	<−1 up to −5 V relative to local ground
Reference DAC	8 bit for V_{ref}
Output-current capability	≈1 mA / section (6 sections: 1 Main + 5 Auxiliary) ; ≈200 µA nominal reference load/section
Output ripple	<0.15 mV; simulated
Power consumption	<15 mW; ≈11 mW at −1.5 V
Main charge pump	16 selectable parallel branches / section

MPW1: NVBG

VOUT - VREF dependence and VOUT range

Vout becomes positive and clamped to < ~1 V by ESD diodes

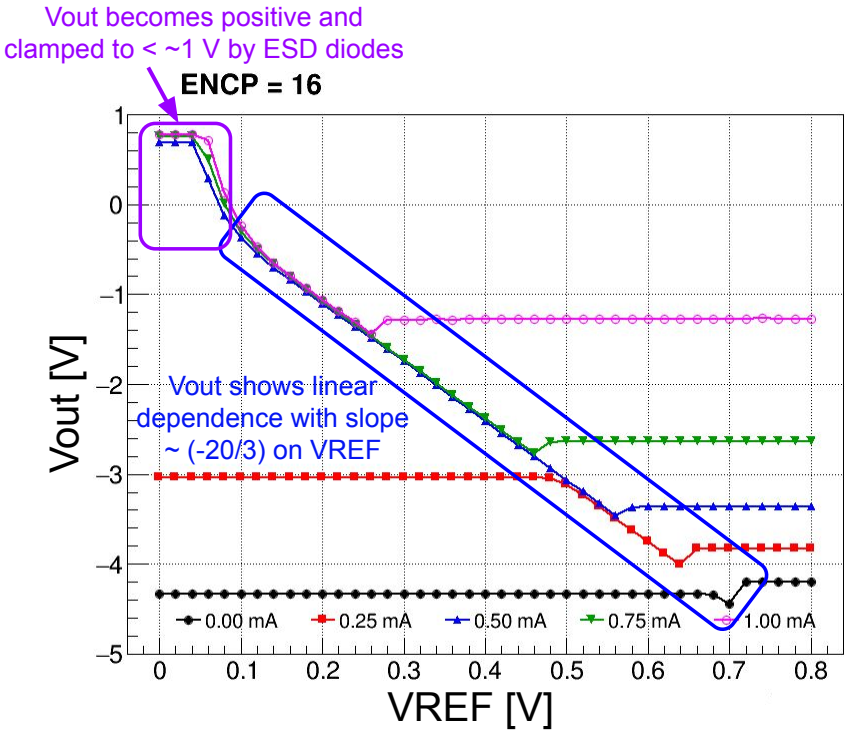


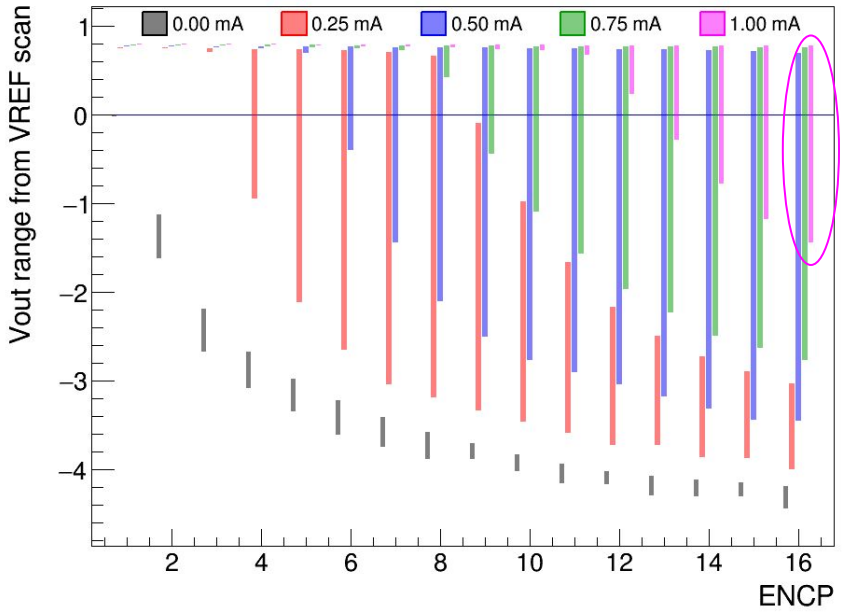


- Vout range from VREF (0 - 0.8V) scan for each ENCP (different load currents)
- **With 1 mA current load, for highest ENCP, Vout reach ~ -1.5 V**

MPW1: NVBG

VOUT - VREF dependence and VOUT range

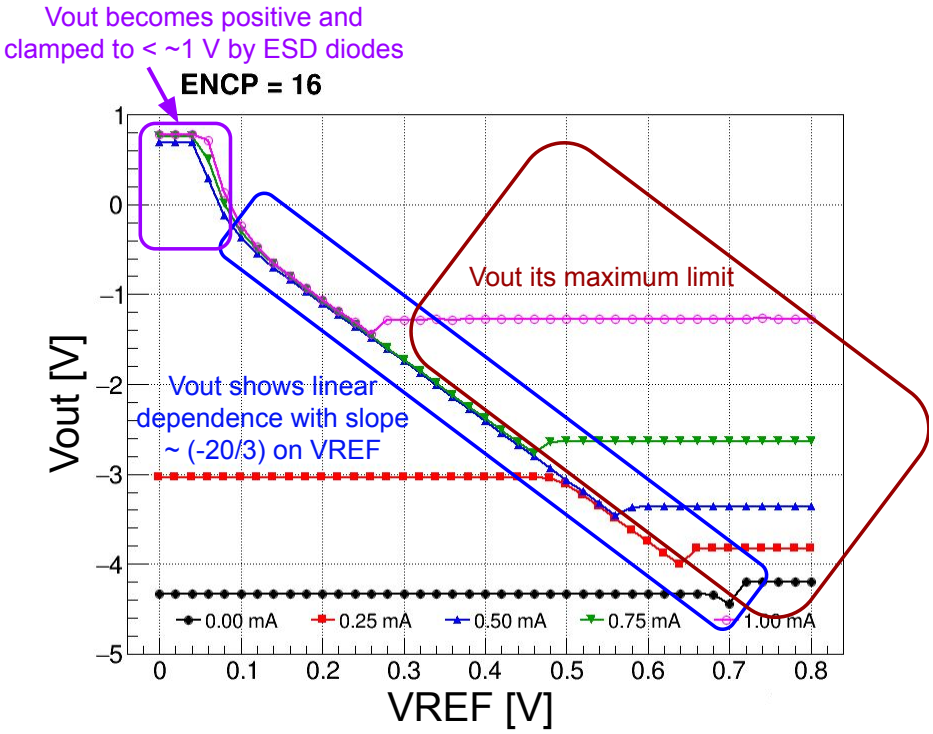


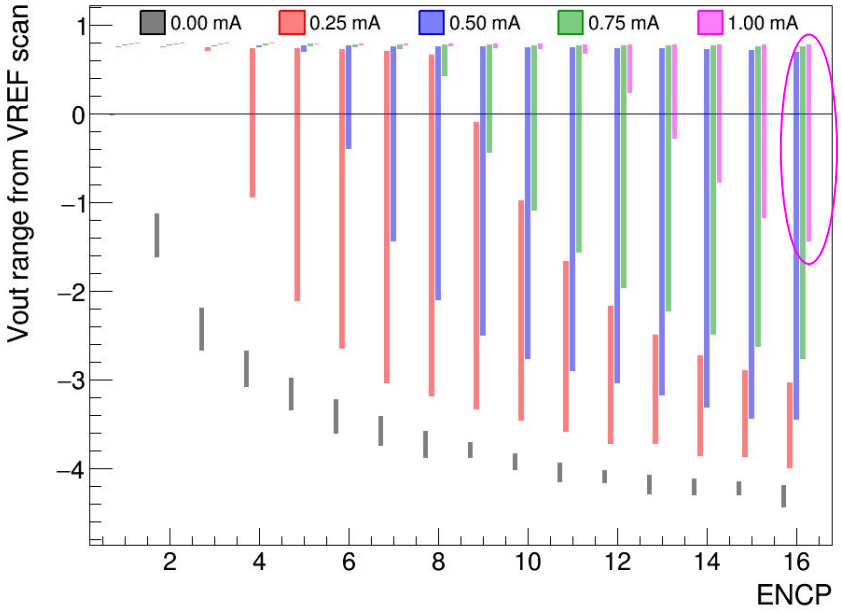


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MPW1: NVBG

VOUT - VREF dependence and VOUT range



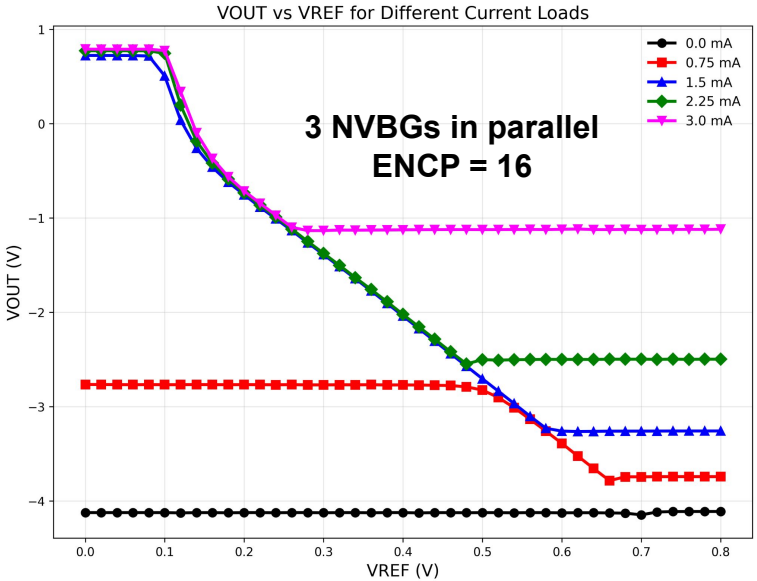


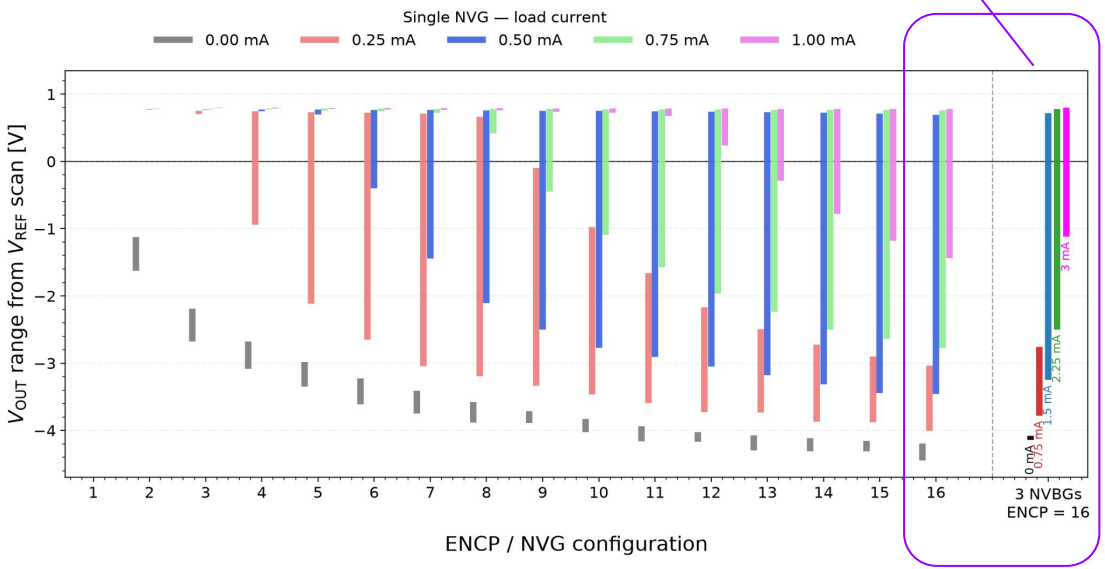
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MPW1: NVBG

VOUT - VREF dependence and VOUT range

1 Closed-loop and 2 opened loop NVBGs in parallel



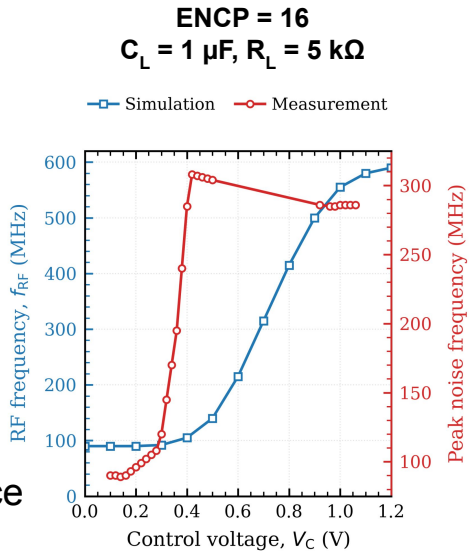


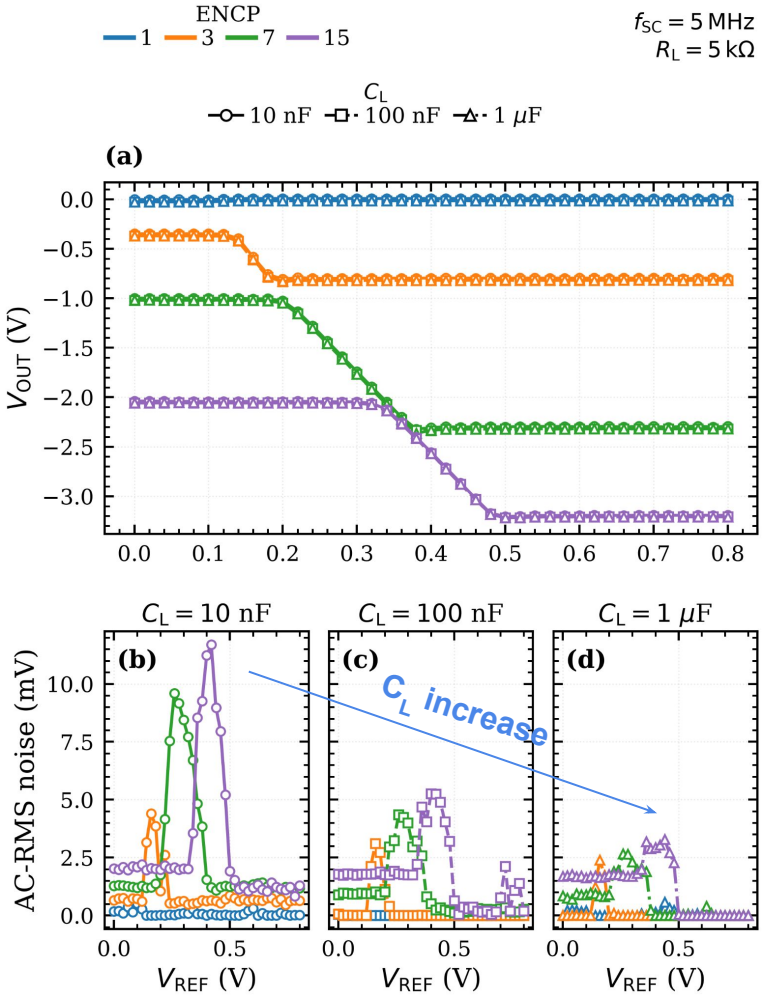
- Parallel operation of three NVBGs extends the load-current capability by 3X while maintaining a VOUT range comparable to a single NVBG
- 6 NVBGs in parallel are implemented in the new chip submission to support up to ~6 mA of load current

MPW1: NVBG

Noise

- VOUT independent of C_L but varies with ENCP
- NVBG Noise ENCP and C_L dependent
- ~ 2-3 mV for C_L = 1 uF
- Peak noise frequency follows the simulated trend, reaching ~300 MHz in measurements
- Confirms the on-chip VCO as the dominant NVG noise source





MPW2: SLDO

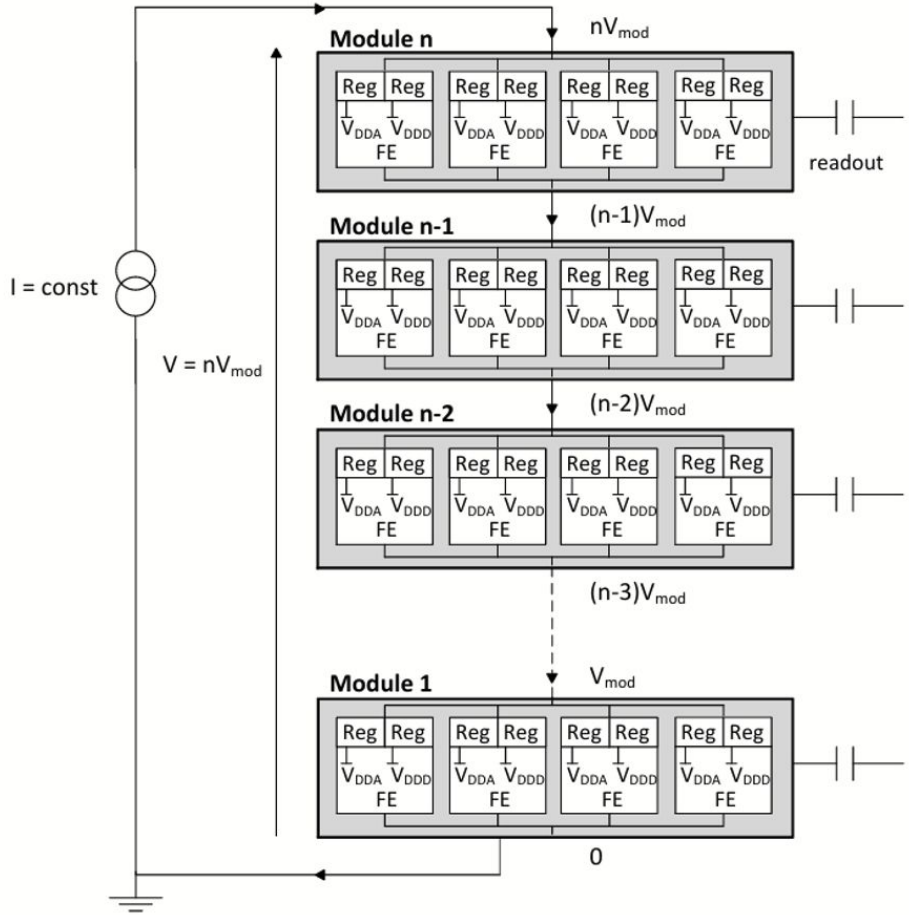
Serial Powering

- Goal is to reduce cable requirements by routing the same current through multiple regulators in series
- Requires a circuit that:

➔ Can shunt current to the next stage

➔ Can regulate the output voltage

➔ Can be parallised in case of multiple sensor domains i.e. has a resistive characteristic



MPW2: SLDO

LDO Loop:

➔ Regulates and stabilizes the output voltage

Shunt Loop and reference stabilization:

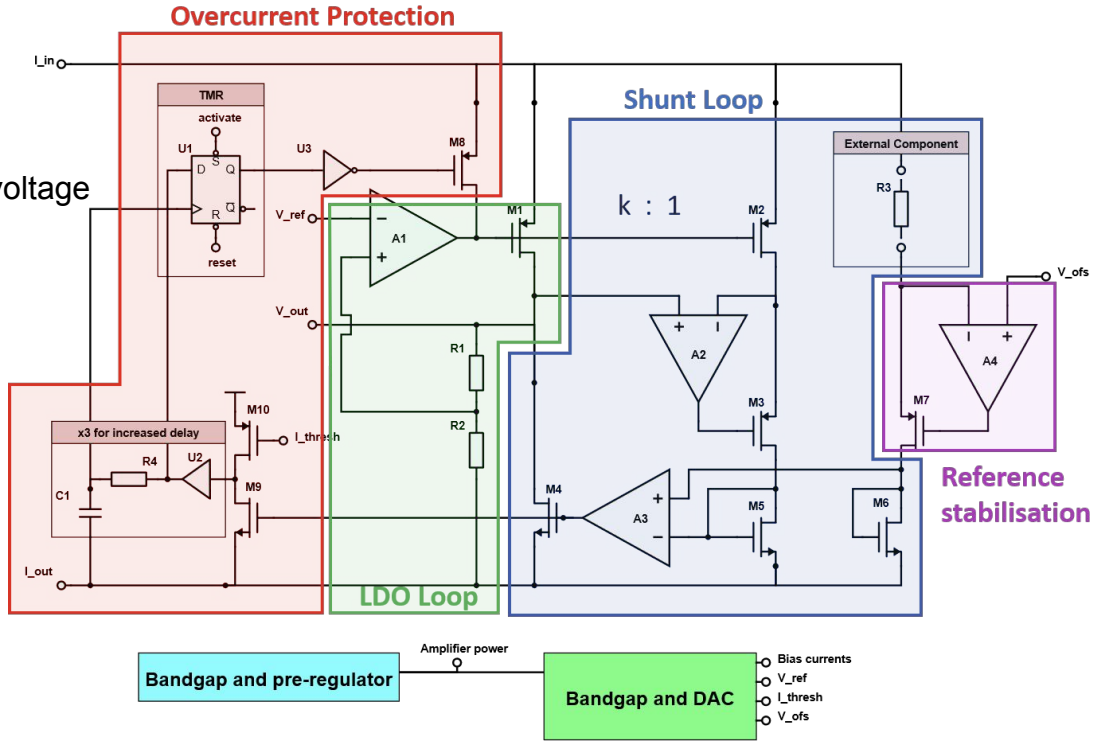
➔ Maintains stable shunt operation and reference voltage

Overcurrent protection:

➔ Protects against excessive load current

Circuit Features

- Overcurrent protection – triggers when shunt current drops below 10mA
- Tri-state output can also be used for power sequencing
- Also DAC to control output voltage



$$I_{in} = k\frac{V_{in} - V_{offset}}{R3} \qquad R_{eq} \approx \frac{R3}{k}$$

MPW2: SLDO

Specifications

- Current specifications driven by expected EIC-LAS consumption based on published MOSAIX data
- Temperature range significantly exceeds expected ePIC temperatures
- SLDO to cover the large current range. Area inefficient, some performance degradation

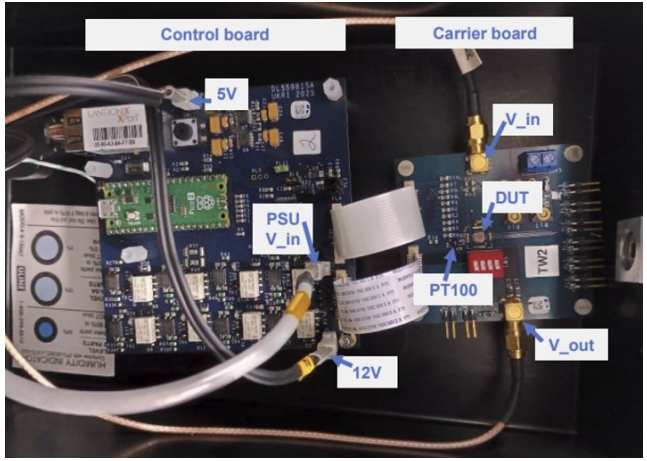
Specification	Unit	Value
Temperature	Degrees Celsius	-20 to 105
Voltage Range	V	1.0 – 1.4
Current capacity	mA	0.04 - 900
Load Capacitance	F	10n – 10u
Shunt current overhead	%	10
Shunt power	% of load power	<35
Total Ionising Dose	Rad	< 1M
Neutron Flux	n_{eq}/cm^2	10e12
Additional features		• Tri-state output • Over-current protection

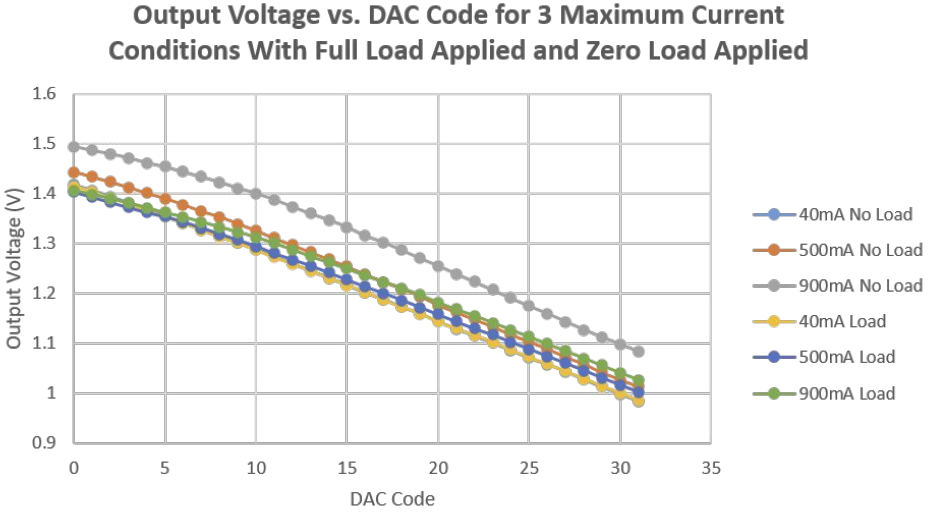
MPW2: SLDO

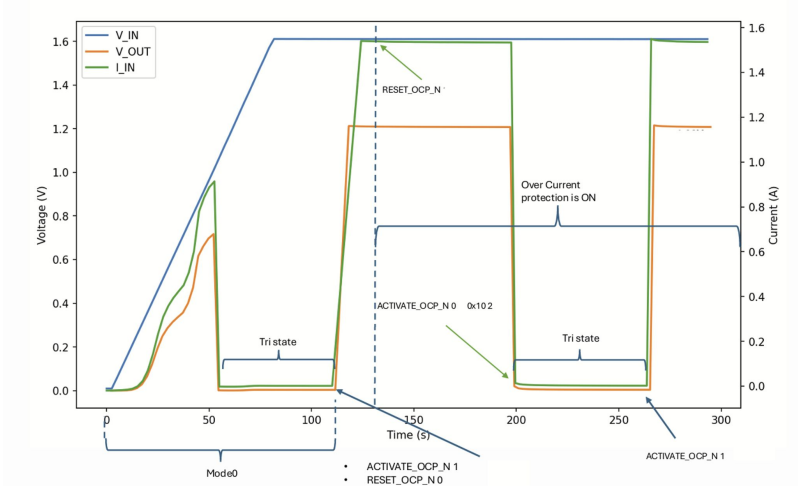
Device Testing

- Fully functional over full range of load currents and shunt conditions. -20 and 27 degrees, all load caps.

- Tri-state output functionality has been verified



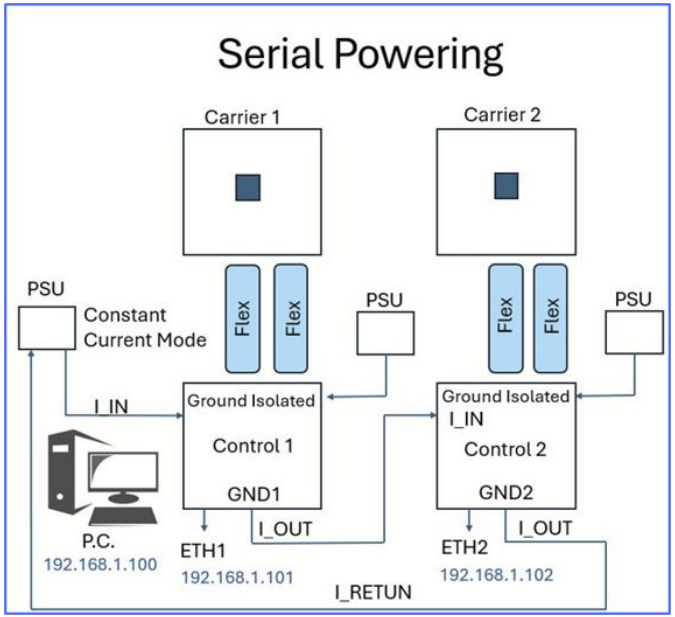


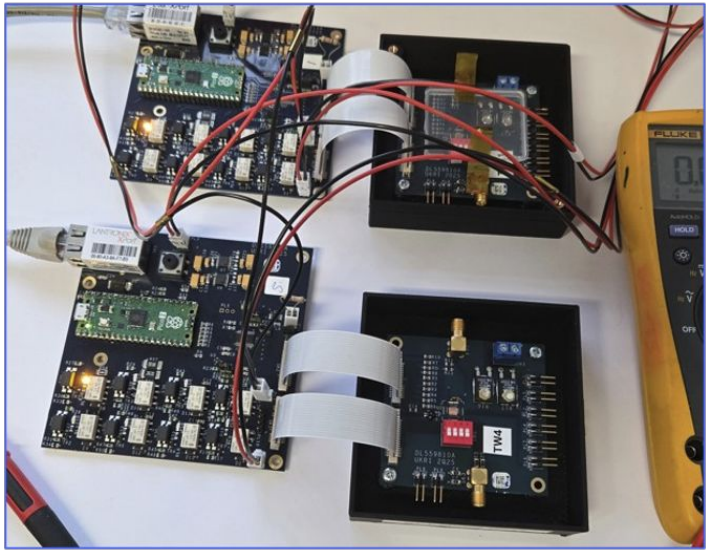


MPW2: SLDO

Serial Powering Chain Testing

First serial powering chain constructed





PSU V_OUT 3.2V 0.06A CC Mode
Board 1 V_IN =1.556V
Board 2 V_IN = 1.641V
Overall V_Drop = 0.003V

No Load test::-
Board 1 Dac set to 0 ∴ V_out = 1.416V
Board 2 Dac set to 0 ∴ V_out = 1.479V
PSU V_out = 3.2V 0.06A CC Mode

Board 1 Dac set to 31 ∴ V_out = 0.984V
Board 2 Dac set to 31 ∴ V_out = 1.055V
PSU V_out = 3.2V 0.06A CC Mode

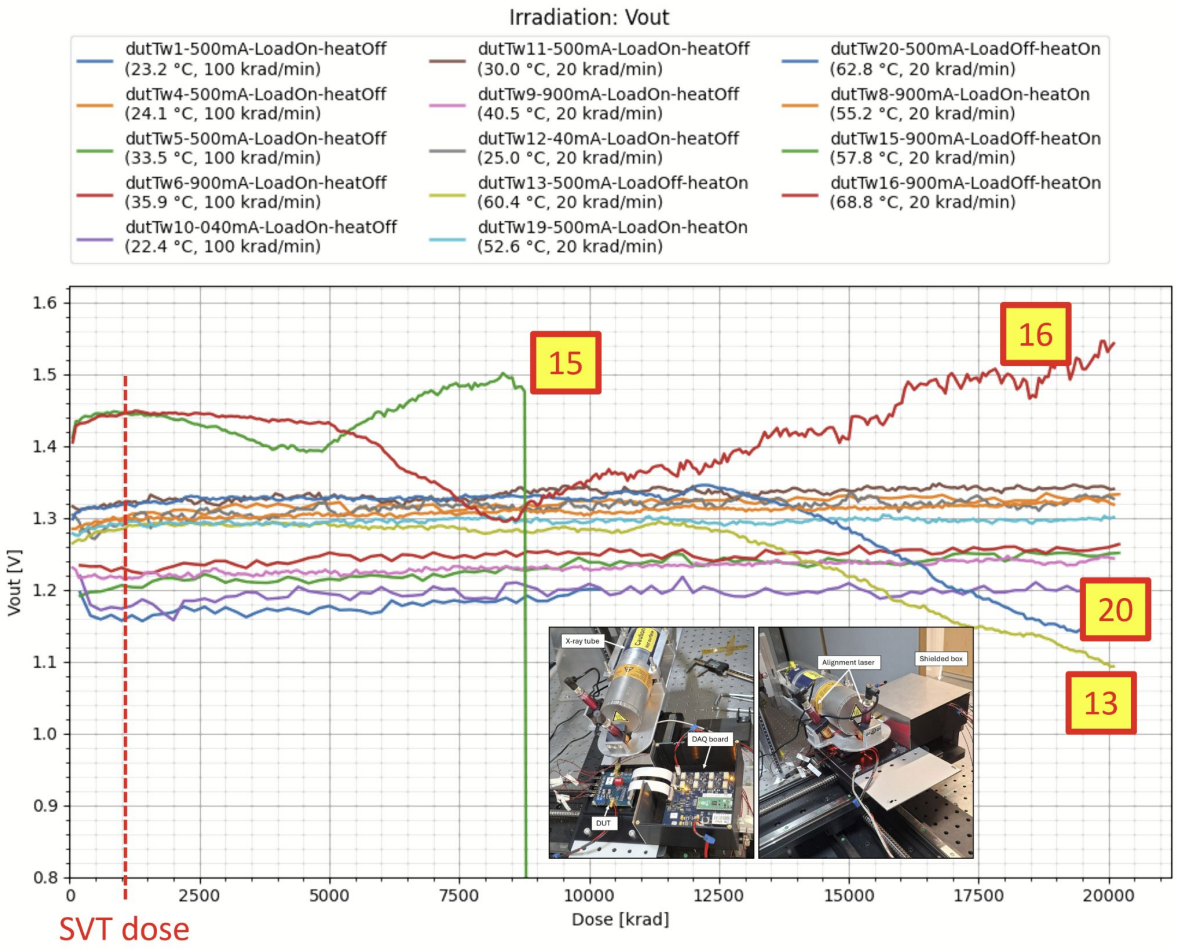
With Load test:-
Board 1 Dac set to 0 ∴ V_out = 1.414V
Board 2 Dac set to 0 ∴ V_out = 1.478V
PSU V_out = 3.2V 0.06A CC Mode

Board 1 Dac set to 31 ∴ V_out = 0.985 V
Board 2 Dac set to 31 ∴ V_out = 1.058V
PSU V_out = 3.2V 0.06A CC Mode

MPW2: SLDO

TID Testing

- Irradiated multiple devices up to 20 MRad (EIC expected dose <1 MRad
- Irradiated under multiple conditions
- High heat, high current with all current shunted shows some failure conditions at multi-Mrad doses
- 4 chips: 13, 15, 16, 20 showed variation with dose, but only at values exceeding the SVT requirements



AncBrain for Slow Control

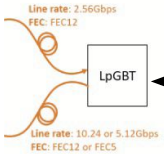
Sub-Module Control:
NVBG and SLDOs

Communication Interfaces:
lpGBT and EIC-LAS

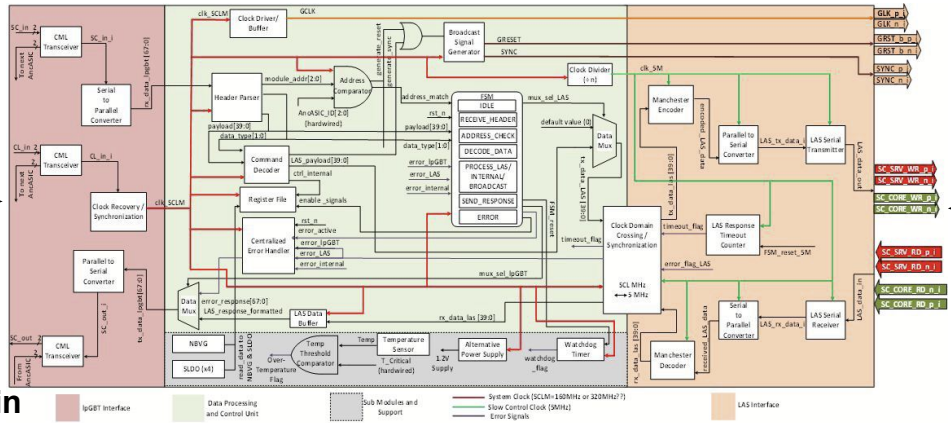
Broadcast Signal Generation:
Broadcast Command Detection, Delay Line Configuration, Register Storage

System Protection:
Error Handling, Watchdog, Temperature

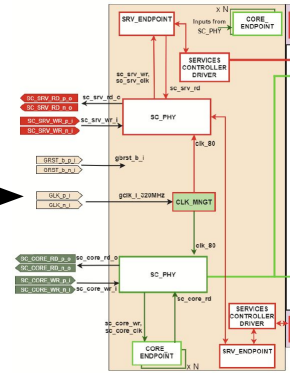
lpGBT Interface

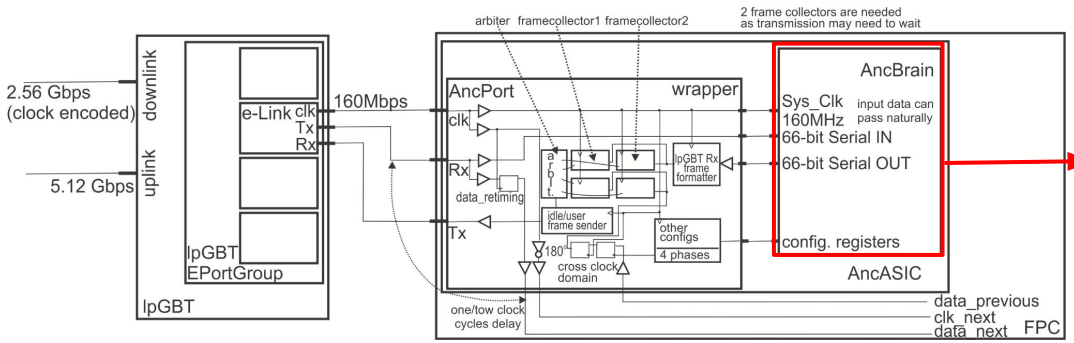


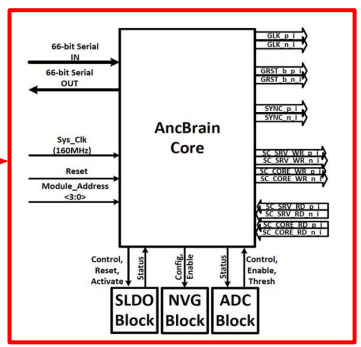
AncBrain Block Diagram



EIC-LAS Interface



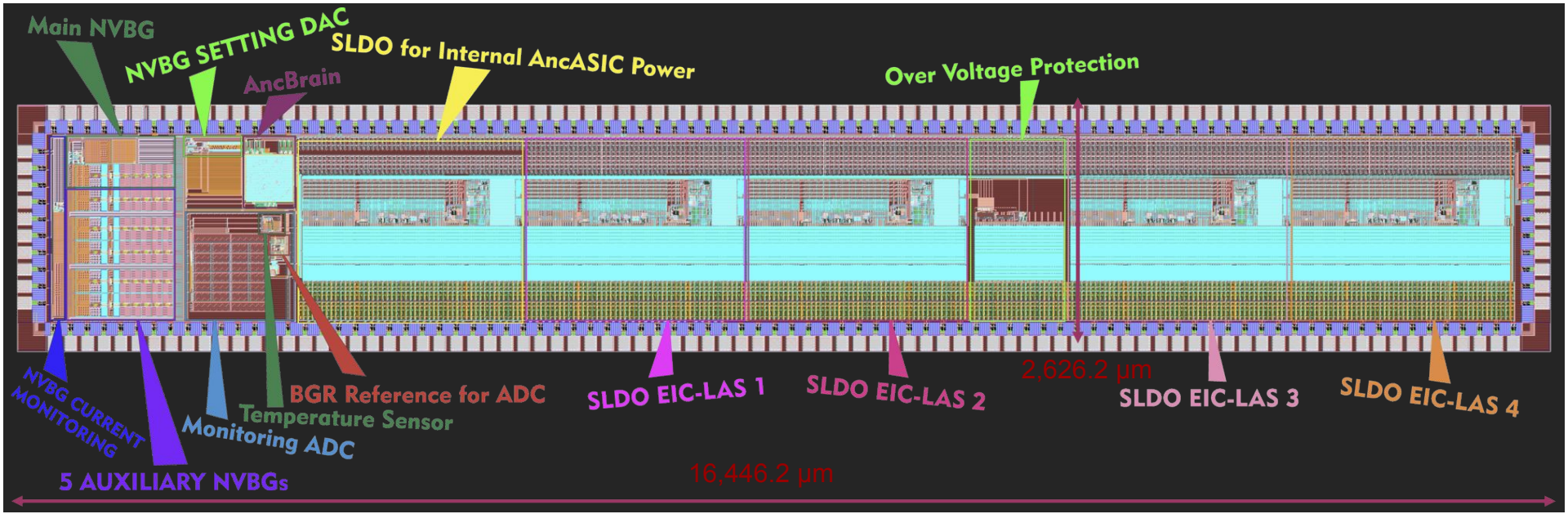




AncBrain is designed to control and monitor the NVBG and SLDOs in the AncASIC, and to provide a slow control hub for the EIC-LAS. AncBrain is included in the AncASIC MPW3 submission.

MPW3: NVBG + Shunt-LDO + AncBrain for Slow Control

- ➔ 5 SLDOs are included in the AncASIC MPW3 submission
- ➔ 6 NVBG design to increase the supply current limit up to 6mA@-1.2V is included in AncASIC MPW3
- ➔ AncBrain is included in the AncASIC MPW3
- ➔ MPW3 submission in September 2026; expected delivery mid-February 2027



Summary and Future Work

Summary

- Presented results for Negative Voltage Bias Generator and Shunt-LDO in a 110nm SOI process
- The functions and characteristics of the NVBG have been extensively tested, and the test results match close to the design expectation.
- A SLDO was included in MPW2 submission and underwent extensive tests, e.g. temperature and total irradiation dose measurements.
- MPW3 submitted in September 2026, expected to delivery mid-February 2027

Future Work

➔ Starting preparation for characterization for MPW3