Oct 22nd 2026

NIFTY
Project Overview
CPAD @ UW 2026

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Xiangyang Ju, Paul Keener, Yuan Mei, Alexis Mulski, Adrian Nikolica,
Nirmalendu Patra, Maurice Garcia-Sciveres, John Shalf

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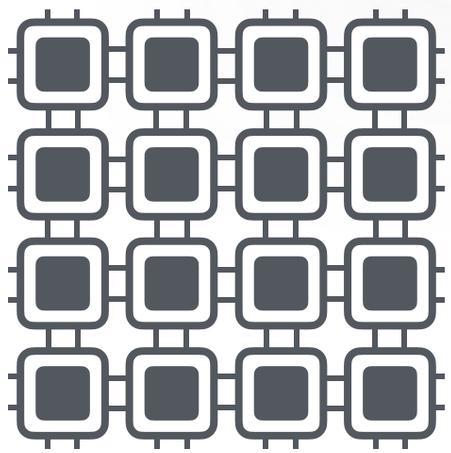
A **nifty** idea…

Over the past few days we've heard talks about innovations in a variety of detector technologies for HEP.
Single point failures continue to be a major challenge.
What if we could make detector instrumentation all a little bit.. niftier?

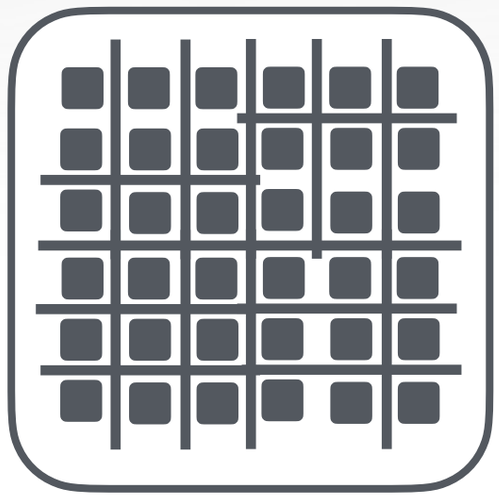
NIFTY is a collection of ideas to make readout fault tolerant using intelligent routing:

Network **I**ntelligence **F**ault **T**olerance is **NI**FTY

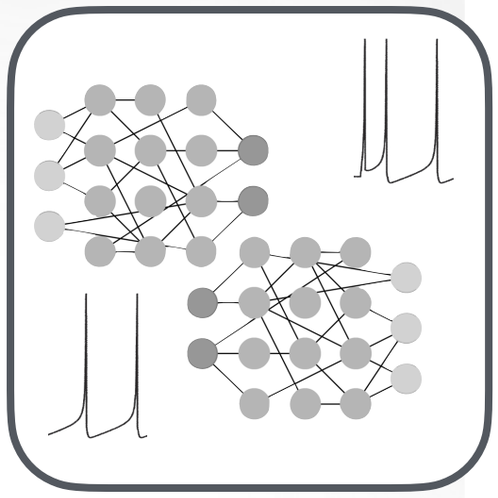
The NIFTY project develops network architectures with built-in intelligence to make detectors tolerant to single-point failures while facilitating load balancing to optimize readout bandwidth. We do this across several branches:



Network off-chip
LArPix vN1



Network on-chip
PixCanvas



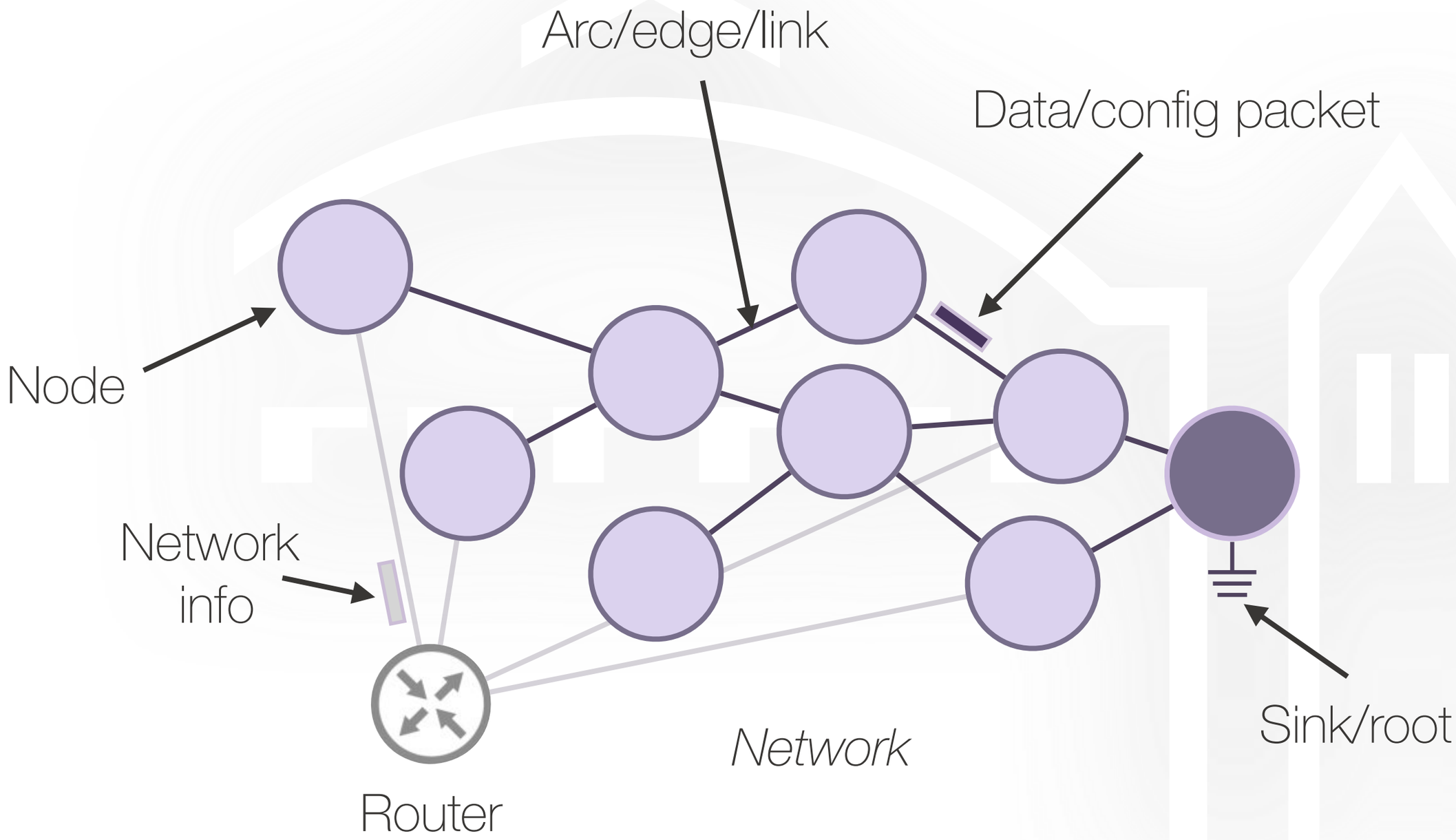
Neuromorphic
NIFTY



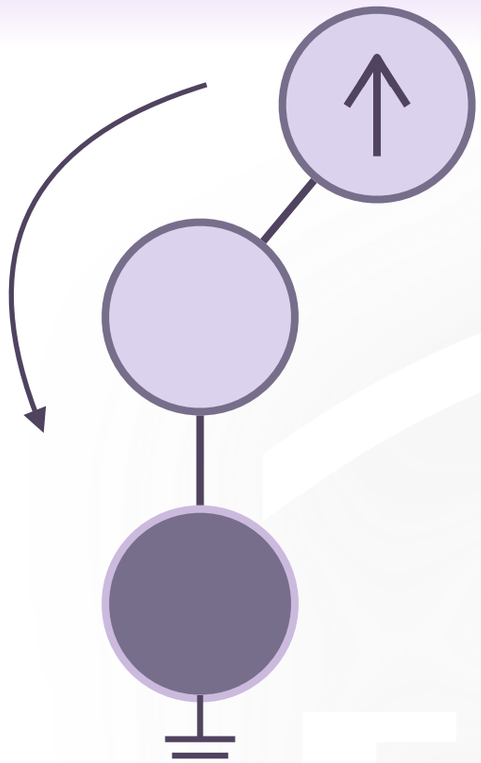
3D mesh for
SmartDust

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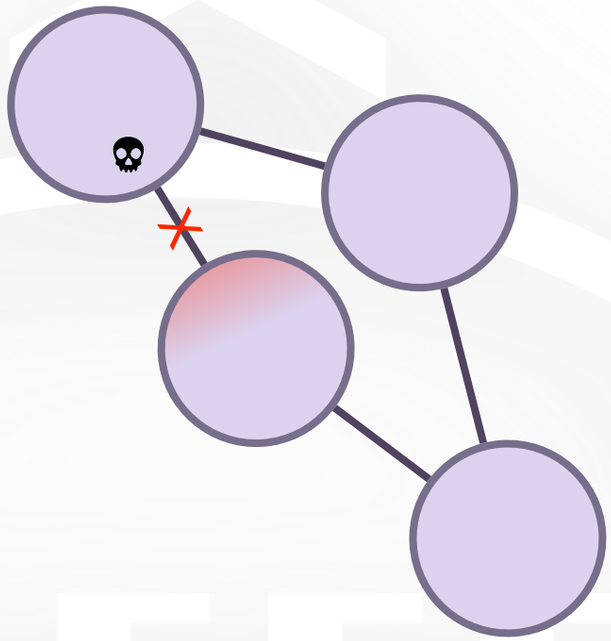
Common **terms**



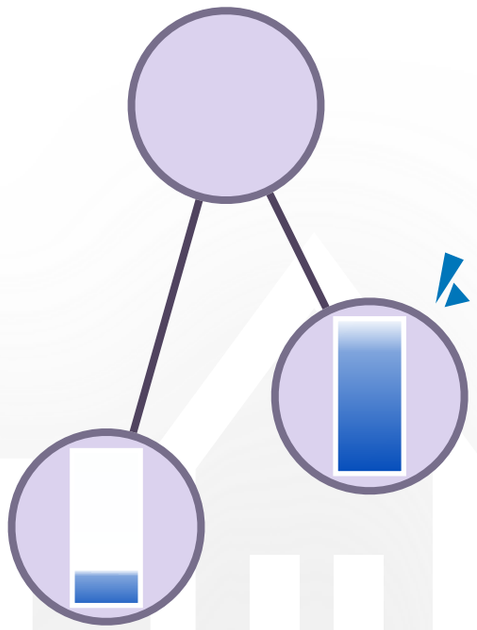
Common **concepts**



Data ultimately flows towards root node ∴ router need a sense of where nodes are wrt root.



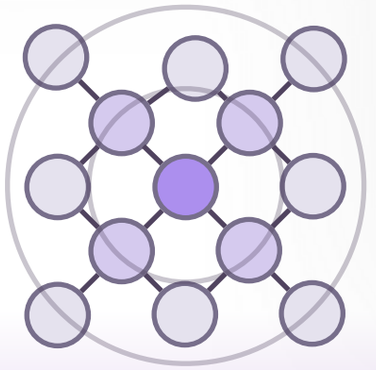
Network adapts to failures ∴ router needs to be aware of node's health.



If a node can buffer data, want to make sure we're not routing to one that is filled ∴ router needs to be aware of node's storage capacity.



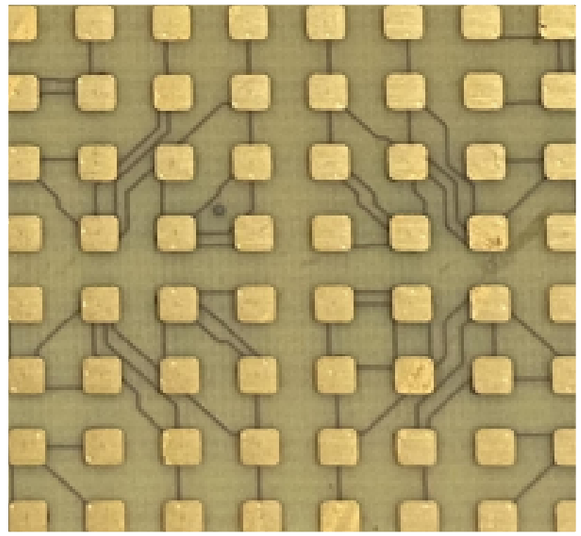
Where is the router? How is info communicated to/from the router?



What is the sphere of influence on a given node's routing decision? Nearest Neighbor? Next-to-NN? Global?

Off-chip networks: **LArPix**

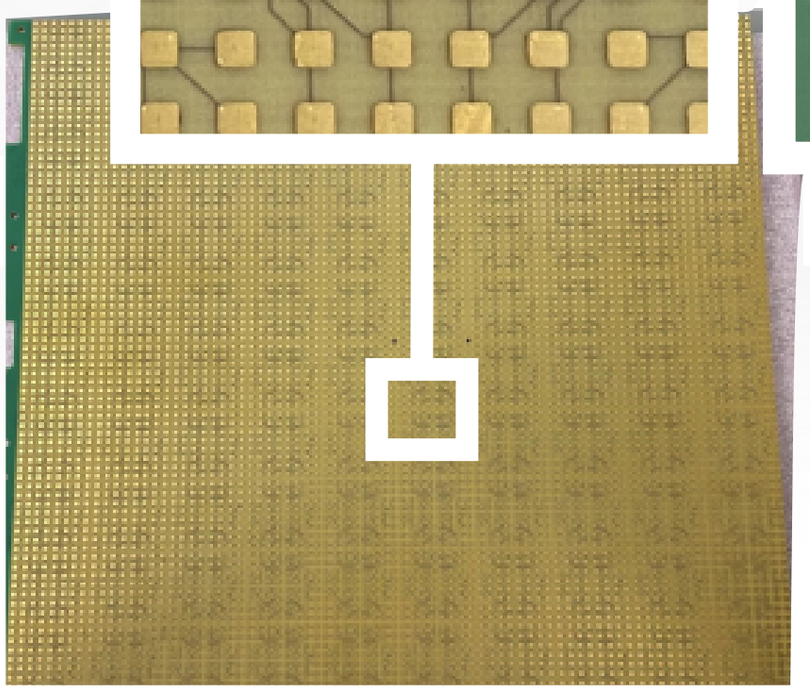
Pixelated electrodes

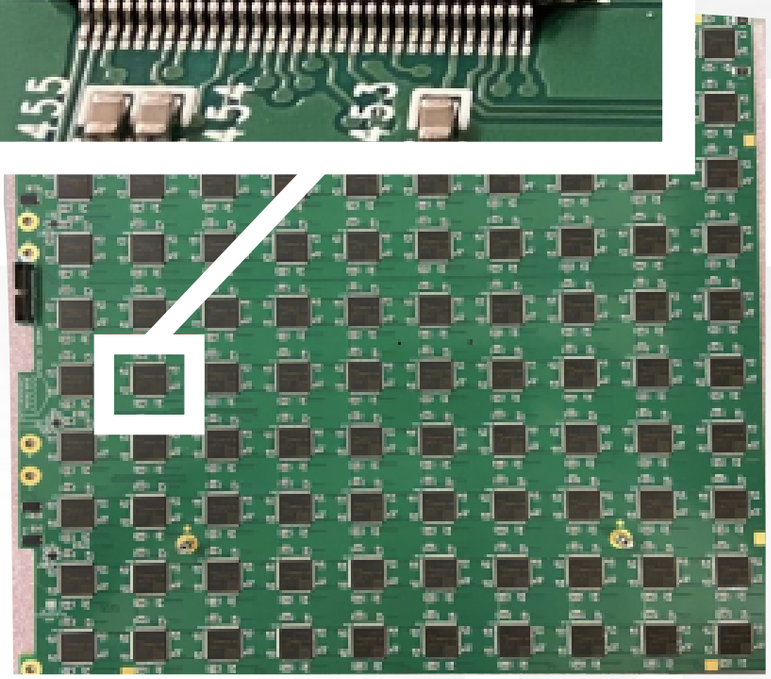


LArPix chip



Tile front



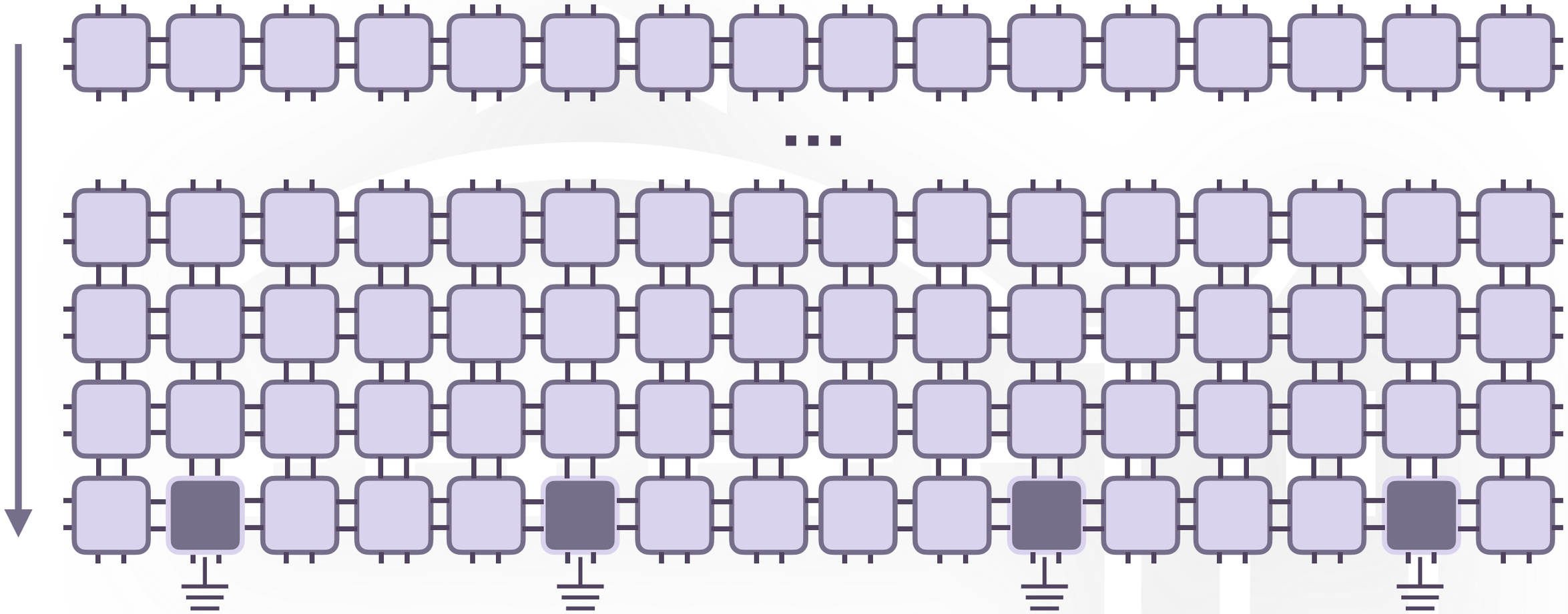


Tile back

Since we just heard about DUNE's LArPix from Dan Dwyer, let's start with an off-chip network.

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Off-chip networks: **LArPix**

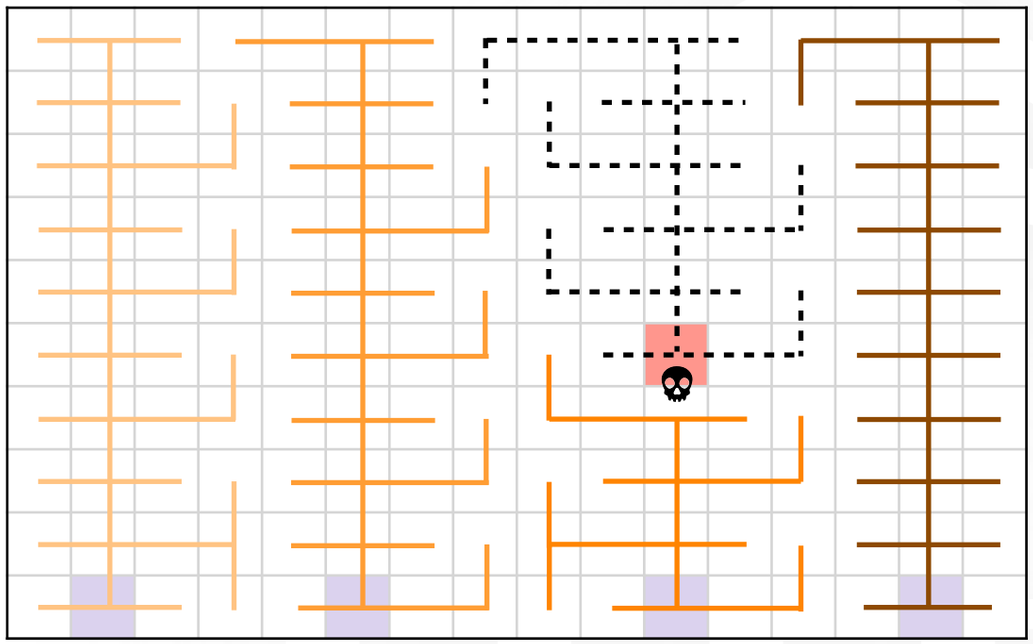


Network fact sheet

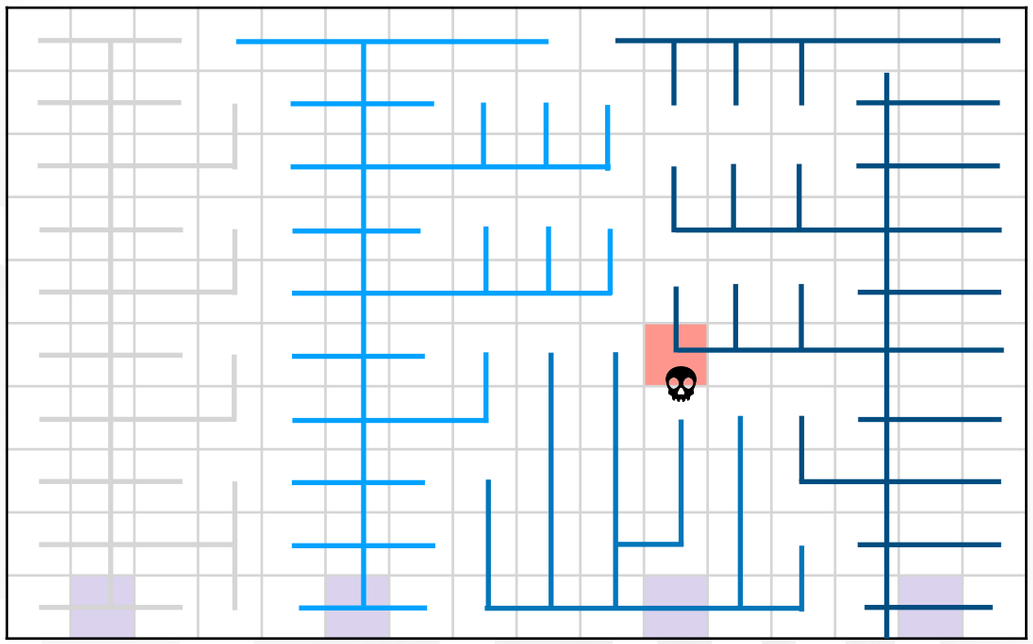
Name: DUNE Tile
Type: 2D mesh, 10 x 16 nodes.
Root nodes: 4, all at base of tile
Arcs/node: 4 tx, 4 rx - serial links

All nodes are data-generating (connected to 64 detector channels).
All nodes can retransmit packets, this includes the root nodes.

Off-chip networks: **HYDRA**



HYDRA 1: “Sawfish” network configuration: with one dead node! Node tx link to closest root is broken.

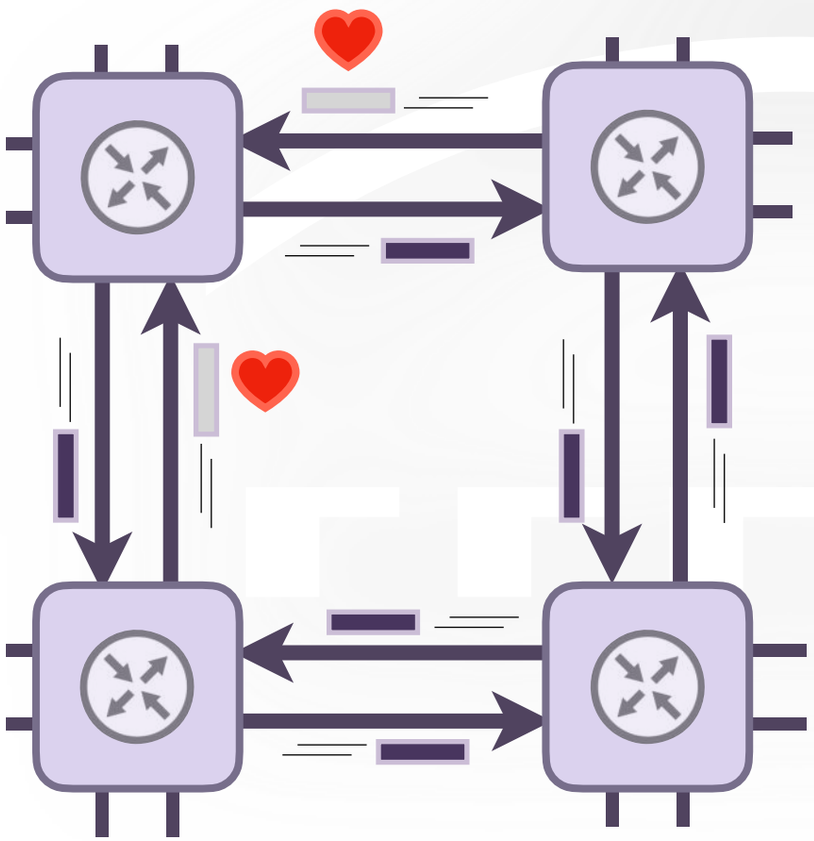


HYDRA 2: Adapted network configuration: other branches route around dead link.

- Network is configured by an off-network router, which communicates with nodes via the roots, hopping from one node to another.
- Network connectivity is static. Large number of messages & hops to alter it.
- Significant latency in both recognizing and responding to failures.



LArPix vN1: A NIFTY remix



Data packet

NIFTY message

1. Instead of an off-network router, have one on each node. Improves ability to respond to failures dynamically.

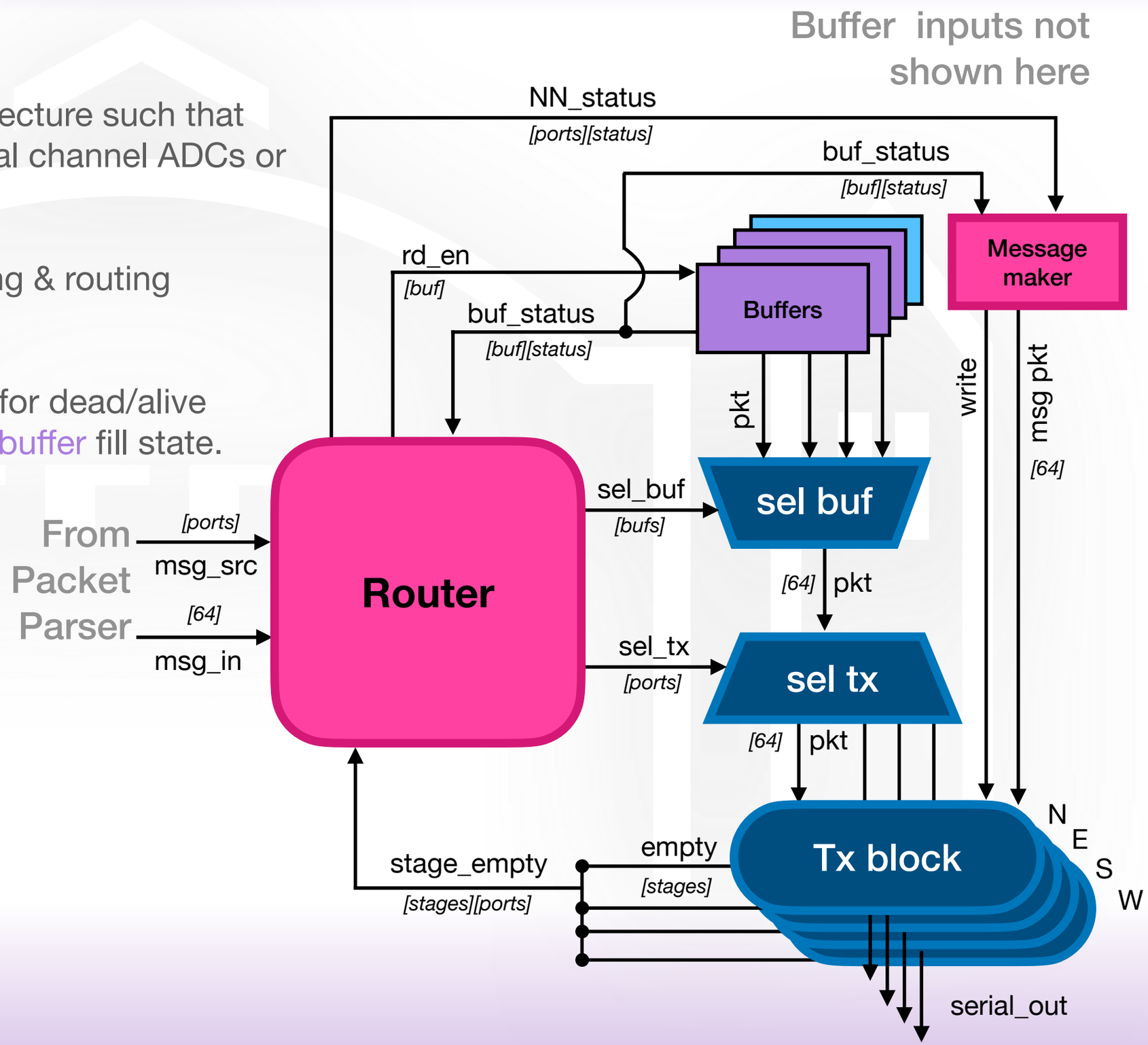
2. To be able to share status e.g. failure, with other nodes: new packet type, the NIFTY message. Takes up some bandwidth because routed over same tx/rx as data.

3. In addition to having some useful content about the state of a node, the messages act as a heartbeat - letting the receiving node know that the sender is still alive in times of sparse data.

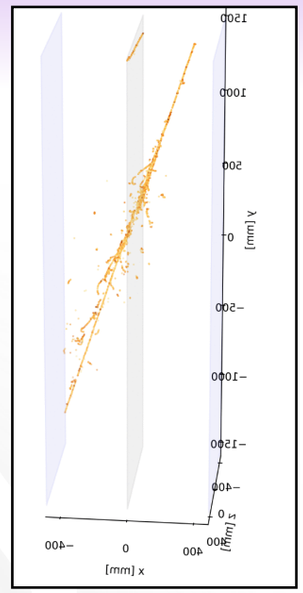
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LArPix vN1: A NIFTY remix

- Redesigned the data flow architecture such that data is pipelined from either local channel ADCs or rx inputs to large global buffers.
- New arch facilitates both fetching & routing packets.
- NIFTY messages used not only for dead/alive status but also to monitor each buffer fill state.
- Two operational modes: HYDRA or NIFTY.
- Backwards compatibility with LArPix v3c means that we can test the chip with the existing DUNE hardware.

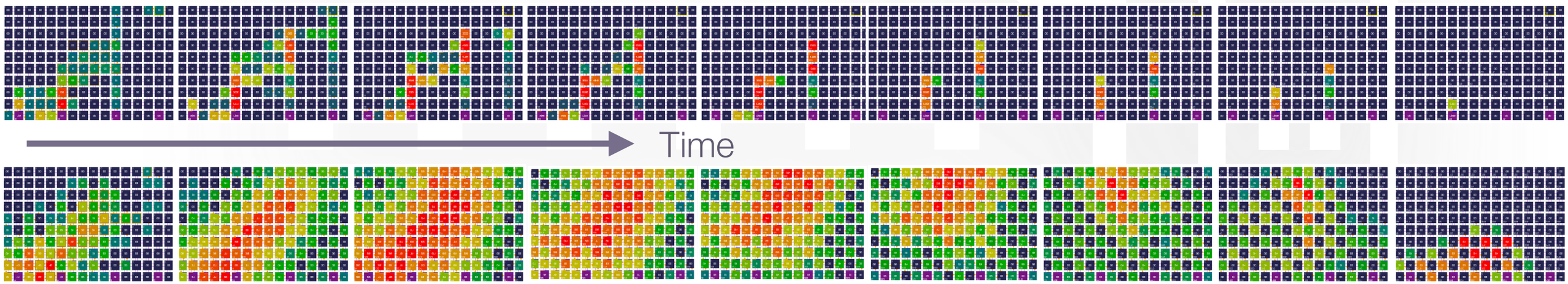


LArPix vN1: Qualifying the **router**



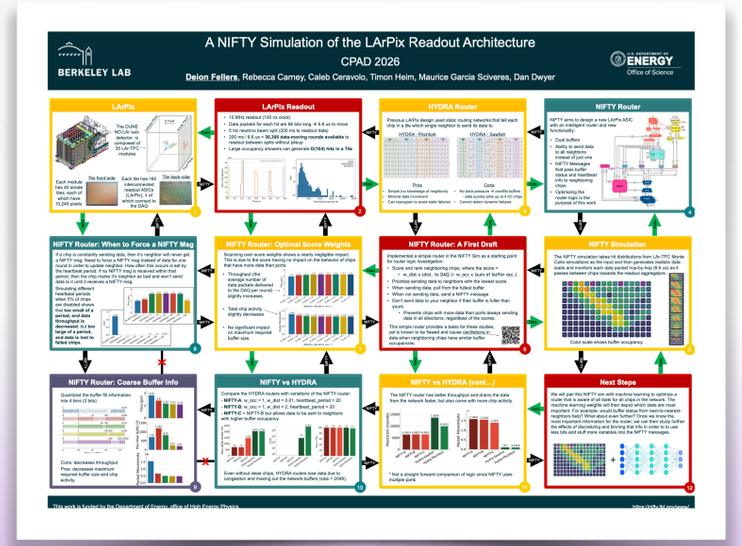
- Data driven exploration of router algorithms using the NIFTY simulation framework.
- Using simulated events from Matt Kramer & Dan Dwyer at Berkeley Lab including more “extreme” cosmic interactions with long tails that stress the network.

HYDRA “Sawfish” network configuration



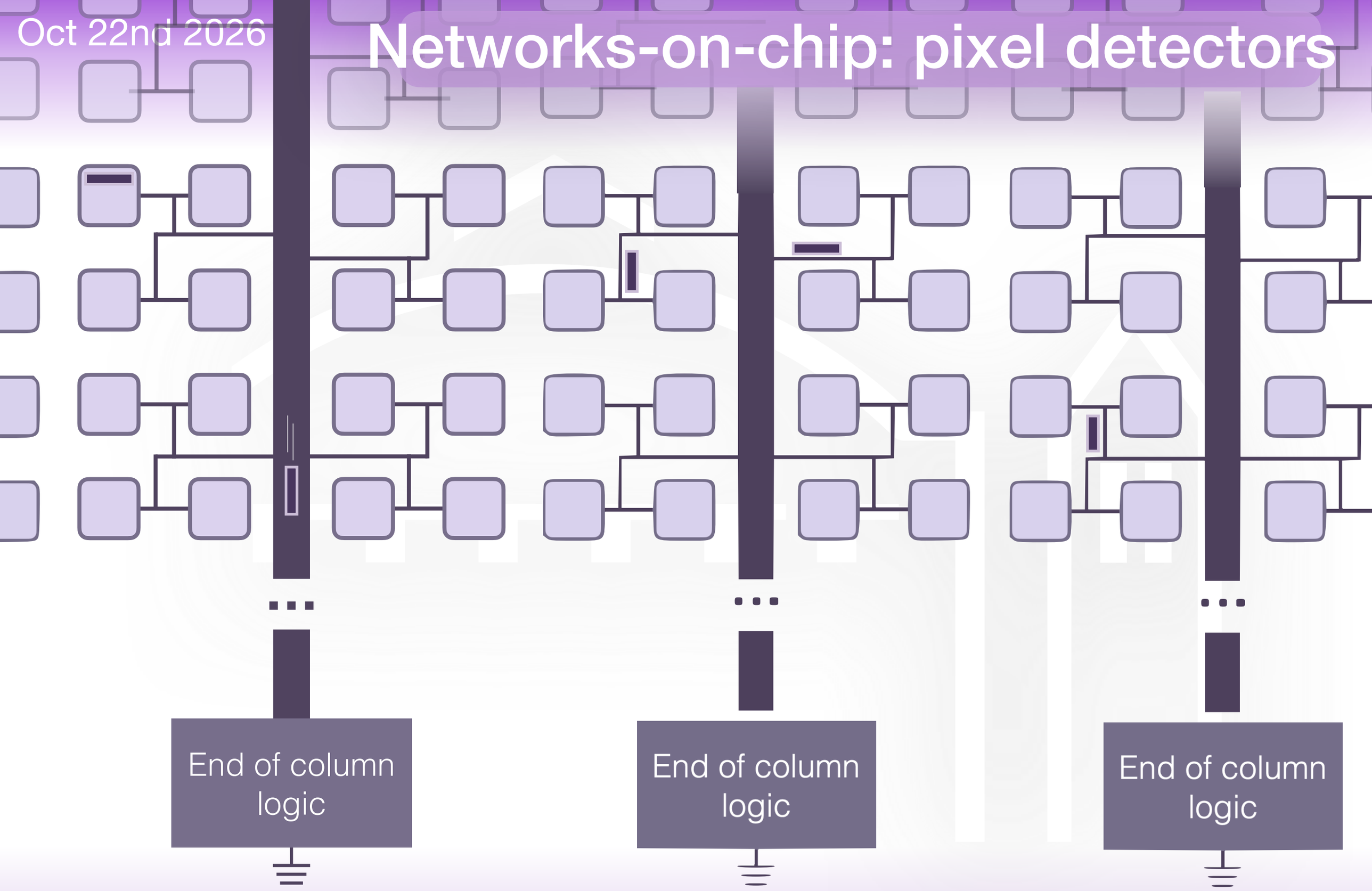
NIFTY “smart” router configuration

Check out Deion Feller’s poster on the NIFTY simulation of LArPix vN1 in his CPAD poster here: https://indico.global/event/17230/contributions/170178/

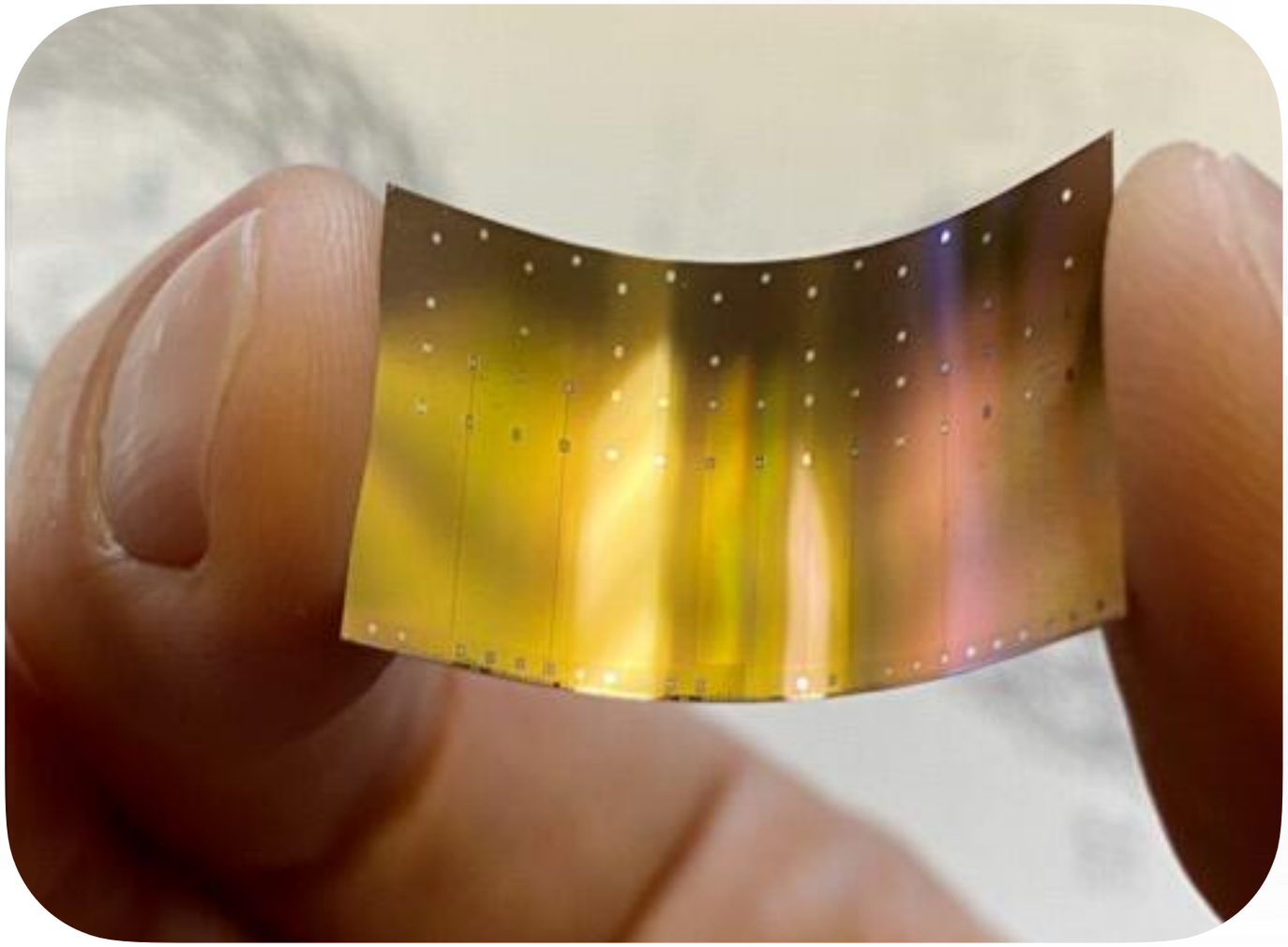


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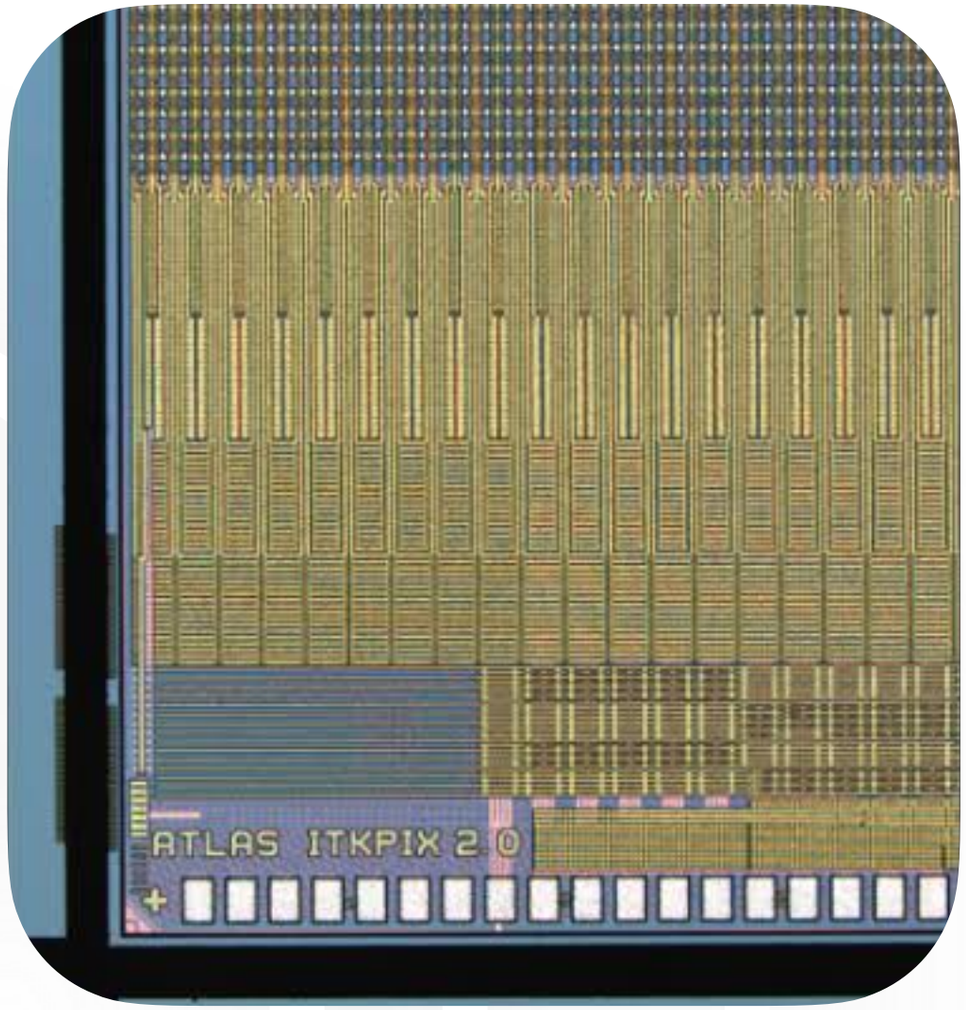
Networks-on-chip: pixel detectors



Networks-on-chip: **pixel detectors**



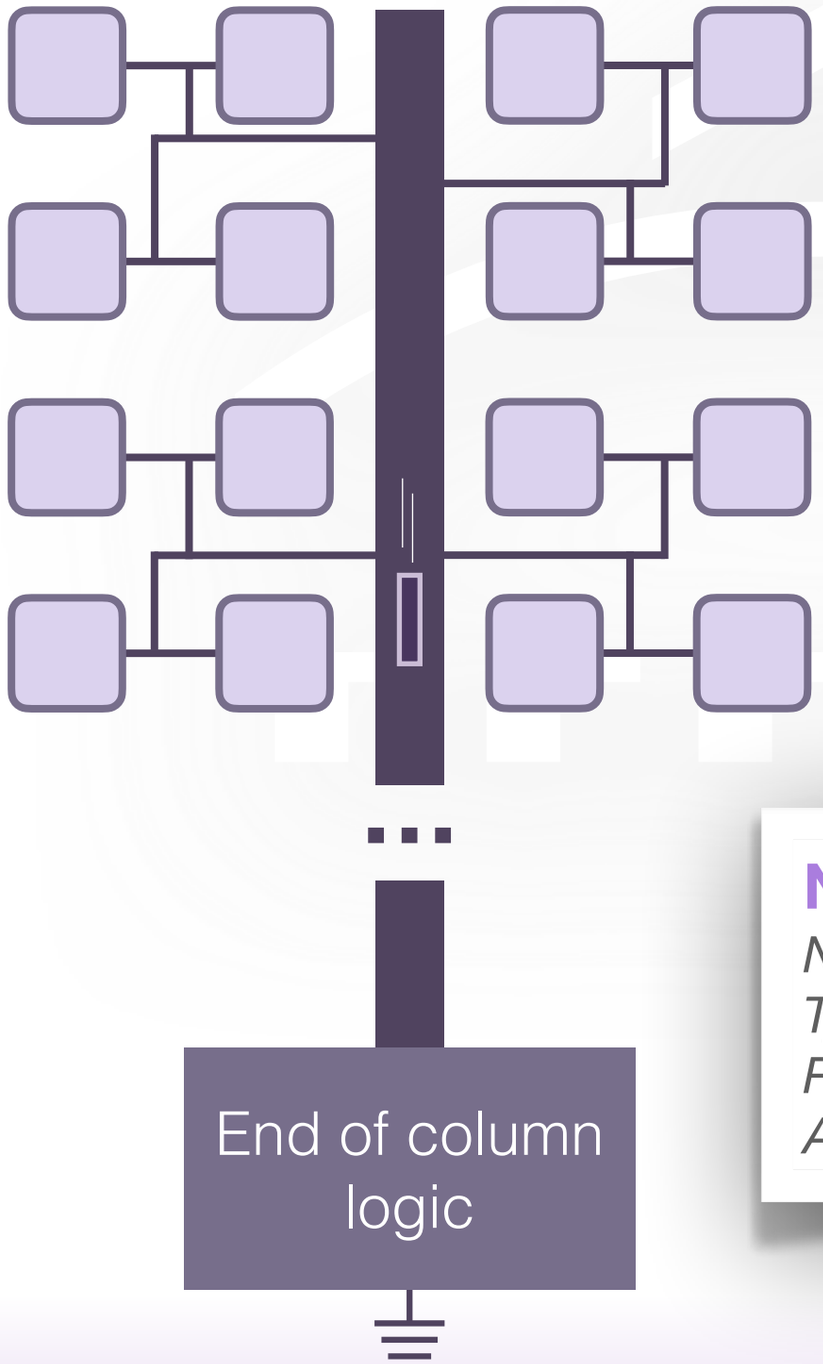
ALICE ITS3 MOSAIX Chip: https://indico.global/event/17230/contributions/169740/



RD53 chips: ITkPix and CROC for ATLAS & CMS, respectively

- Pixel detectors & associated readout subject to extreme conditions in collider experiments: can induce permanent or transient failures, incl. SEUs.
- Expensive to fabricate, especially for large form-factors: route around wafer defects.

Networks-on-chip: **pixel detectors**



- Unlike LArPix tiles, not a mesh network: instead there is a columnar bus for regions of data-generating pixels.
- Pixels/regions are not nodes, they just generate data and store it.
- Bus manager arbitrates readout.
- No centralized storage, data stored near pixel till needed. Need to read out hits whilst accruing more, trigger rate << hit rate (potentially accrue hits at 40 MHz, 1 MHz trigger).

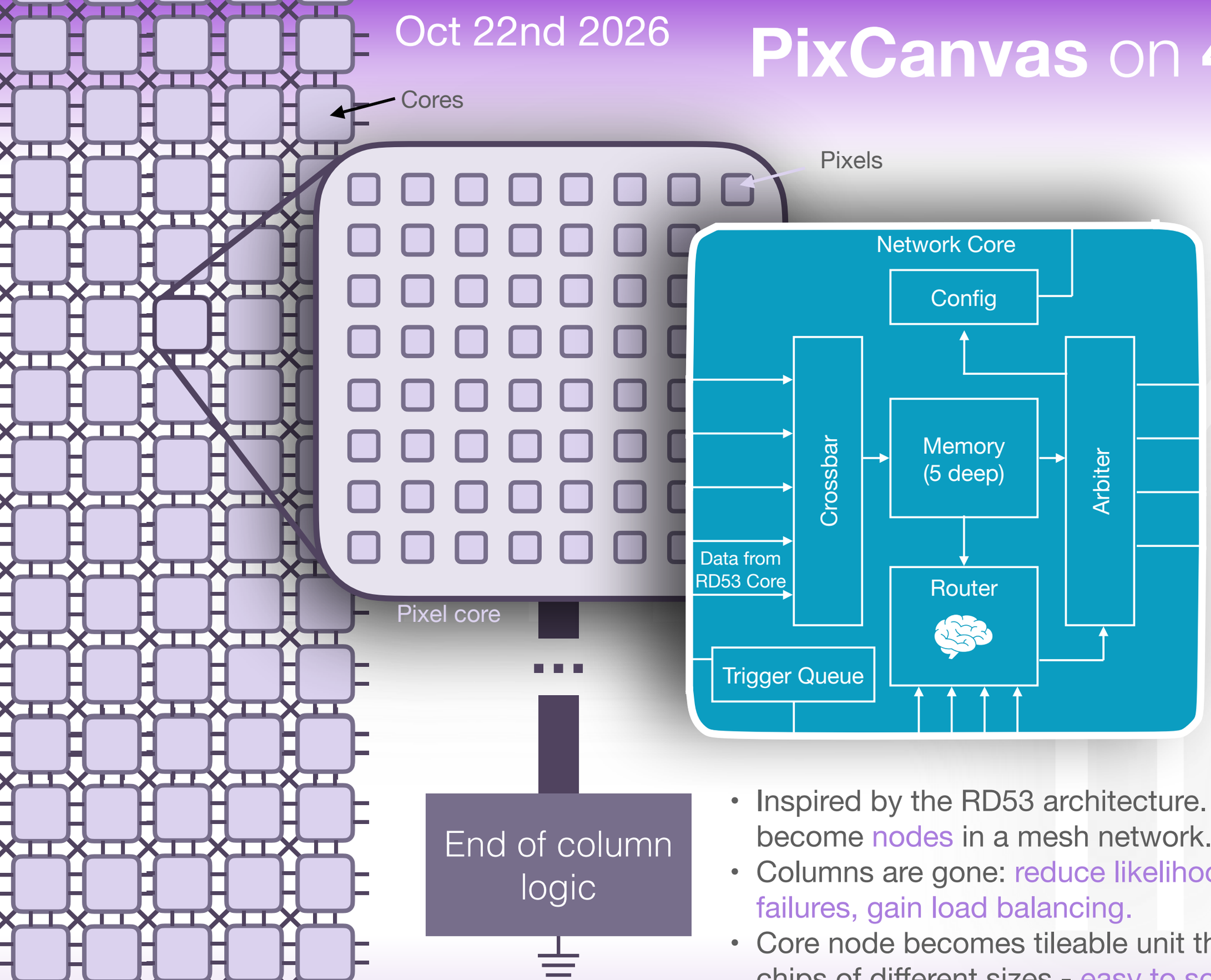
Network fact sheet

Name:	Pixel detector, e.g. ITkPix, CROC, MOSAIX
Type:	Leaves on a bus, then tree below EoC.
Root nodes:	End of column / event builders
Arcs/node:	Varies! Columnar bus is the key.

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PixCanvas on 4DFabric



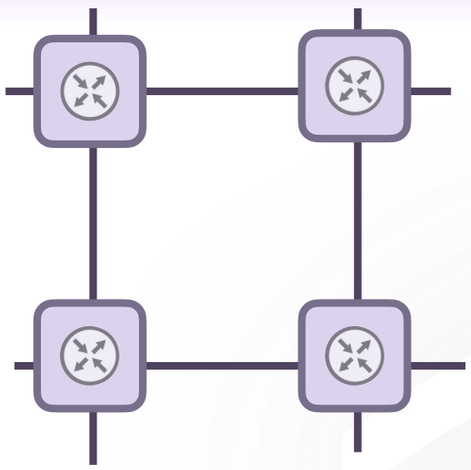
- Inspired by the RD53 architecture. Cores of pixels become nodes in a mesh network.
- Columns are gone: reduce likelihood of single-point failures, gain load balancing.
- Core node becomes tileable unit that be used to fill chips of different sizes - easy to scale!

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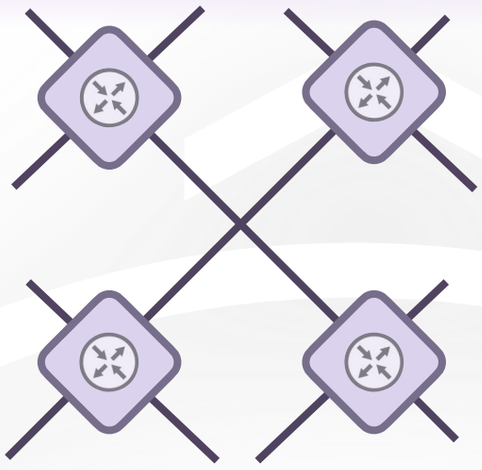
Network core graphic from Timon Heim.

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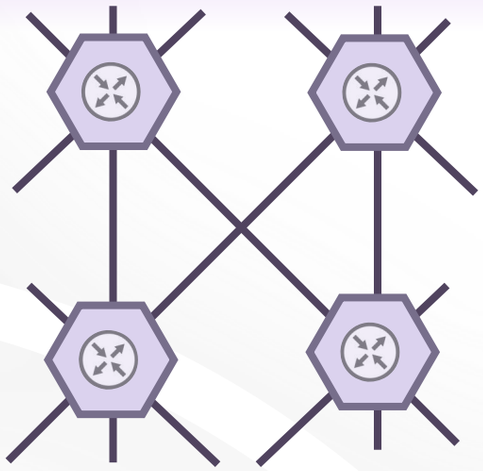
PixCanvas on 4DFabric



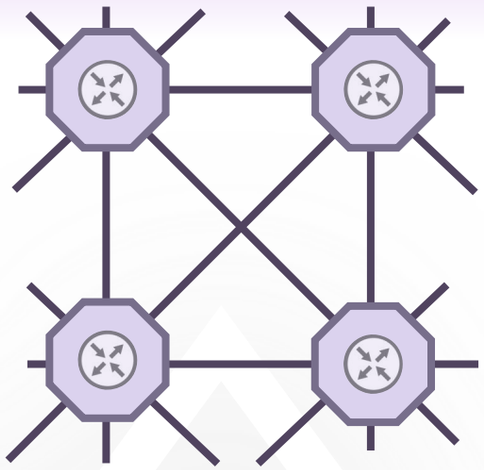
Square mesh



Diagonal mesh



Hexagonal mesh

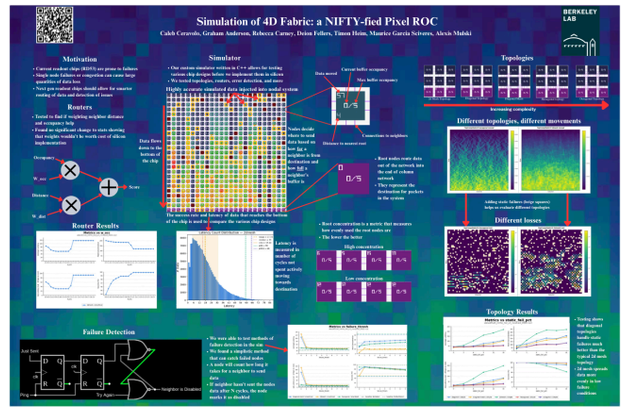


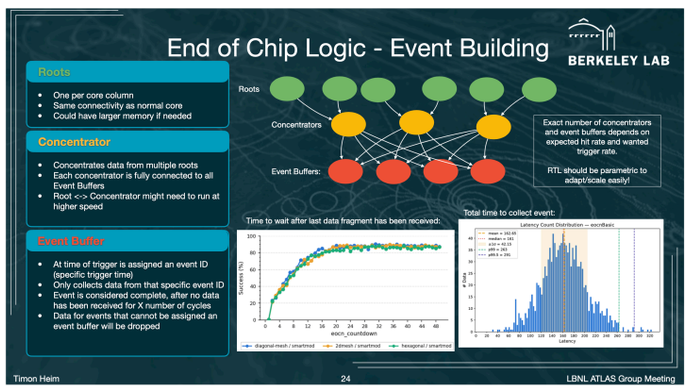
Octagonal mesh

1. NoC means can customize the mesh: square, diagonal, a mix of the two. Check out Caleb Ceravolo's poster exploring these topologies and their effect on throughput, latency, and load balancing in the periphery: https://indico.global/event/17230/contributions/169741/.

2. Add dedicated lines for node status via nifty messages (won't affect bandwidth, but still additional activity).

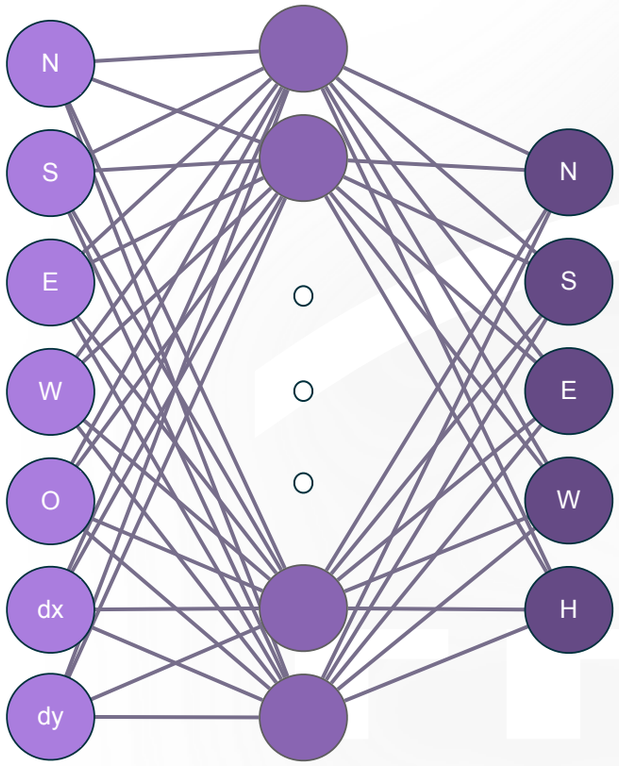
3. How the mesh drains into the periphery and events are built is a whole other topic, that Timon Heim discusses - alongside the PixCanvas chip! - in his talk here: https://indico.global/event/17230/contributions/169739/

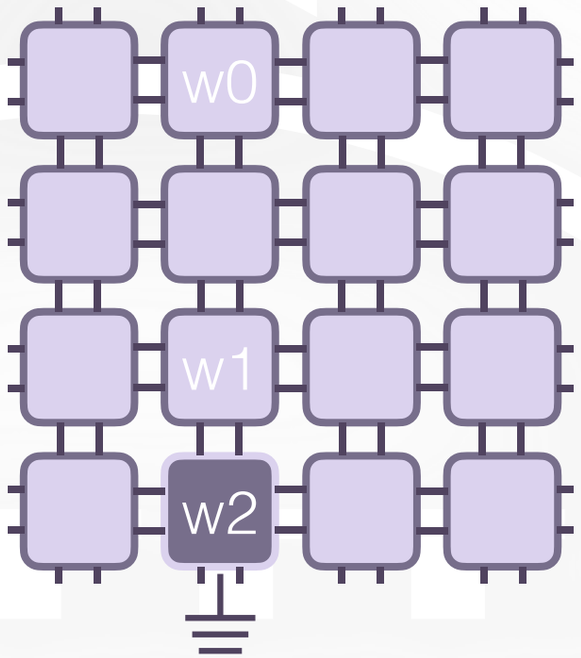


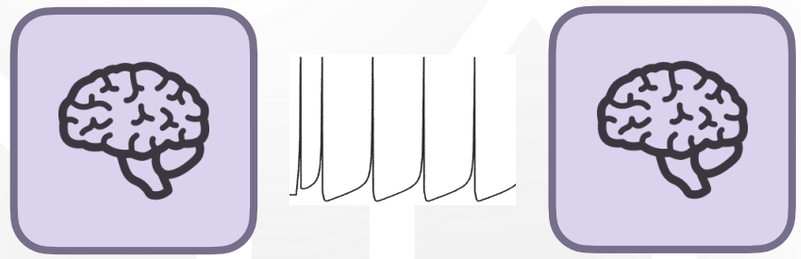


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Spiking on-chip/off-chip

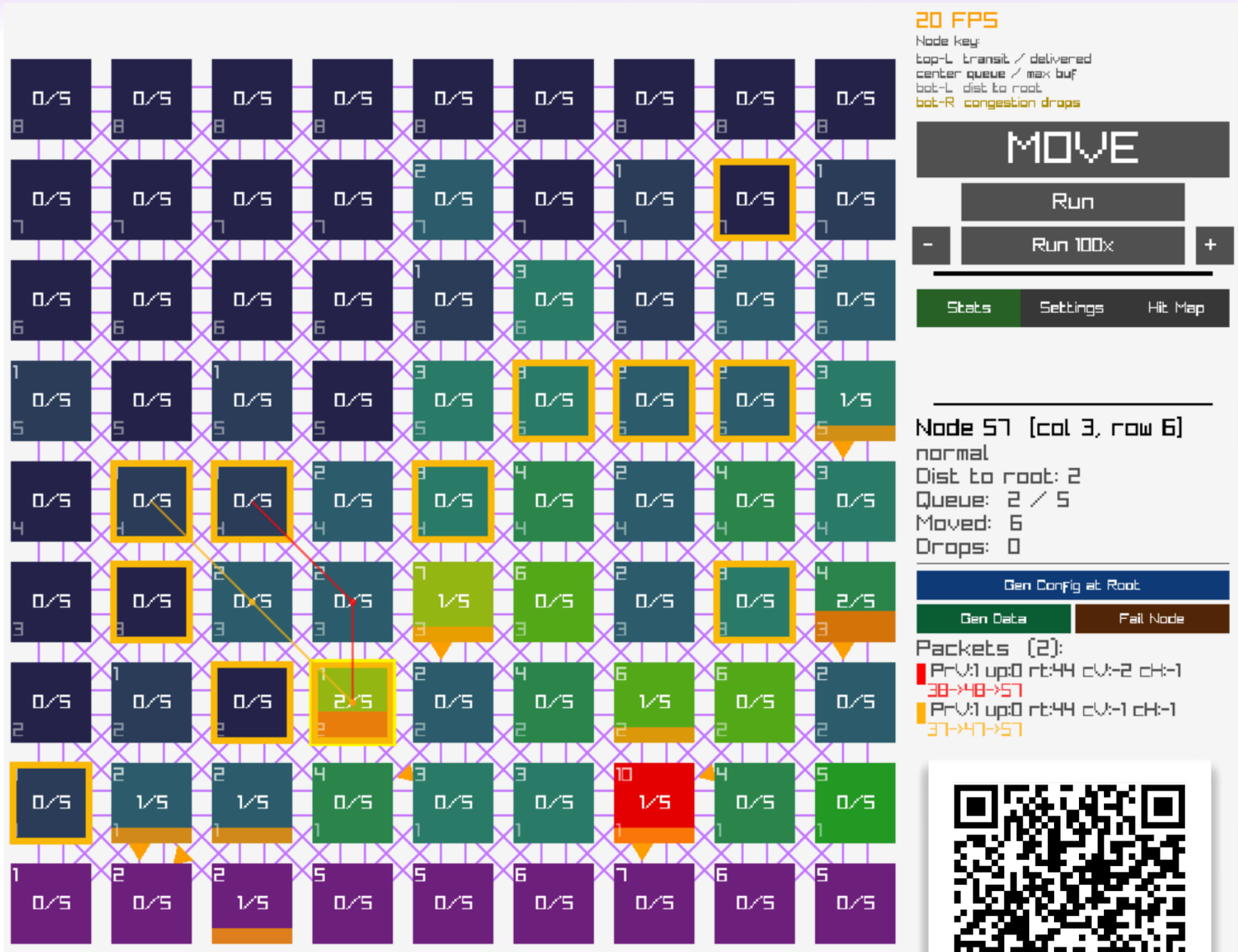






- Routing algorithms explored so far could easily be adapted for simple ML tools.
- Spiking neural networks potentially offer a fault-tolerant, lower power solution to expand router functionality. Quantized representation. Analog interfaces.
- NIFTY is exploring a spiking NN implementation of a router and off-chip spiking interfaces. Continuing to explore setting up the problem correctly..

Simulation **framework**



[Playlist of topology & router studies from Deion's poster session]

- All three branches of the project use a custom simulation framework in C++ with visualization using RayLib and web assembly endpoint support via Emscripten.
- Designed to explore different network topologies, routing schemes, node storage types - even nifty message-passing!
- C++ lends itself well to the shared components of the project, derived node types, common sequence of events. All 3 branches of NIFTY can benefit from features developed. Including hooks to established python ML toolkits like scikit-learn and PyTorch to support SNN node development. CI scenarios to benchmark known failure types.

Collaborative development



Maurice Garcia-Sciveres
PI, Senior Scientist
Berkeley Lab, Physics Div



Graham Anderson
Undergraduate student
UC Berkeley, EECS



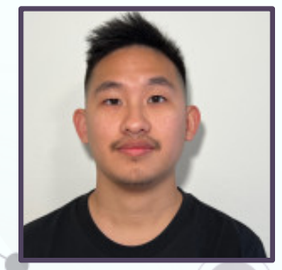
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Rebecca Carney
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Berkeley Lab, Eng div



Caleb Ceravolo
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Jay Chan
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Berkeley Lab, CS div



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Kalindi Gosine
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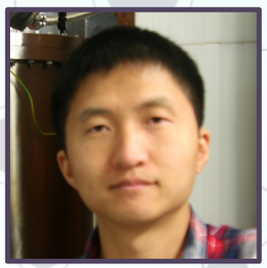
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Electrical engineer
UPenn, Physics



Nirmalendu Patra
Computer systems eng
Berkeley Lab, CS div



John Shalf
Department head
Berkeley Lab, CS div

Whilst we have individual responsibilities within the 3 branches of NIFTY, our efforts span the full project. Nifty is collaborative by design, with open meetings, shared toolkits and frameworks.

A **nifty** summary

The NIFTY project develops network architectures with built-in intelligence to make detectors tolerant to manufacturing and operational single-point effects and at the same time provide data load balancing to optimize readout bandwidth.

NIFTY combines integrated circuit design, systems engineering, machine learning, and particle physics instrumentation expertise across three divisions at Berkeley Lab, University of Pennsylvania, and the University of Texas Arlington.

In this first phase, the project is working to produce two demonstrator chips in the next few months: collider-experiment-style PixCanvas and DUNE-inspired LArPix-vN1.

Network **I**ntelligence **F**ault **T**olerance is **NI**FTY

https://nifty.lbl.gov/www/about/

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