A Cryogenic Charge Imager for Continuous Operation in Liquid Noble Gases

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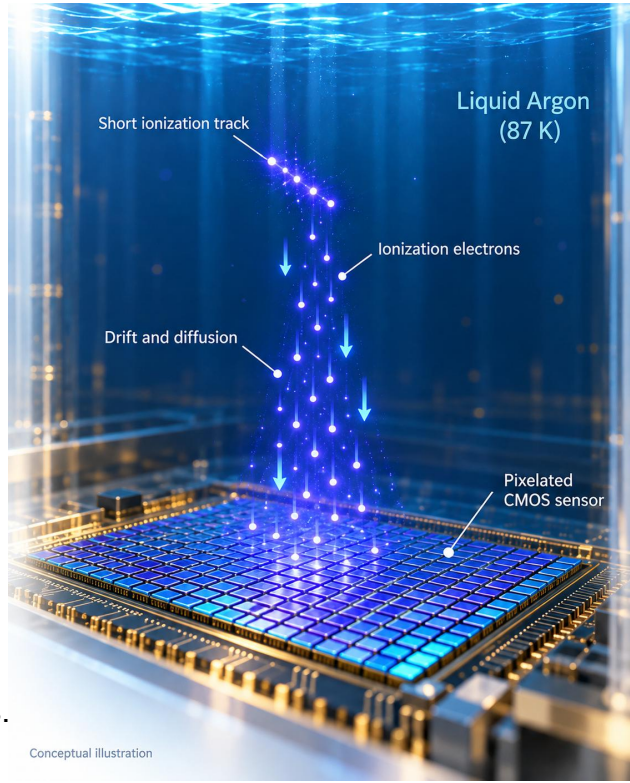
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Cryogenic Charge Imager

CryoChargeImager is a **pixelated CMOS sensor** designed to **collect drifting electrons directly on its pixel electrodes** and measure their **two-dimensional charge distribution** in liquid noble-gas detectors.



Goal: Fine-pitch imaging of weak charge signals

- We aim to **measure weak charge signals** and **resolve fine structures in ionization tracks**.

3 main design targets — to be achieved simultaneously:

➢ 50 μm pitch

- an **exploratory design choice** for **fine sampling** of the arriving charge distribution.
- At longer drift distances, the achievable spatial resolution may become **diffusion-limited**.

➢ 20–30 e^- RMS ENC

- With fine pixels, charge from one event can be **shared among multiple channels**, and electron **diffusion** can spread it further.
- Therefore, **low electronic noise** is essential to preserve these small per-pixel signals.

➢ ~1 μW/pixel

- The pixel front ends are designed to remain **continuously biased during acquisition**.
- **Low power per pixel** helps limit the **heat load** in cryogenic detectors, and **supports scaling to larger arrays**.

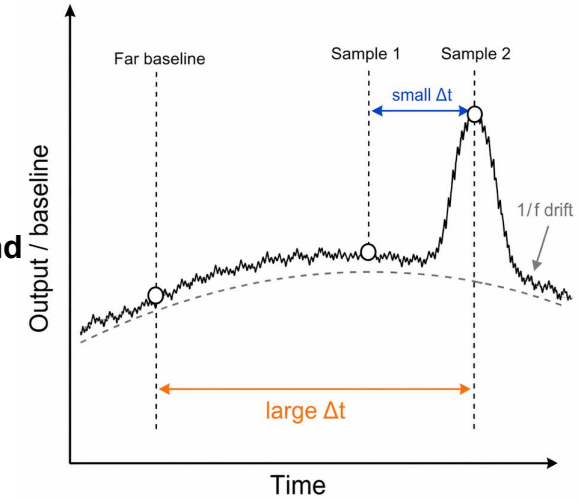
Two Key Challenges

Challenge 1: Low-noise front end under a tight power budget

- The **charge-sensitive amplifier (CSA)** is the first amplification stage, and its **input transistor** is often a dominant source of front-end noise.
- Higher input-transistor **transconductance (gm)** generally helps reduce input-referred thermal noise.
- However, increasing **gm** usually requires more bias current and therefore more power.
- need to balance **low noise and low power consumption**.

Challenge 2: Low-frequency noise in compact pixel readout

- A compact pixel leaves limited space for a **full shaper and readout chain**.
- When baseline and signal samples are separated by a long time interval, **1/f noise and baseline drift** become harder to cancel.
- We need effective noise suppression with **minimal in-pixel circuitry**.

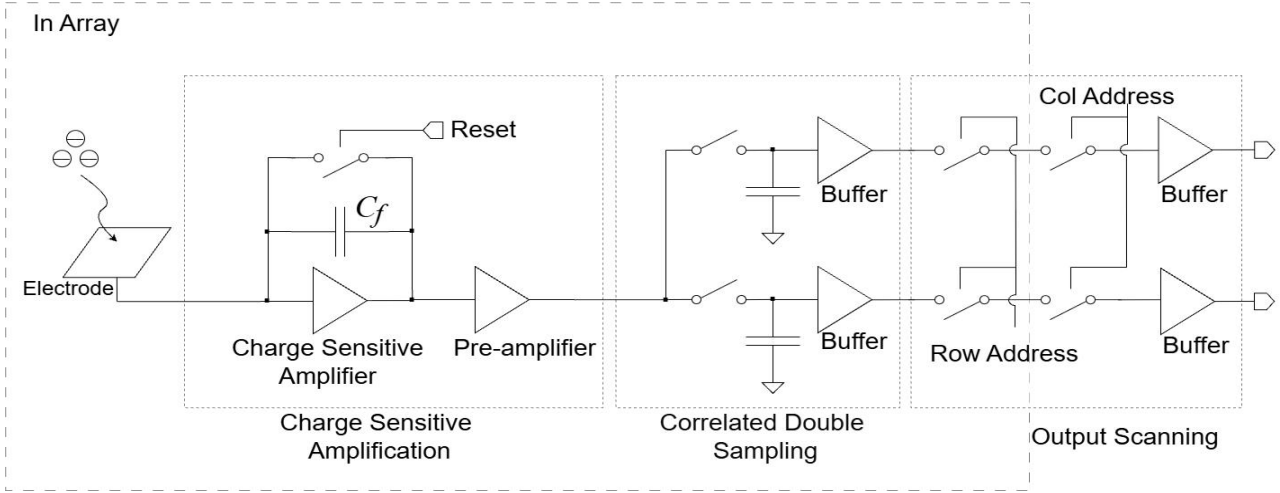


CDS = Sample 2 − Sample 1

Our solution:

- Optimize the **CSA** for low noise under tight power budget
- Use extra **low-pass filtering** to limit the effective noise bandwidth and reduce integrated thermal noise.
- Use **in-pixel correlated double sampling (CDS)** with closely spaced samples to suppress reset noise and low-frequency fluctuations.
- Store both samples locally for sequential readout, so the **CDS sampling interval is independent of the full-array readout time**.

Pixel Architecture and Readout Scheme



- Each pixel integrates a **charge-collection electrode,** a low-noise **CSA**, a **pre-amplifier**, **CDS** circuit and **row selection**.

- The **preamplifier** boosts the signal before sampling, reducing the **input-referred noise from the sampling stage**.
  - because the **sampling capacitors** are much larger than **feedback capacitor (Cf)** for analog hold, their **kTC noise** could otherwise degrade the low-noise performance of the CSA
- Two **sampling capacitors** capture the nearby baseline and signal samples.
- **Local low-power buffers** isolate the stored analog values from the downstream scanning network.
- After **globally synchronized sampling**, the stored values are selected by **row/column scanning** and sent off chip through two **shared output buffers**.

- **Key idea:** to perform the **critical filtering and CDS sampling locally** inside each pixel, while using **shared scanning** only for output

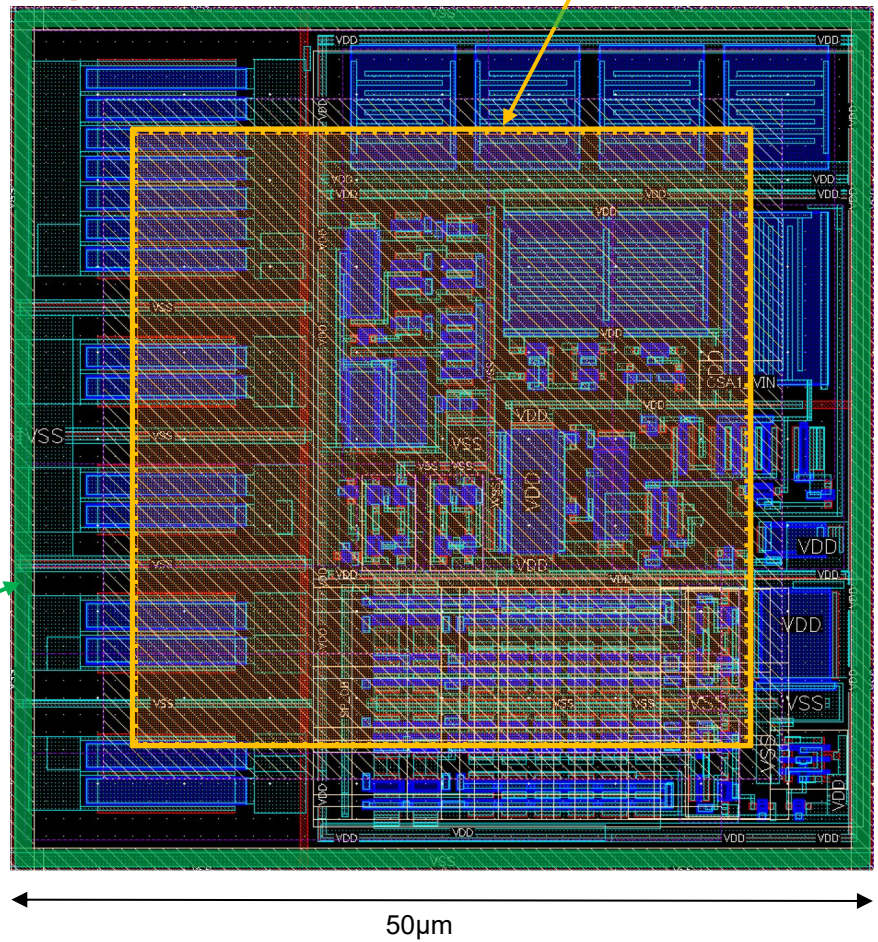
Pixel Design

Front-end design choices

- Implemented in **TSMC 180 nm**
- The **CSA** uses a **telescopic cascode** topology
  Chosen for **low noise, high single-stage gain** (~9500 V/V, ~80 dB, DC), and **compact** implementation (no compensation capacitor is needed)
- **feedback capacitor(Cf) = 25 fF**
- Noise is optimized for **input capacitance < 100 fF**
- The power budget is intentionally **focused on the front end**: **>60%** of the pixel power is assigned to the CSA.

Pixel layout

- A **guard ring** surrounding **charge-collection electrode** helps shape the local field and improve charge collection
- Each pixel is placed in its own **deep N-well:** improve **substrate isolation,** reduce **inter-pixel noise coupling**



Transient-Noise Waveforms of CDS Operation

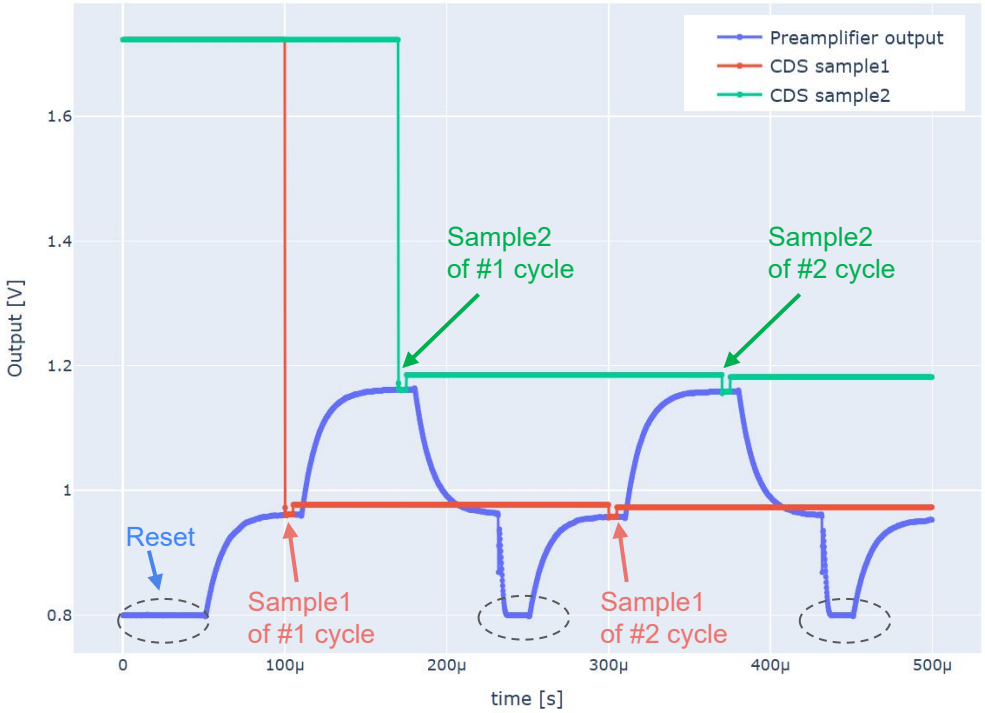
- Because the circuit contains **reset** and **sampling switches**, a **transient-noise simulation** is used to directly show the time-domain noise behavior

- The simulated noise **bandwidth** is chosen wide enough to cover the noise frequency range visible to the circuit during operation

- **blue**: the **preamplifier output** after CSA; its low-level region corresponds to the **reset state** of the CSA

- **red** and **green:** two **CDS sample-hold nodes;** they track the preamplifier output during sampling and hold the value afterward

- A small jump appears due to **charge injection** from the sampling switch transistors;
  - mainly through **parasitic gate-to-source/drain capacitors** driven by the **sampling control signal**;
  - here it mainly behaves as a **repeatable offset** and is expected to be **calibratable**

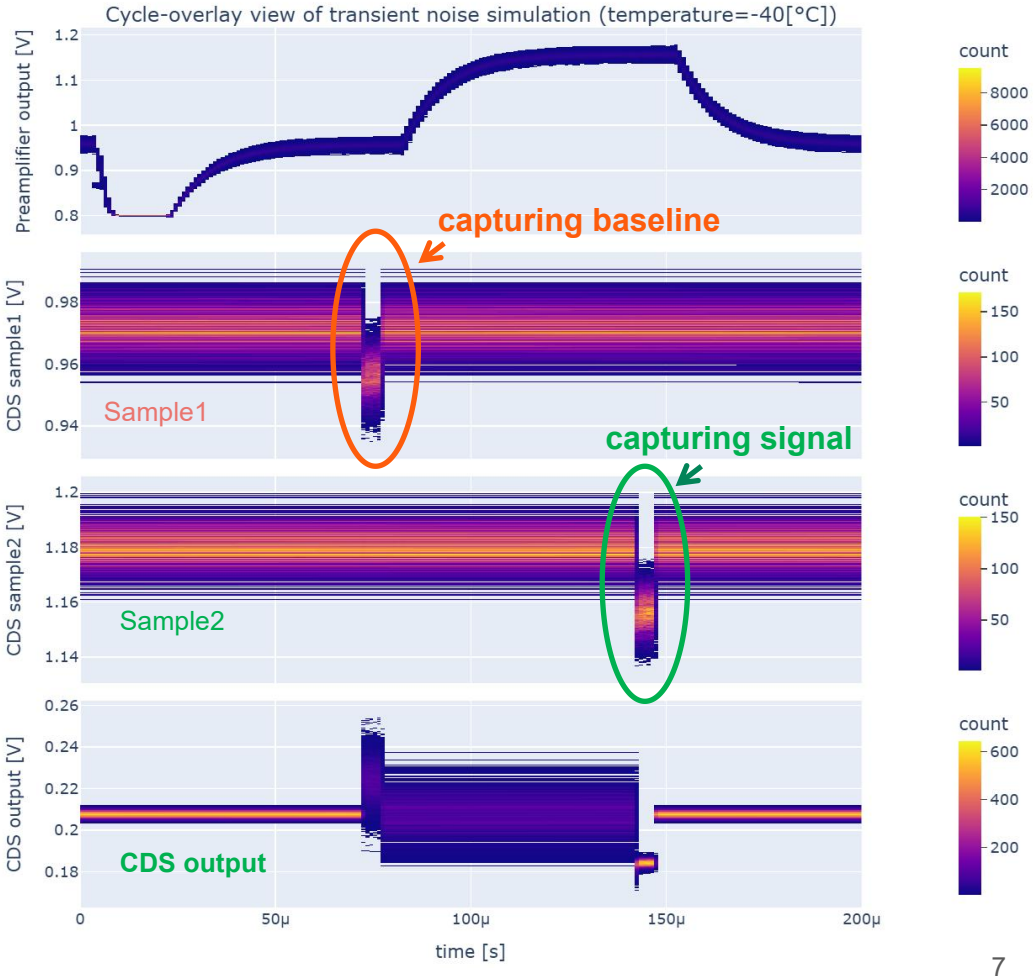


- simulated **CDS timing behavior** is consistent with the intended **time-domain** operation

Statistical Time-Domain View of CDS Noise Suppression

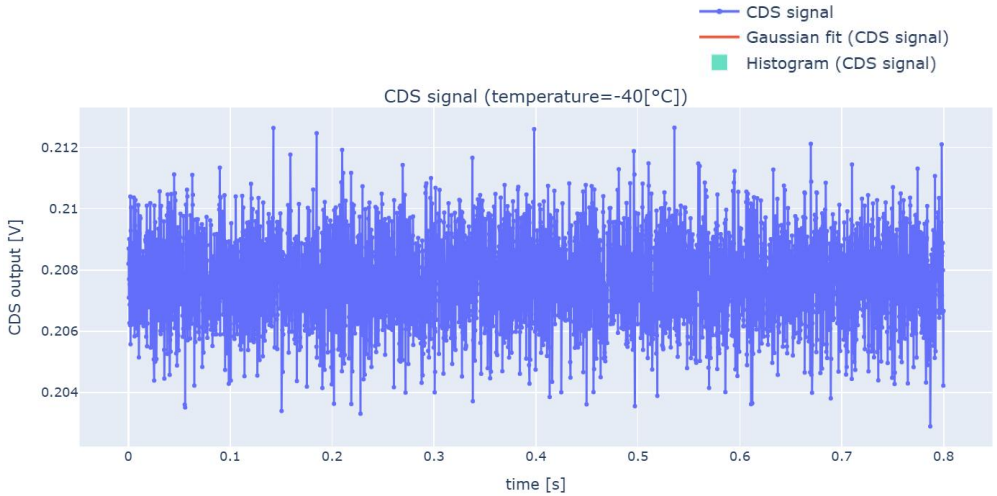
Color = count in the amplitude histogram at each time point

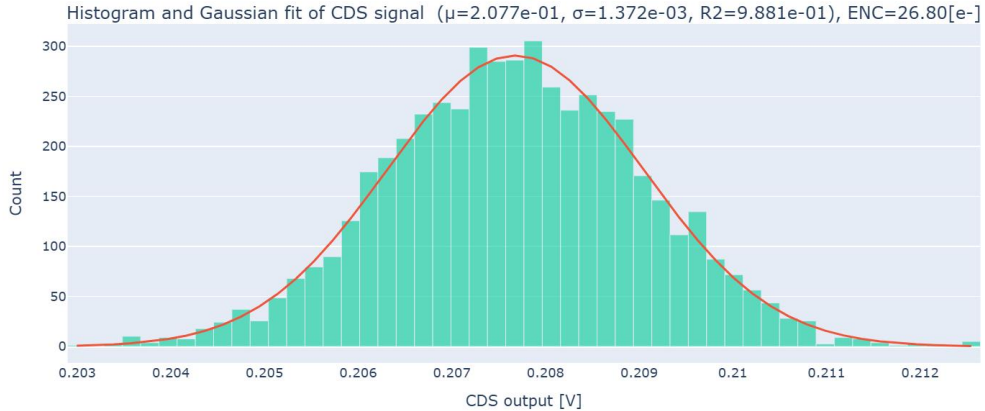
- Many transient-noise cycles are **aligned in time** and **accumulated statistically**
- The **amplitude distribution** at each time is approximately **Gaussian**, and its **vertical spread** reflects the **noise sigma**
- The first three panels show the **preamplifier output**, **CDS sample1**, and **CDS sample2**.
- The switching-induced charge-injection jumps are also aligned in time, because they are caused by the repeatable sampling action.
- The fourth panel shows the **CDS output = sample2 − sample1**.
  - **before sample1**： spread is narrower → lower noise
  - **between sample1 and sample2**：
    much larger spread → higher noise
  - **after sample2**： narrow again → lower noise
- The CDS noise is **low** when sample1 and sample2 belong to the **same event** and are taken **close in time**, but becomes **much larger** when the two stored values come from **different cycles** and are separated by a **longer effective time interval**.
- **This gives a direct visual demonstration of CDS-based low-frequency noise suppression from the transient-noise simulation.**



Final Simulated CDS Noise Result

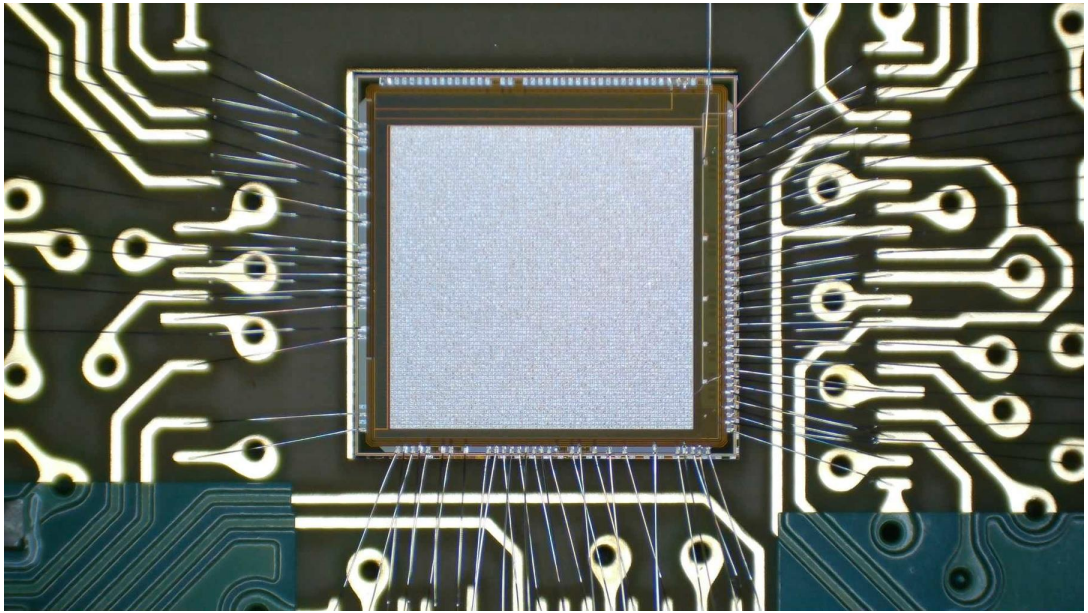
- At the valid CDS **extraction time**, one **CDS output** value is taken from each cycle.
- **upper panel**: **extracted CDS values** versus **time**.
- **lower panel**: **histogram** and **Gaussian fit** of the CDS output.
- The fitted **σ** is converted to **input-referred ENC**, **giving 26.8 e^- at -40 °C (28.2 e^- at 27°C)**.



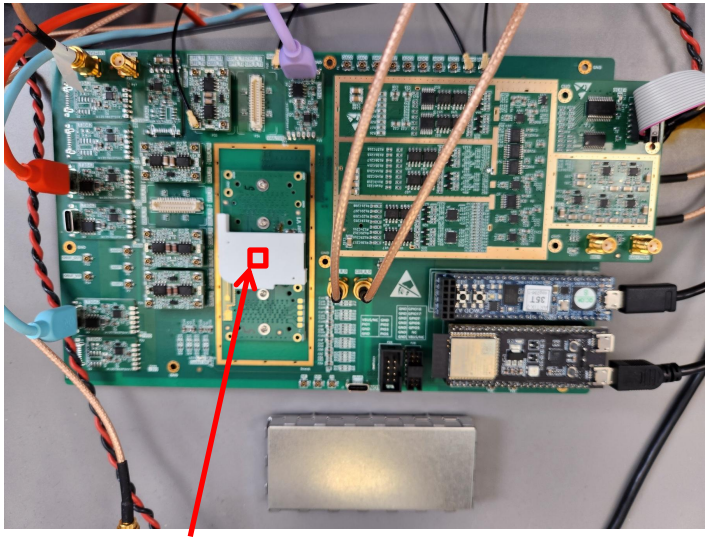


First Silicon

Bonded chip and carrier



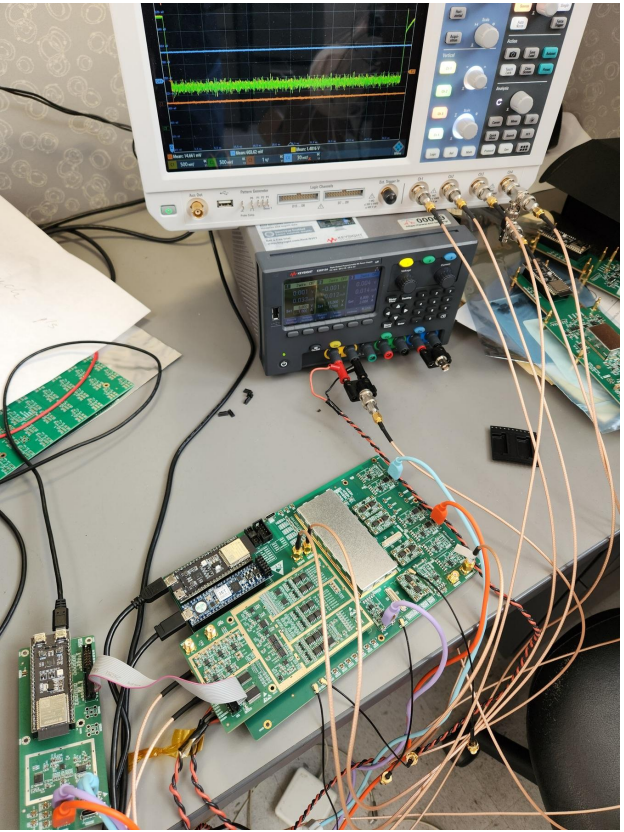
Evaluation board



The ASIC is under a 3D-printed protective cover.

- The microscope image on the left shows the fabricated die and its **wire bonds** to the carrier.
- Chip size **5mm × 5 mm,** contains an **80 × 80** array, giving **6,400 pixels** at a **50 µm pitch**.
- The photograph on the right shows the evaluation board used for electrical characterization.

AI-Assisted Electrical Characterization Workflow



- **First, we use AI to control the test instruments.**

  - The oscilloscope, waveform generator, programmable power supplies, FPGA, and MCU are all connected to a PC, and **fully controlled by AI**.

  - AI-assisted scripts coordinate instrument setup, bias scans, waveform capture, and data logging.

- **Second, we protect the ASIC at the hardware level.**

  - Earlier AI-driven tests(**this April/May**) on our SKY130 ASIC showed that unsafe commands, such as out-of-range DAC settings, could damage the chip.

  - For **CryoChargeImager**, we built a protected test platform with **hardware-enforced safety limits** and continuous **readback of bias voltages and currents**.

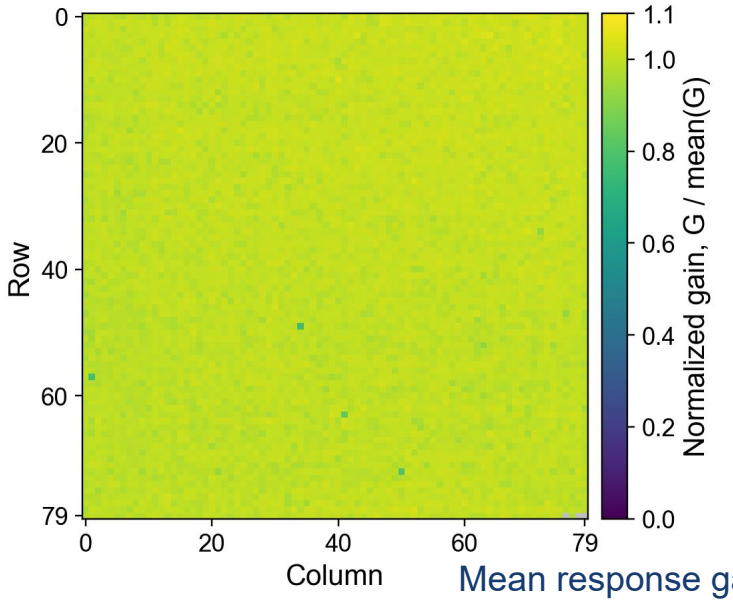
  - This allows the AI to check operating conditions while the hardware prevents unsafe settings from reaching the ASIC.

- **Finally, we keep the tests traceable and people in the loop.**

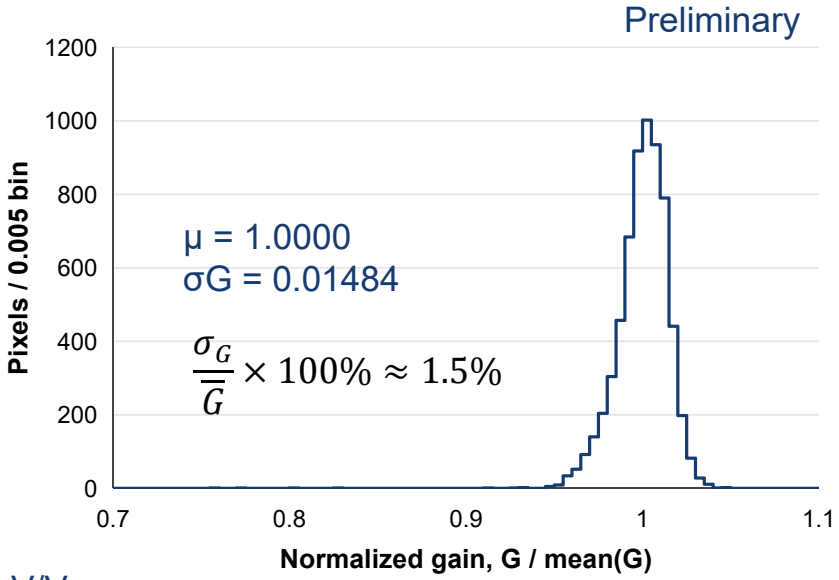
  - Test code, instrument settings, hardware connections, and measurement results are all **version-controlled in Git** for **full traceability and re-checking**.

  - **People remain in the loop** to define test goals, verify waveforms visually, and confirm the cabling and hardware state.

Full-Array Response Uniformity

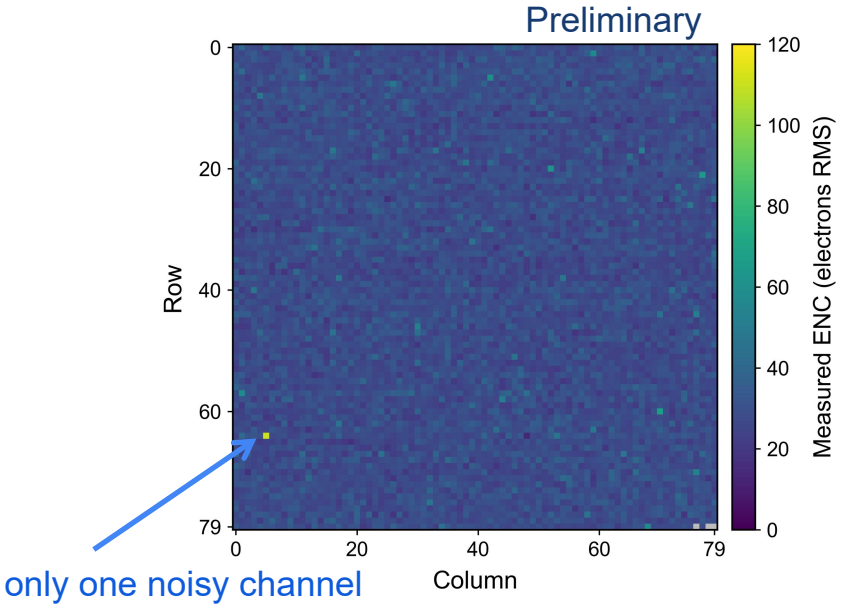


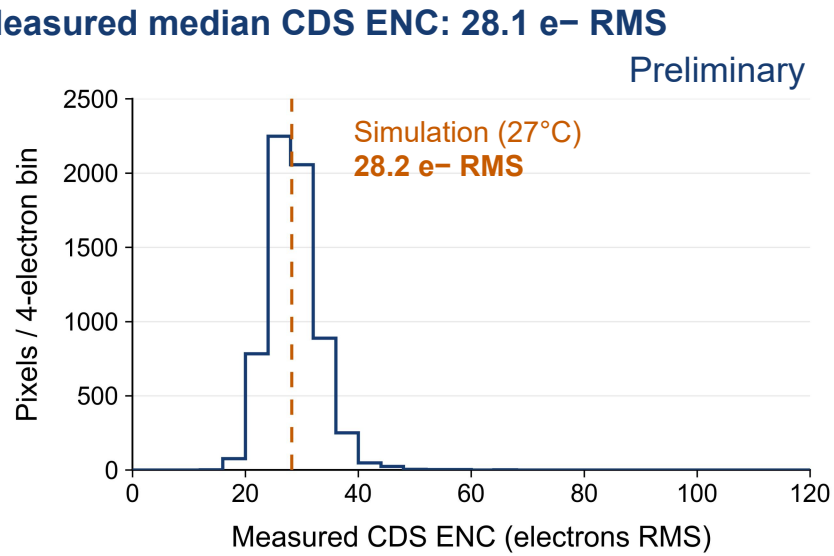
Mean response gain: 1.631 V/V



- Each pixel has the **same nominal guard-ring geometry**, so the capacitive coupling to the **charge-collection electrode** is expected to be **basicly the same across the array**.
- We apply a voltage step to the **common guard ring**, injecting approximately **the same test charge** into each pixel.
- By comparing the resulting **CDS responses**, we can evaluate the **pixel-to-pixel gain uniformity** (Each response is normalized to the array mean).
- As shown in the histogram, the normalized responses are **closely clustered around one**, with a relative RMS **gain spread** of only **1.5%**, **indicating good gain uniformity across the array**.

Full-Array CDS Noise





- The noise is **low across most of the array**, with **one pixel showing much higher noise**.
- At room temperature, the **median input-referred noise** is **28.1 e⁻ RMS** across all pixels,.
- This result is **in close agreement with the simulation**, which predicts **28.2 e⁻ RMS at 27 °C**.

Preliminary result. Input-referred ENC calculated using Cf=25fF(design value); independent absolute charge calibration is pending.

Power Consumption

Quantity	Measured / derived value
Total ASIC power	≈6.25 mW
Number of pixels	6400
Average per pixel	≈0.98 µW/pixel

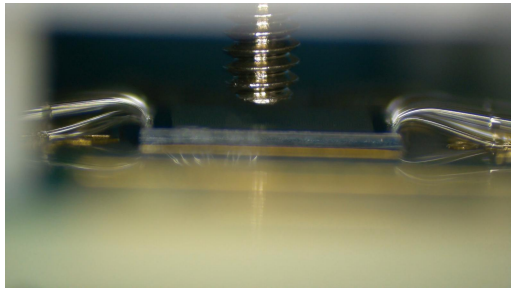
Preliminary

- We measured the ASIC **power consumption during full-frame readout at room temperature**.
- The current frame rate is about **20 frames per second**, mainly limited by **oscilloscope waveform acquisition and data transfer**.
- The total power is about **6.25 mW** for the **6,400 pixels**.
- This gives an average of **0.98 µW per pixel**, close to our **design target of 1 µW per pixel**.
- The **analog circuitry** dominates the measured power. The digital contribution is small in this setup..

6.25 mW ÷ 6400 ≈ 0.98 µW per pixel

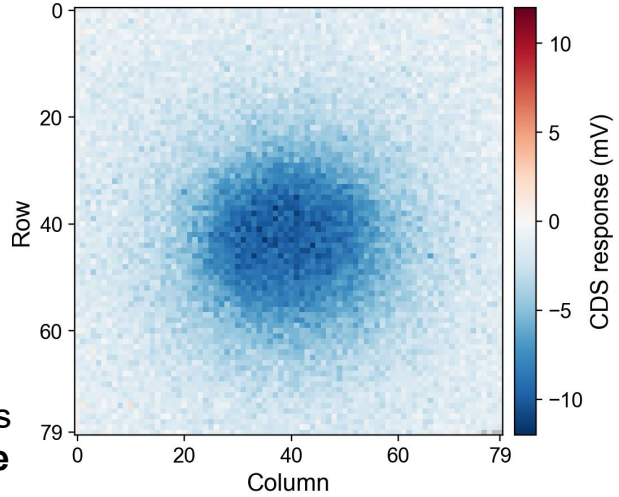
Spatial Response to an External Electrode

Screw electrode

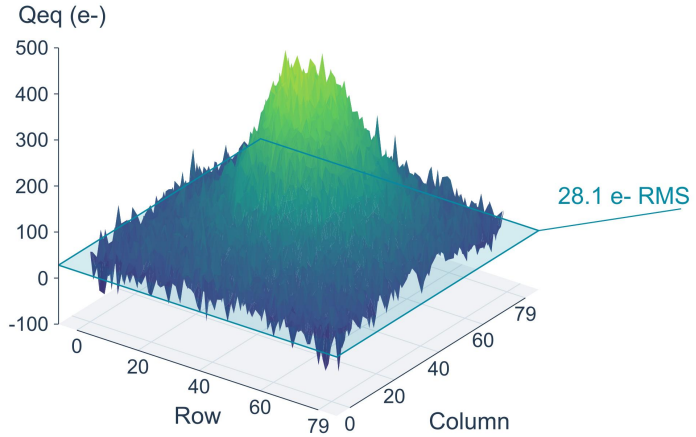


- A small **screw electrode** is placed above the chip.
- We apply voltage pulses to this electrode to **inject test charge signals into the pixel array** through capacitive coupling.

2D CDS response



3D input-equivalent charge



- The **2D CDS response map** shows a clear spatial pattern, with the **strongest response near the electrode** and weaker responses farther away.
- The **3D surface** shows the same response converted to **input-equivalent charge**, with a **peak of about 460 e^-** .
- The blue plane shows a 28.1 e^- RMS noise reference.
- This demonstrates **a clear spatial response across the pixel array** using capacitive injection.

Summary and Next Steps

Summary

- We developed an **80 × 80 pixel CMOS charge imager** with **50 μm pitch**, combining **continuously biased front ends** and **in-pixel CDS sampling**.
- Room-temperature tests demonstrate **full-array operation** and a **relative RMS gain spread of about 1.5%** across the pixel array.
- The median CDS noise is **28.1 e^- RMS** (at 27 °C), absolute charge calibration is pending.
- The power consumption during full-frame readout is about **1 μW/pixel** (at 27 °C).
- These results provide **an encouraging starting point** for **fine-pitch, low-noise, and low-power charge imaging in liquid argon**.

Next Steps

- Test the ASIC in **liquid argon**, including cryogenic noise and power performance, followed by **direct collection of drifting electrons**.
- Explore **in-pixel timing using a time-to-amplitude converter (TAC)** in the next chip version, toward **three-dimensional track reconstruction**.

Thank you!

Backup

Noise sources in charge readout

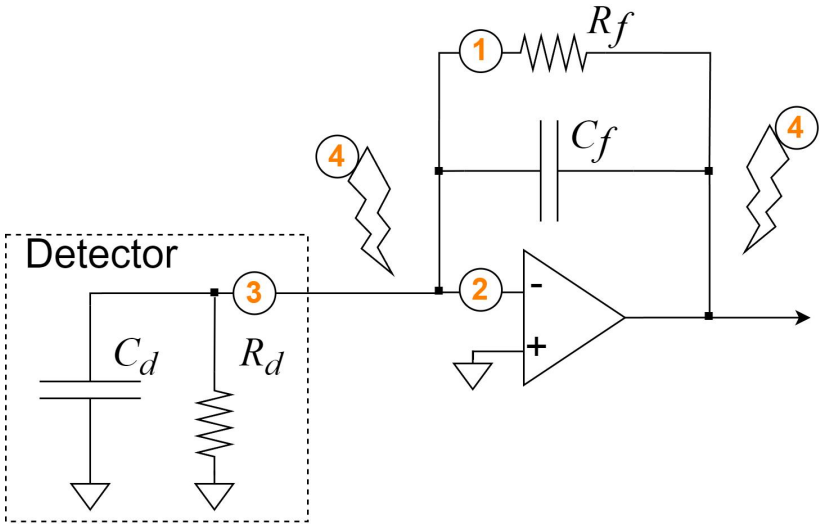
1.Thermal noise of the feedback resistor:
Rf normally very large, > **10^8** Ohm
thermal noise can be a major contribution here

2. Internal noise of the voltage amplifier:

- **Thermal noise:** produced by the thermal motion of charge carriers within any resistor in the amplifier
- **1/f noise** (or flicker noise): primarily associated with semiconductor fabrication process
- **Shot noise**: originates from the Poisson process of the discrete charge carriers movement

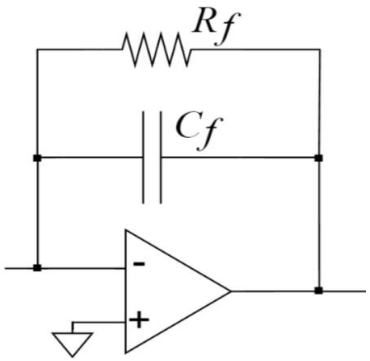
3. Detector contribution:

- **Leakage current:** the resistance (Rd) along the path of the leakage current will bring additional thermal noise into CSA
- **Capacitance**: will affect the noise performance of CSA



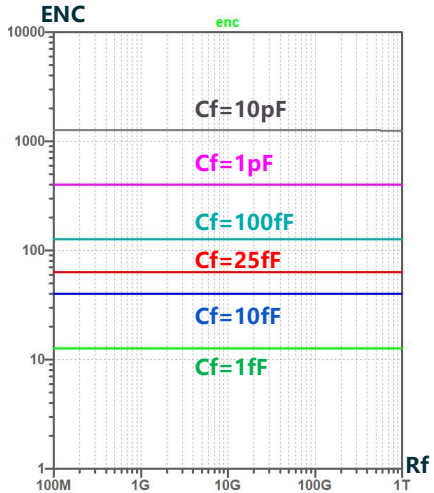
4. Environmental interference: mainly involves external EM radiation coupling, such as 60Hz noise from the power line everywhere

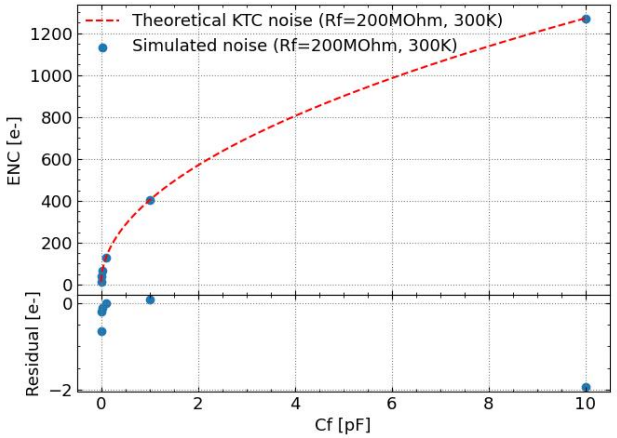
Continuous-reset scheme for CSA



- A large feedback resistor Rf **continuously discharges** the feedback capacitor Cf.
- This scheme **avoids reset dead time**, but introduces **thermal noise from Rf**
- A larger Rf gives higher resistor **noise spectral density**, but a smaller bandwidth
- Therefore, the integrated **equivalent noise charge(ENC)** from Rf **is set by Cf, ideally independent of Rf** (without shaper)
  → This leads to the familiar **kTC noise** behavior $Q_n = \sqrt{k_B T C_f}$

- Simulation: for an **ideal CSA** (noiseless), sweep Cf and Rf, observe the changes in **ENC**
  Cf = 1fF, 10fF, 25fF, 100fF, 1pF, 10pF
  Rf = 100M ~ 1T (10^8~10^{12})
  (**1mHz~1GHz**, 300K temperature) .
- Simulation agrees with the expected kTC trend





Continuous-reset scheme for CSA

- For common **CRm-RCn shaping**, the feedback decay time constant Rf*Cf is usually chosen to be **much longer than** the shaper time constant (**shaping time**) (or peaking-time scale)

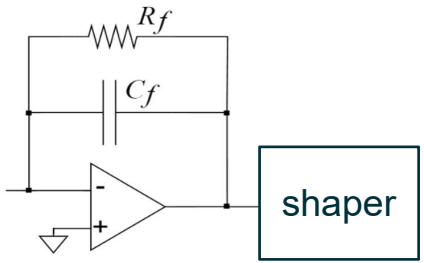
- Simulation: for an **ideal CSA + shaper** sweep Cf and Rf , **ENC input-referred**
  Cf = 1fF, 10fF, 25fF, 100fF, 1pF, 10pF
  Rf = 100M ~ 1T (10^{8}~10^{12})
  (1mHz~1GHz, temperature= **- 40C**)

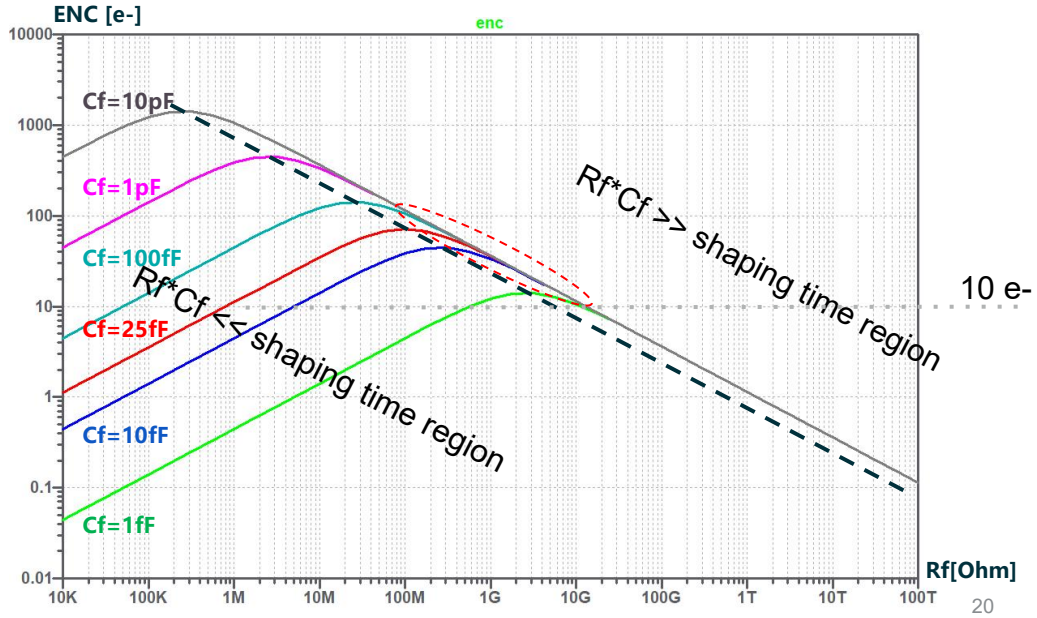
- Shaper: CR2-RC3, shaping time=2us

- Rf*Cf << shaping time: ENC ↑ with Rf, Cf
- Rf*Cf >> shaping time: ENC ↓ with Rf, not change with Cf

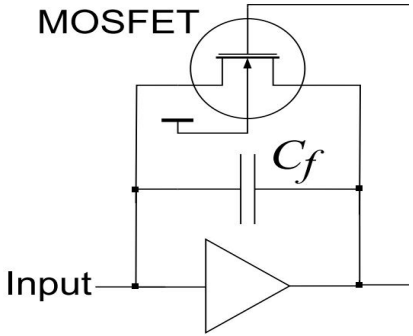
- For continuous-reset CSAs, Rf is commonly in the range of **hundreds of MΩ to a few GΩ**, depending on Cf, **leakage current**, and the required decay time constant .

- **Even with an ideal CSA, the continuous-reset feedback path can easily contribute more than 10e- ENC.**





Pulsed-reset scheme for CSA



- Cf is discharged only during short reset intervals by a switch.

- During reset, the on-state switch (modeled as a resistor) and Cf still introduce **kTC noise!**
- This noise is **sampled** onto Cf and **frozen** after the switch opens
- As a result, it appears mainly as a random post-reset **baseline offset**
  → **"reset noise"**

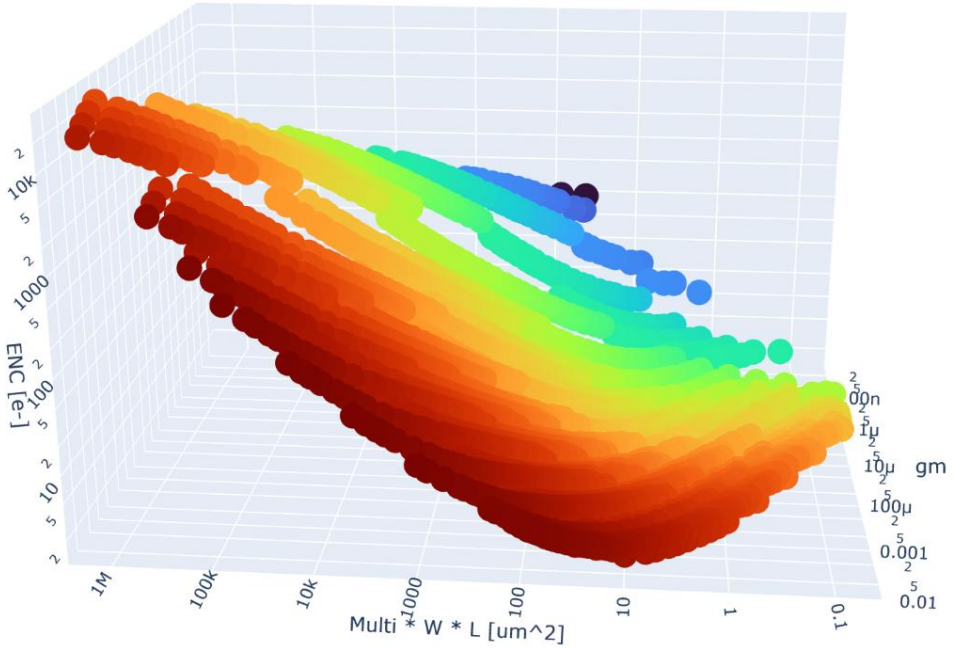
- With **baseline subtraction**, much of this effect can be **removed!**
  → pulsed-reset scheme removes the continuous feedback-resistor noise contribution.

- **The pulsed-reset scheme can be better for achieving few-electron noise**.

- However, if the **off-state leakage current** becomes significant, the circuit starts to deviate from the ideal pulsed-reset picture.

Design Lessons from low-noise CSA Study

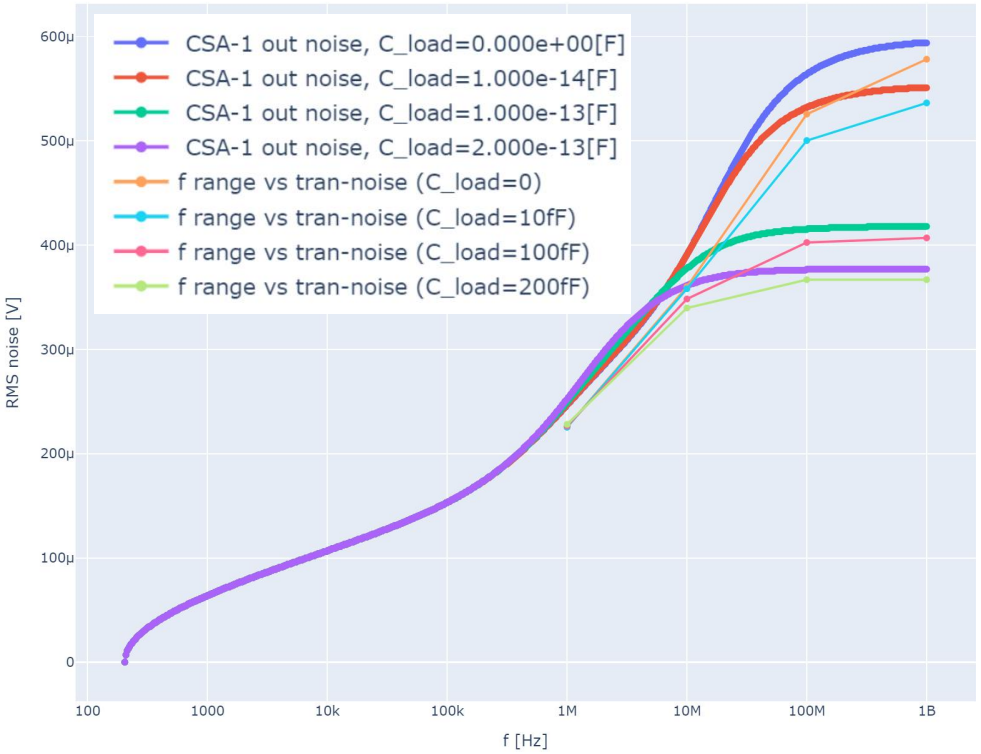
- **Larger input-transistor transconductance (gm) is essential for lowering ENC**, also reduces the input-referred **thermal noise** of the MOS input device.
- However, increasing gm usually requires **more bias current** and therefore **more power**.
- Excessive current is not always beneficial: although it increases gm, it can also **reduce voltage headroom, dynamic range** and **voltage gain**.
- To approach few-electron noise, a **PMOS input transistor** is preferred, mainly because it offers smaller low-frequency noise than NMOS in this process.
- **The input-device capacitance** should be **matched to the detector capacitance**; for a detector capacitance of about 100 fF, the best ENC is obtained when the input-device gate capacitance is of the same order.
- This matching optimum arises because **transistor sizing** changes both the **input capacitance** and the **transconductance** at the same time.

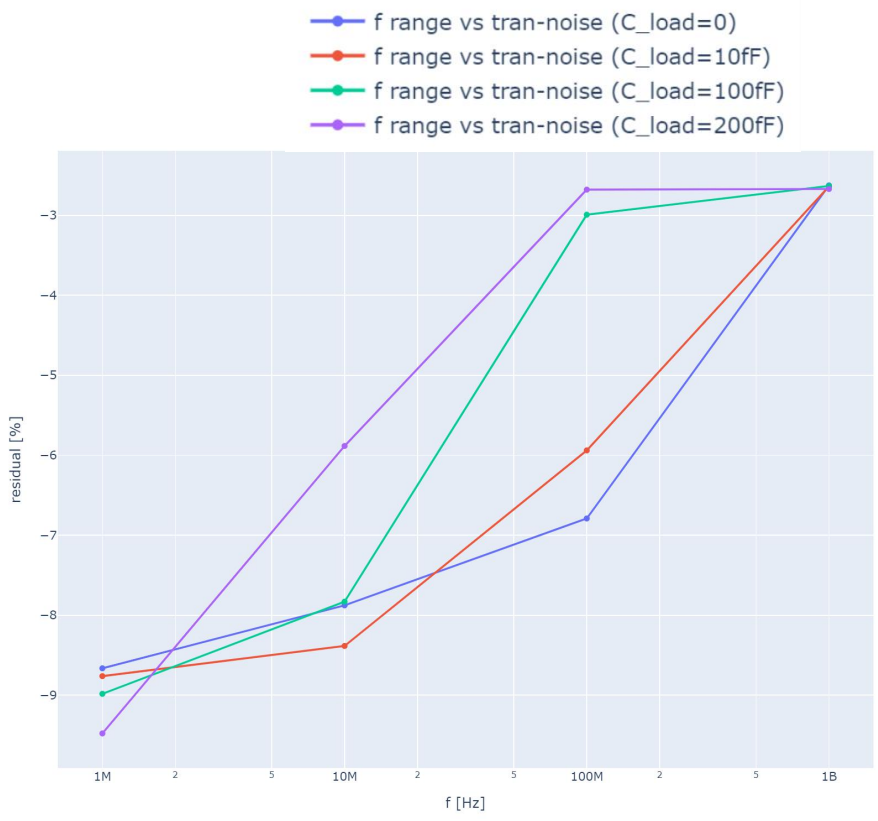


- The optimum is therefore not a single best point, but a **co-optimized** design region, **balancing noise, power, device area, capacitance matching, and practical transistor operating conditions.**

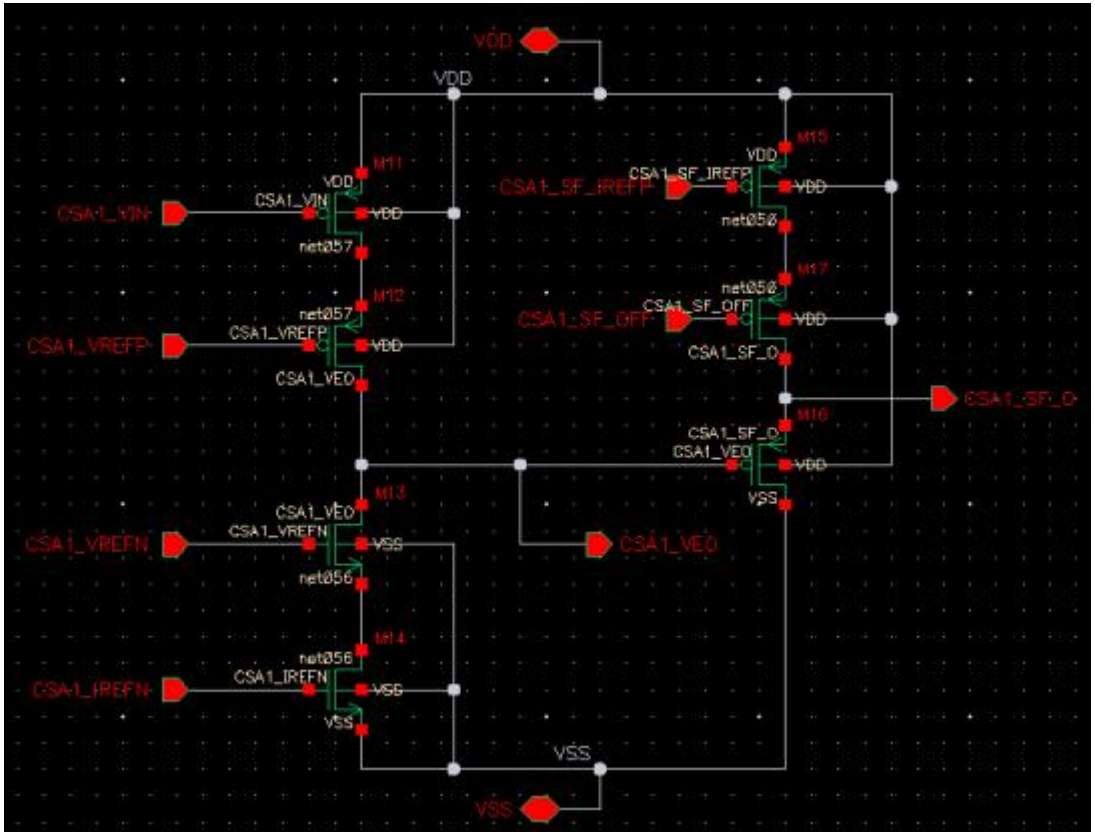
AC noise vs. Transient noise

（tran_noise - ac_noise）/ac_noise <10%,
provided enough integration frequency range

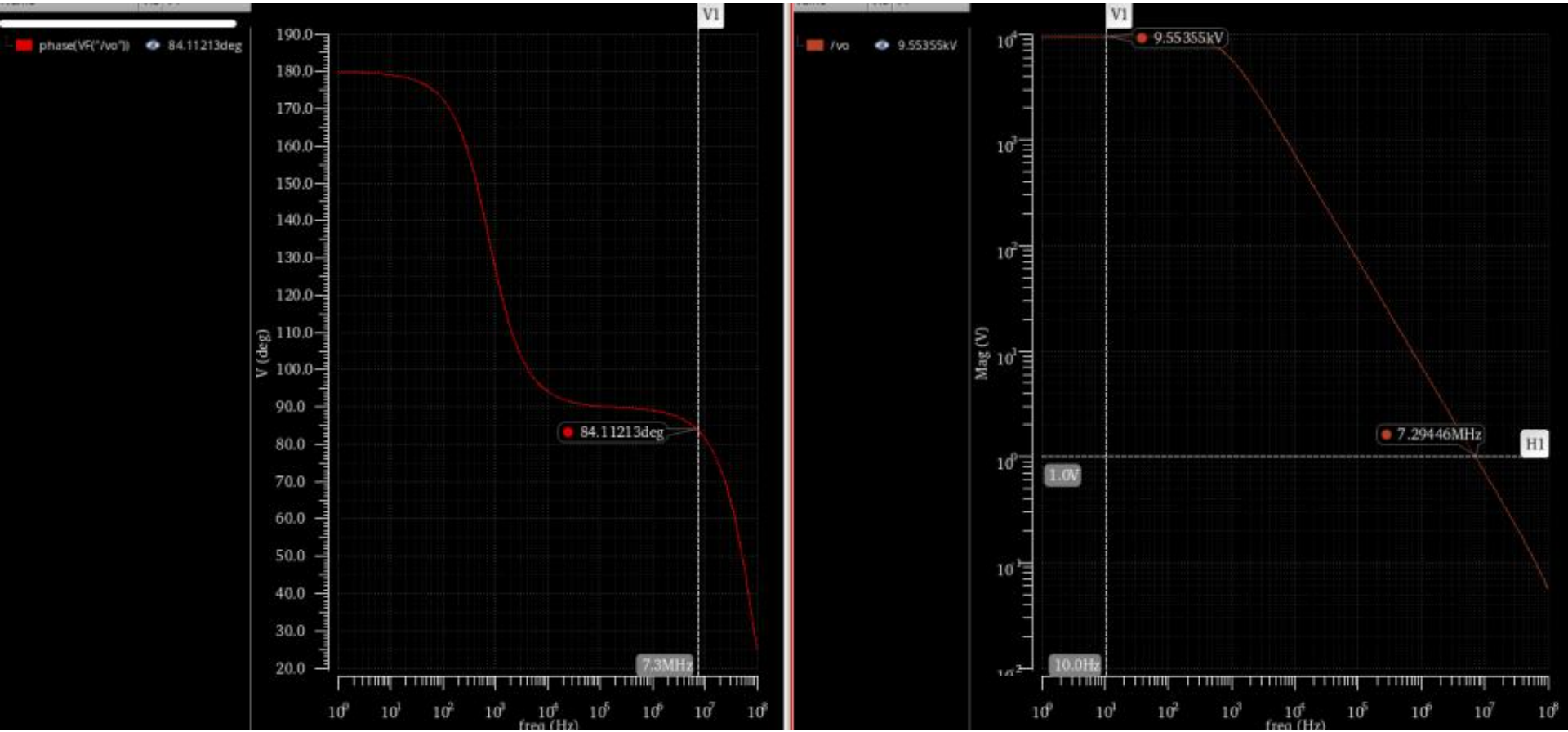




CSA


VDD
VDD
M11
VDD
CSA1_VIN
CSA1_VIN
VDD
net057
M12
net057
CSA1_VREFP
CSA1_VREFP
VDD
CSA1_VEO
M13
CSA1_VEO
CSA1_VREFN
CSA1_VREFN
VSS
net056
M14
net056
CSA1_IREFN
CSA1_IREFN
VSS
VSS
VSS
M15
VDD
CSA1_SF_IREFP
CSA1_SF_IREFP
VDD
net058
M17
net058
CSA1_SF_OFF
CSA1_SF_OFF
VDD
CSA1_SF_O
CSA1_SF_O
M16
CSA1_SF_O
CSA1_VEO
CSA1_VEO
VDD
VSS

Cryogenic Charge Imager CSA AC Response

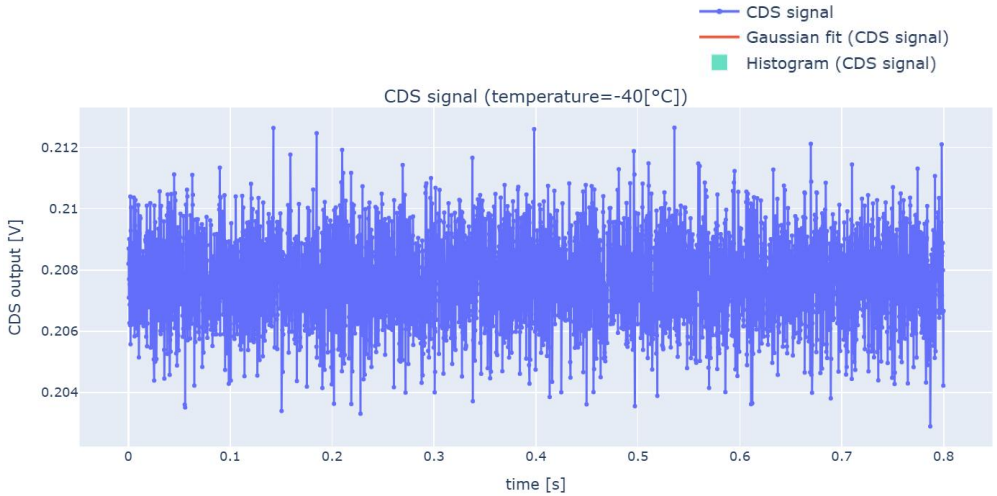


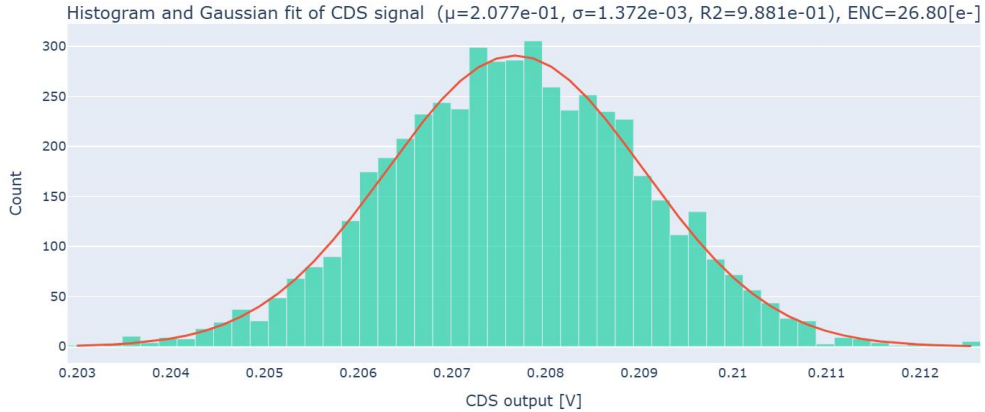
Final Simulated CDS Noise Result

- At the valid CDS **extraction time**, one **CDS output** value is taken from each cycle.
- **upper panel**: **extracted CDS values** versus **time**.
- **lower panel**: **histogram** and **Gaussian fit** of the CDS output.
- The fitted **σ** is converted to **input-referred ENC**, **giving 26.8 e⁻ at -40 °C (28.2 e⁻ at 27°C)**.
- The **preamplifier gain** has already been divided out in this conversion.
- For comparison, the noise of either **sampled path alone** is about **118 e⁻ (CSA reset noise included)**, **which provides an approximation to the noise level without CDS**.

Signal	Sampled path alone	CDS output
ENC at -40 °C	118 [e-]	26.8 [e-]

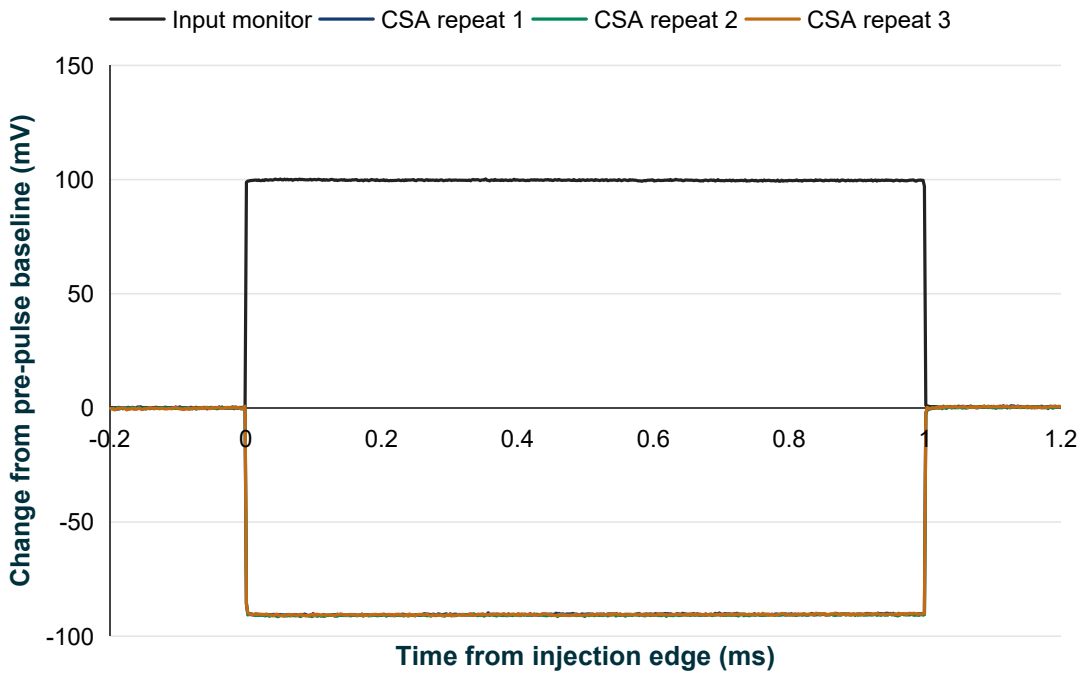
- This comparison shows that **CDS effectively improves the pixel noise performance.**





Backup: Millisecond-Scale Signal Retention in the CSA

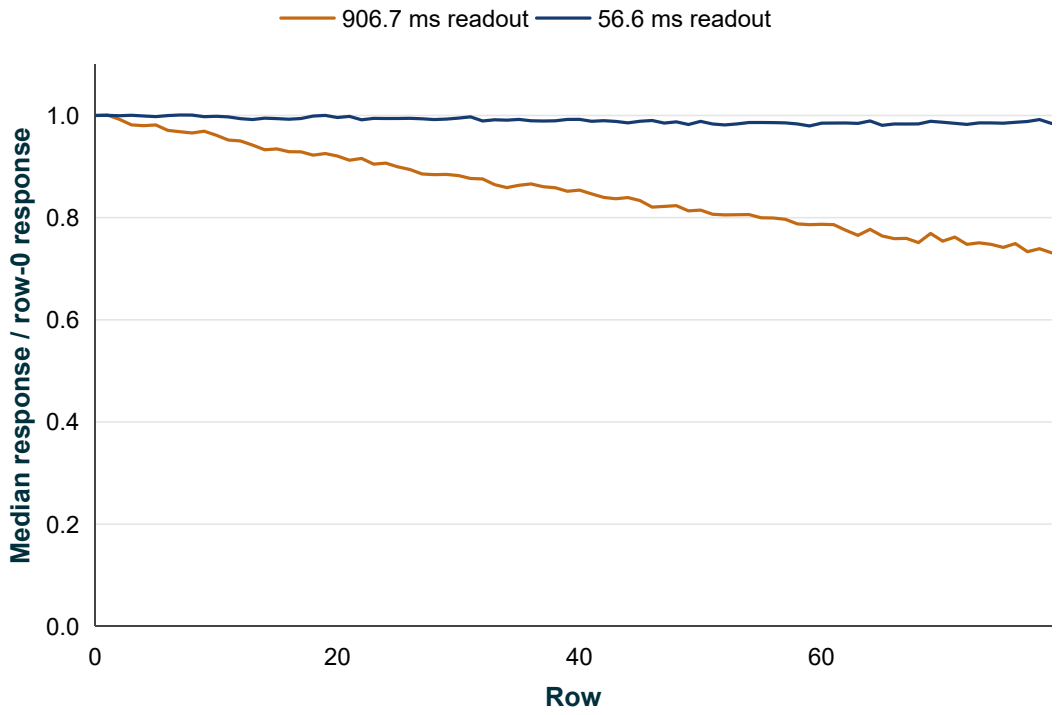
Three repeated responses to a 1 ms injection pulse



- The black trace shows the injection monitor. The colored traces show three repeated CSA responses.
- The pulse produces a voltage step of about **91 mV**. This level remains nearly constant until the pulse returns after **1 ms**.
- From 0.2 to 0.8 ms, the fitted change is **below 0.3 mV** in all three measurements.
- This shows that the **standalone CSA** can retain the injected signal on a millisecond time scale.

ASIC #4 CSA test structure. 1× external buffer. This measurement concerns the CSA, not the CDS storage capacitors.

Readout Time and Stored-Signal Stability



- Each frame uses one pair of **global CDS samples**, followed by sequential scanning.
- The orange curve uses a **906.7 ms** frame readout. The blue curve uses a **56.6 ms** readout.
- Each curve shows the row median divided by the response of its own first row.
- The faster scan greatly reduces the **row-dependent response variation**, consistent with shorter analog hold times.

ASIC #5. Both curves use the same 6,397-pixel selection. Readout durations exclude host transfer.