An Open-Source Waveform Digitizer ASIC

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Outline

- Project overview
- Initial design target
  - Circuit design
  - Simulation results
- Design methodology
  - Digital on top flow using open-source tools
  - AI-assisted design with human in the loop
- Project status



Why Open Source?

Proprietary PDK e.g. IRSX, 250 nm

NDA: needed even inside one collaboration

Queue: small academic orders wait

Cost: each iteration is expensive

Closed: design files cannot be published

Open PDK and open tools GF180MCU

Share: whole design public, Apache 2.0

Review: anyone can check every file

Cost: ≈ $6k per design on a shuttle

Port: same flow on newer open nodes

Goal: a waveform-sampling ASIC anyone can read, rebuild and modify

Open PDK also allows AI tools in the flow, used as a tool under human review

Approach and Staged Plan

Open process

GF180MCU open PDK
180 nm, 3.3 V, MIM caps

Low-cost shuttle

wafer.space
≈ $6k → ~1,000 dies,
chip-on-board

Public repository

github.com/sykeisuke/asic_rd
Apache 2.0, open to all

Nightly build: full chip rebuilt from scratch, DRC + LVS, ~30 min → always ready to submit

Staged plan

Tape-out 1

flow-flush design
1 channel × 4 cells, 8 bit,
20 MSa/s

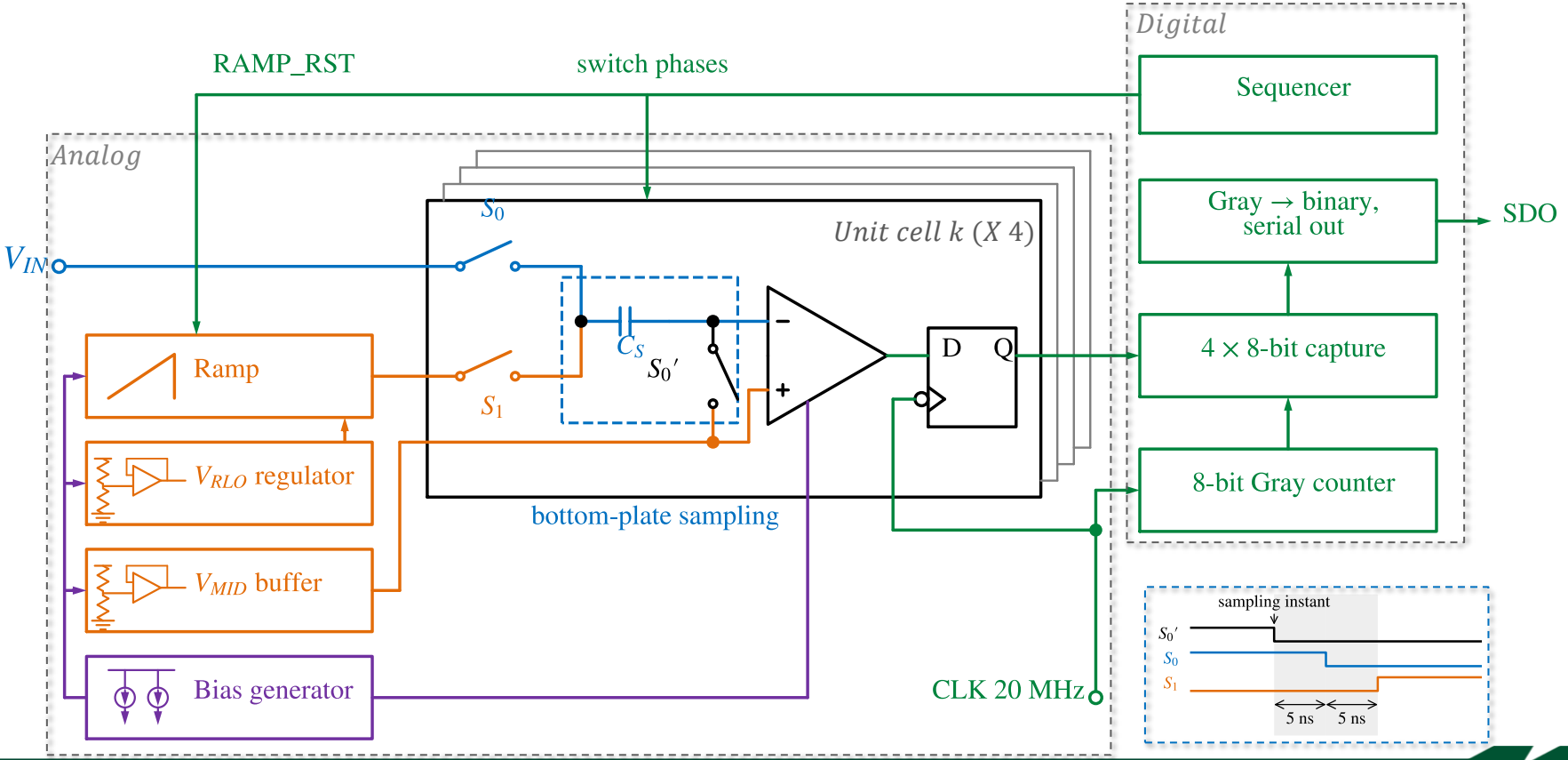
Tape-out 2

more cells and channels
smaller comparator

IRSX class

32,768 cells, 12 bit
many channels

Tape-out 1: Architecture

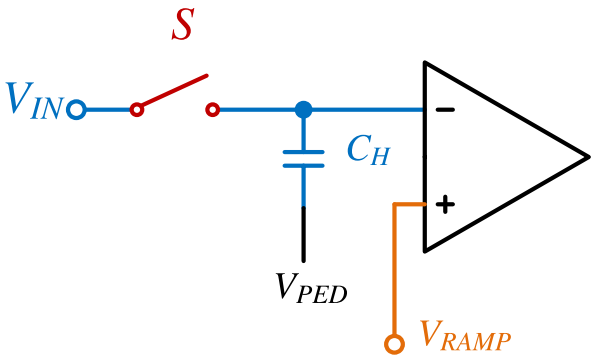


Tape-out 1: Spec vs IRSX

	IRSX (reference)	Tape-out 1 (this work)
Process/supply	–	GF180MCU, 3.3 V devices
Channels × cells	32 768 cells (16 × 32 × 64)	1 × 4
Hold capacitor	14 fF	54.5 fF MIM (5 µm × 5 µm)
Sampling	top-plate, 2.2 GSa/s	bottom-plate, 20 MSa/s (50 ns)
Analog bandwidth	500 MHz	> 10 MHz measurement target
ADC	12-bit Wilkinson	8-bit Wilkinson, 0.5–2.0 V (5.86 mV LSB)
Clock / conversion	–	20 MHz clock / 256 counts = 12.8 µs
Noise target	–	0.25 LSB rms (ENOB > 7)
Static power (sim., AVDD)	–	755 µW
Readout		4 × 8-bit Gray capture, serial

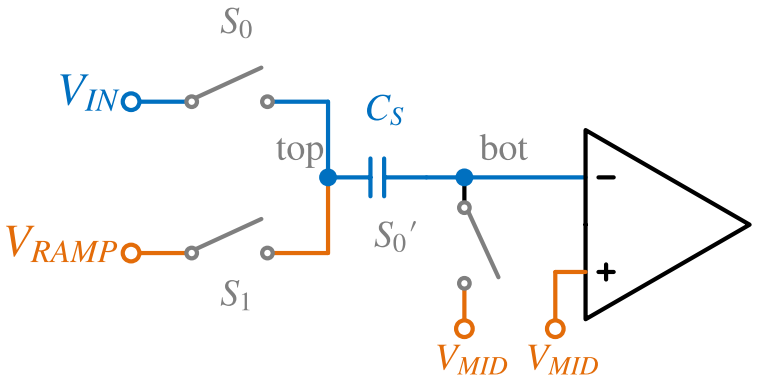
Sampling Unit Cell: Top vs Bottom Plate Sampling

Top-plate sampling (IRSX)



S opens on V_{IN}:
charge injection depends
on the signal

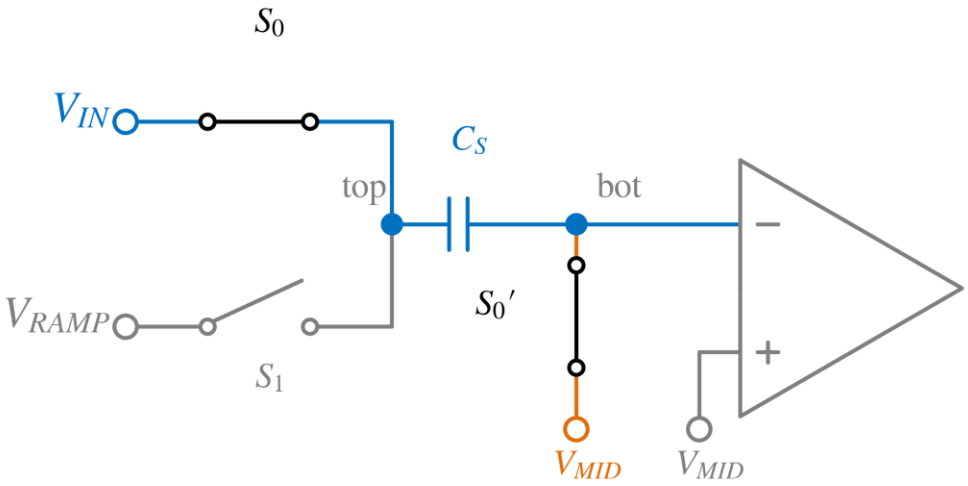
Bottom-plate sampling (this work)

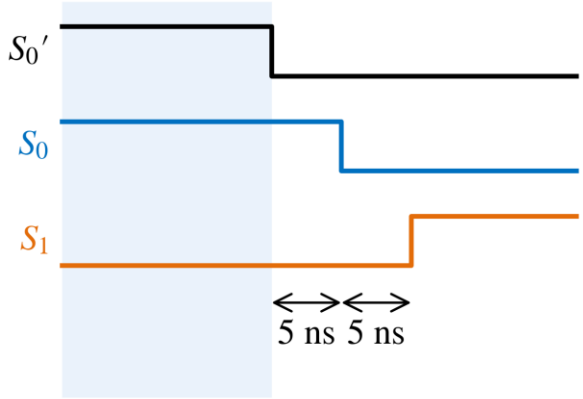


S_0' opens first, always at V_{MID}:
constant injection = one offset per cell
trips at $V_{RAMP} = V_{IN} - V_{PED}/\alpha$

Sampling Unit Cell: Bottom Plate Sampling

1 Track | 2 Sample | 3 Isolate | 4 Convert



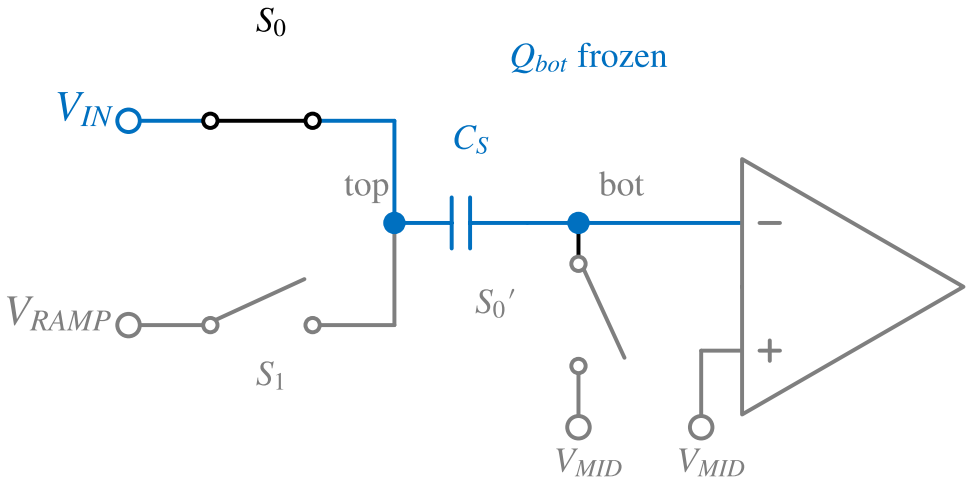


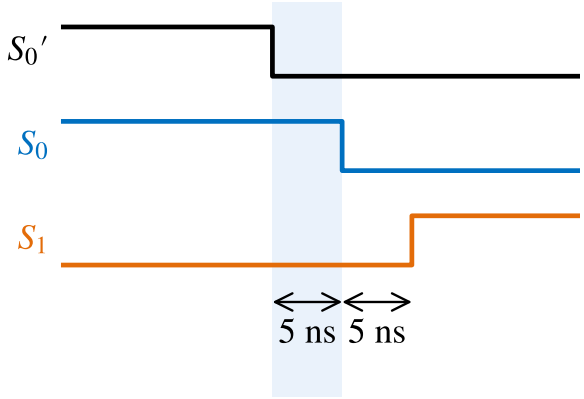
S_0 and S_0' closed: $V_{top} = V_{IN}$, $V_{bot} = V_{MID}$

C_S follows the input

Sampling Unit Cell: Bottom Plate Sampling

1 Track | **2 Sample** | 3 Isolate | 4 Convert



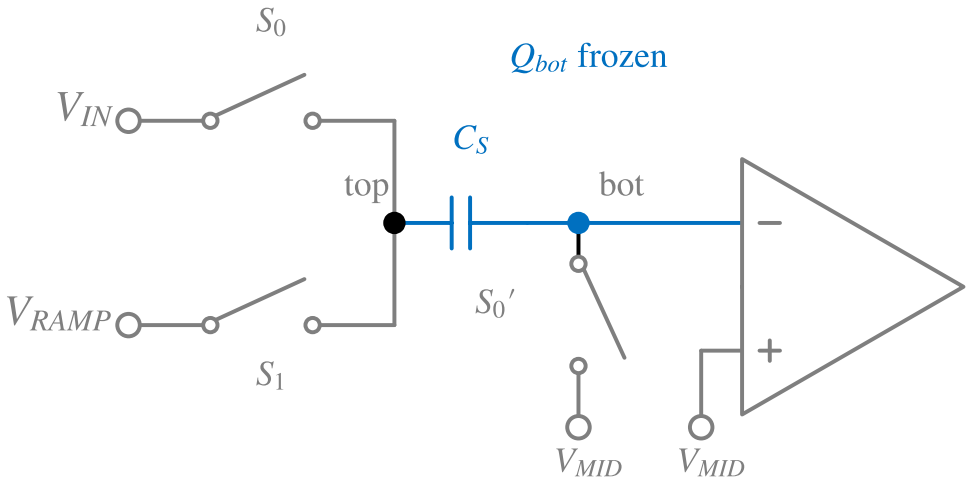


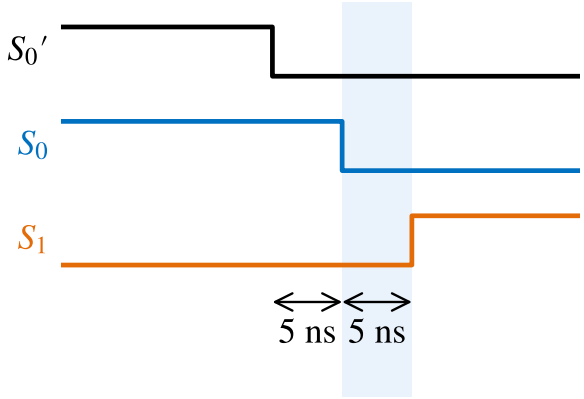
S_0' opens = sampling instant: $Q_{bot0} = C_S\,(V_{MID} - V_{IN}) + C_{parasitic}\,V_{MID} + Q_{ped}$

Q_{ped}: charge injected by S_0'; later changes in V_{IN} cannot alter Q_{bot0}

Sampling Unit Cell: Bottom Plate Sampling

1 Track | 2 Sample | **3 Isolate** | 4 Convert



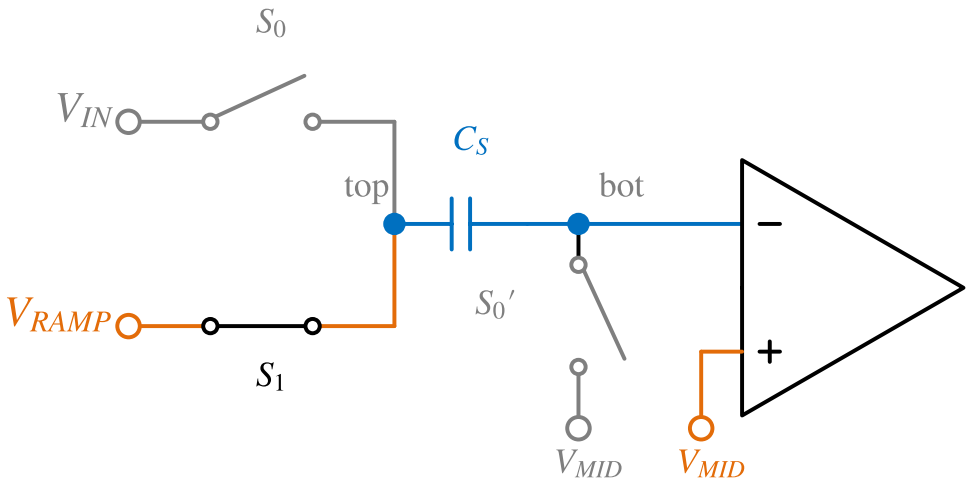


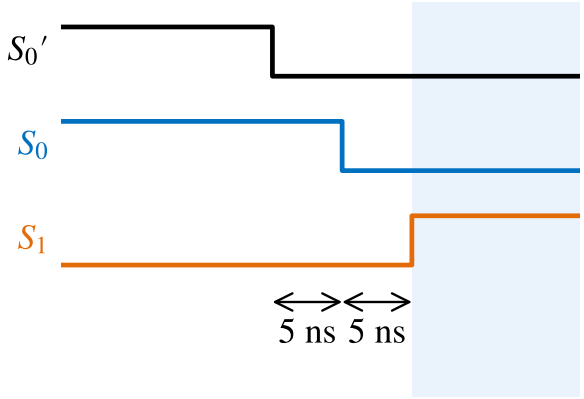
S_0 opens: the top plate leaves V_{IN}; Q_{bot0} stays frozen on the bottom plate

both plates float; the charge cannot leave the bottom plate

Sampling Unit Cell: Bottom Plate Sampling

1 Track | 2 Sample | 3 Isolate | **4 Convert**





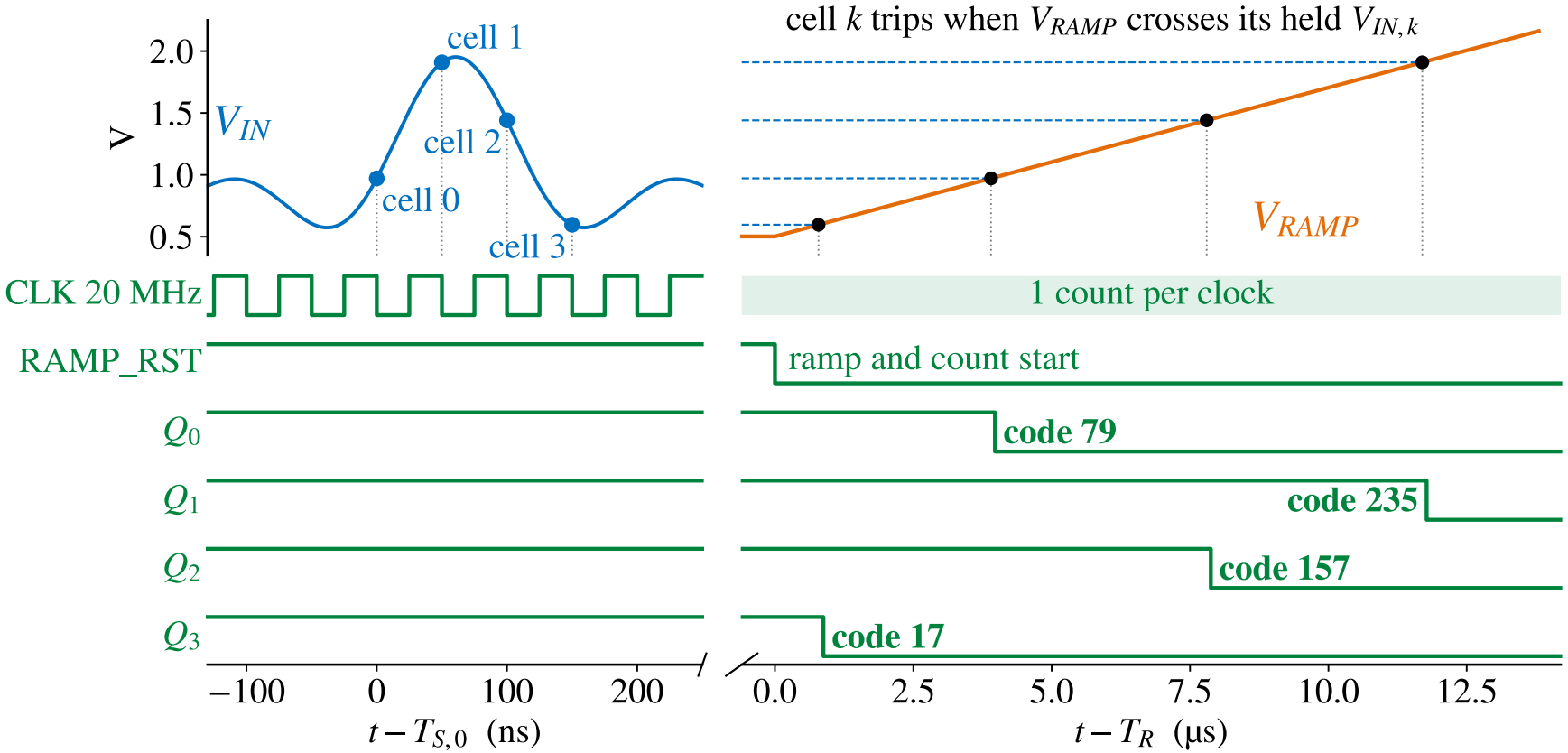
S_1 closes, the ramp drives the top plate: $Q_{bot1} = C_S\,(V_{bot} - V_{RAMP}) + C_{parasitic}\,V_{bot}$

Charge conservation at bot, $Q_{bot1} = Q_{bot0} \Rightarrow V_{bot} = V_{MID} + V_{PED} + \alpha\,(V_{RAMP} - V_{IN})$

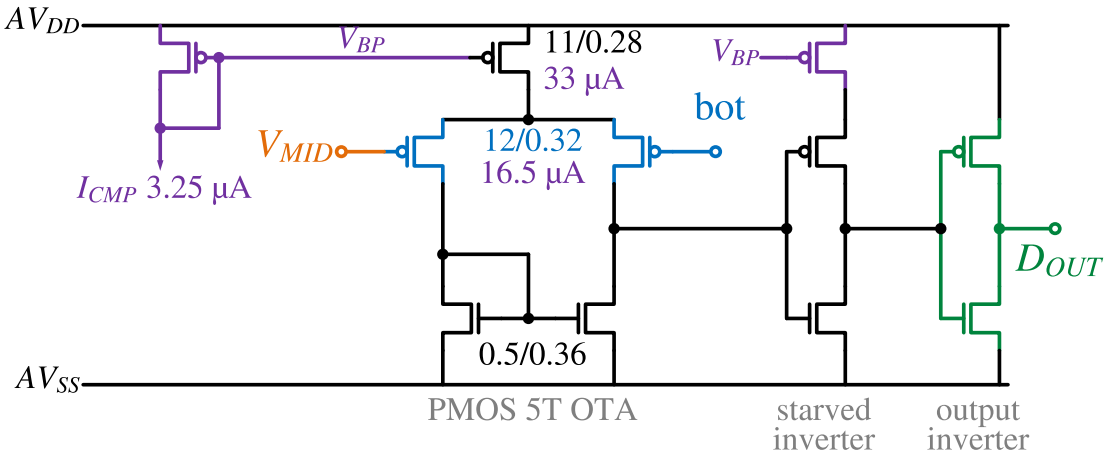
where $\alpha = C_S / (C_S + C_{parasitic})$, $V_{PED} = Q_{ped} / (C_S + C_{parasitic})$

comparator trips at $V_{RAMP} = V_{IN} - V_{PED}/\alpha$, the same offset for every input

Sampling Phases: Timing Diagram

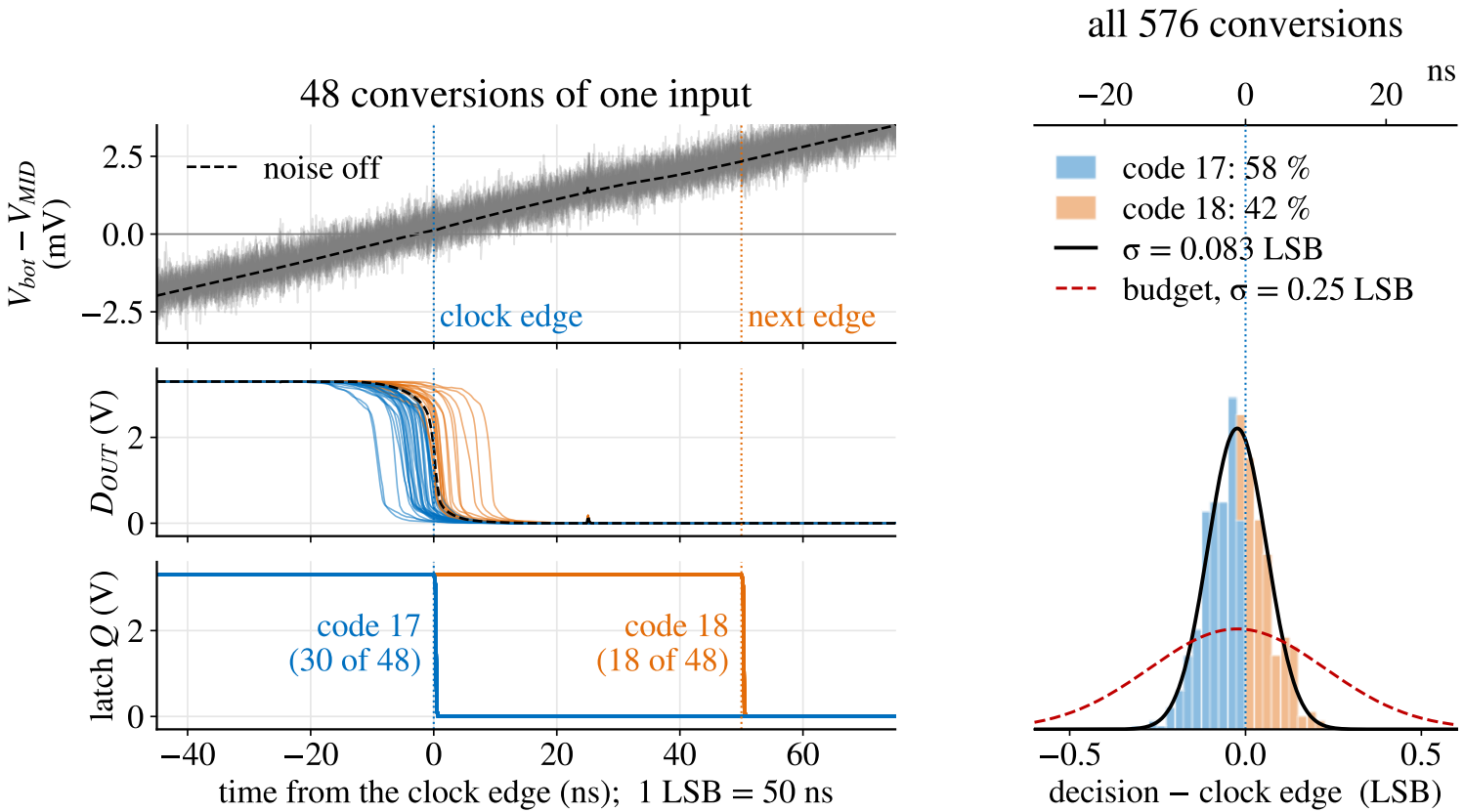


Comparator

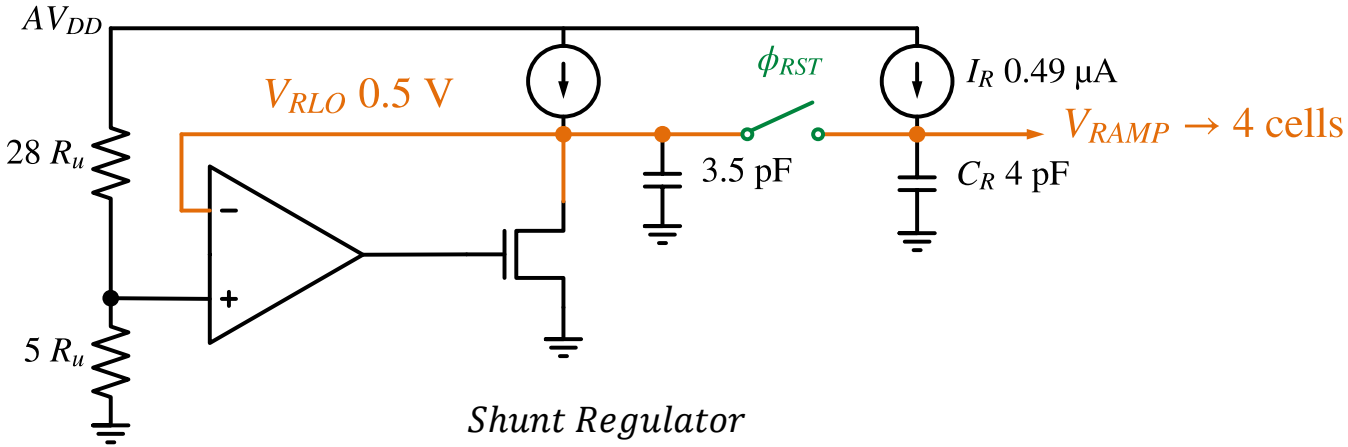


	Spec	Simulated (135 PVT)
$Delay$	$\leq$ 12.5 ns (1/4 LSB)	$\leq 11.6\ ns$
$Noise$	$\leq 0.08\ LSB$	$0.036\ LSB$ (VACASK Transient)
$Gain$	$> 60\ dB$	$\geq 89\ dB$
$\sigma(V_{OS})$	–	$2.1\ LSB$
$Power$	–	$110\ \mu W$
$Area$	–	$39.4\ \mu m^2$

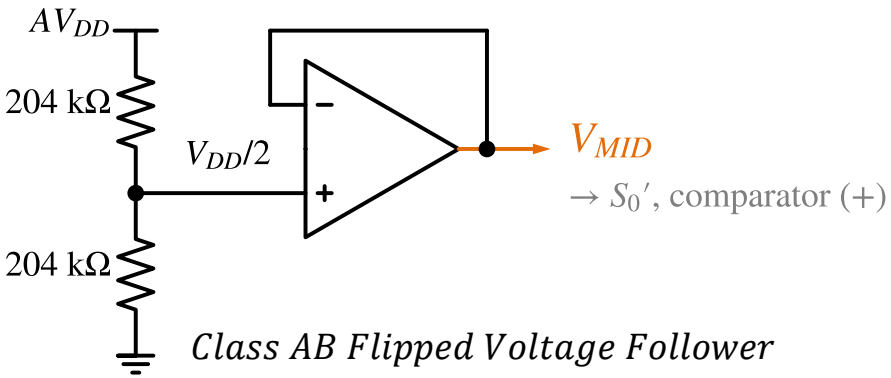
VACASK Noise Sim: Ramp + Unit Cell



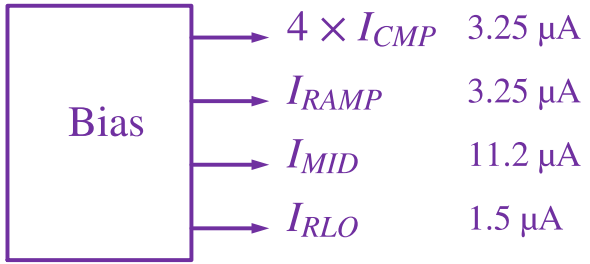
Reference, Ramp, and Bias Design



Shunt Regulator

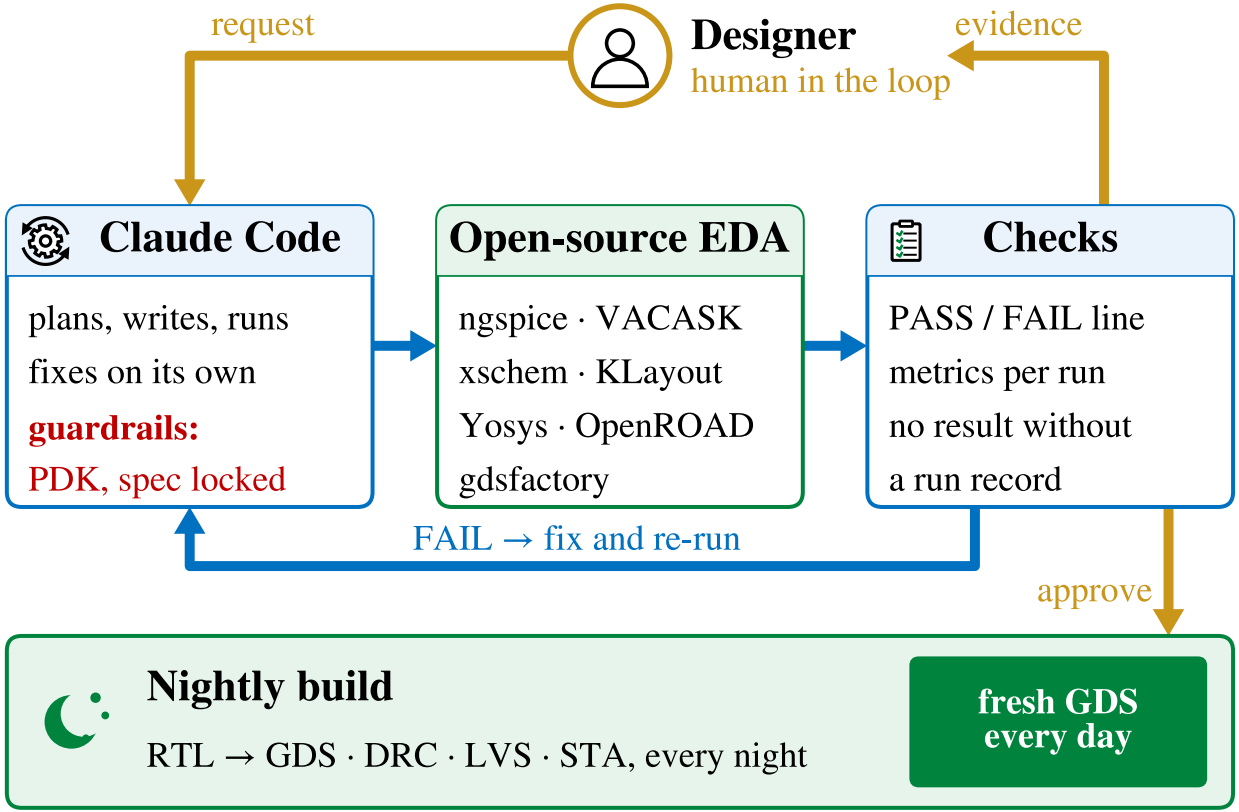


Class AB Flipped Voltage Follower



Constant − g_m Bias Generator

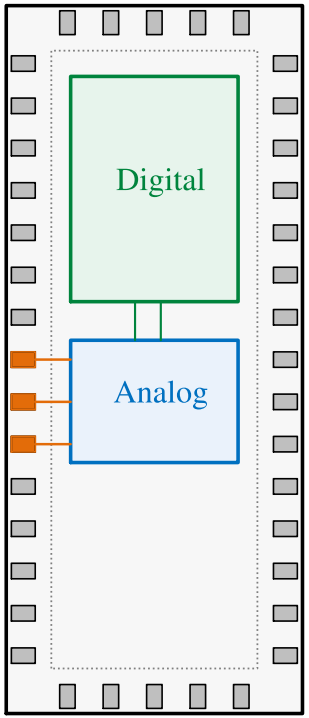
An AI-Assisted Design with Human in the Loop



Open source makes it possible

- ✓ Open PDK
- ✓ Free, scriptable tools
- ✓ Text sources in git
- ✓ Pinned container
- ✓ Two open simulators
- ✓ Open shuttle template

Digital on Top Flow



pad ring + seal from the template

wafer.space template
pad ring, slot size, pad order

↓

chip_top.sv
digital top + analog macros wired

↓

macros.py
analog GDS → hard macro (LEF, pins)

↓

LibreLane: Yosys + OpenROAD
synthesis, placement, routing

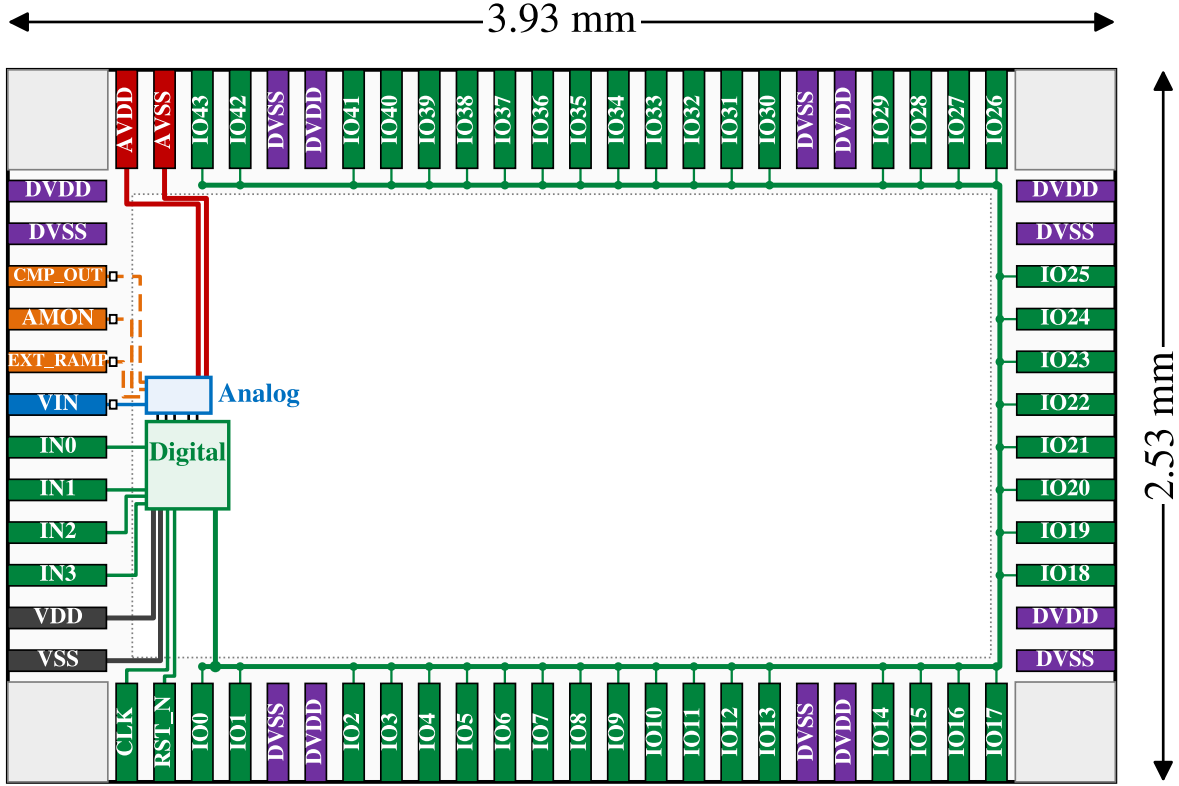
↓

analog_routes.tcl
the 5 analog pad-to-macro wires

↓

Sign-off
DRC · LVS · antenna · density · XOR

Chip Top

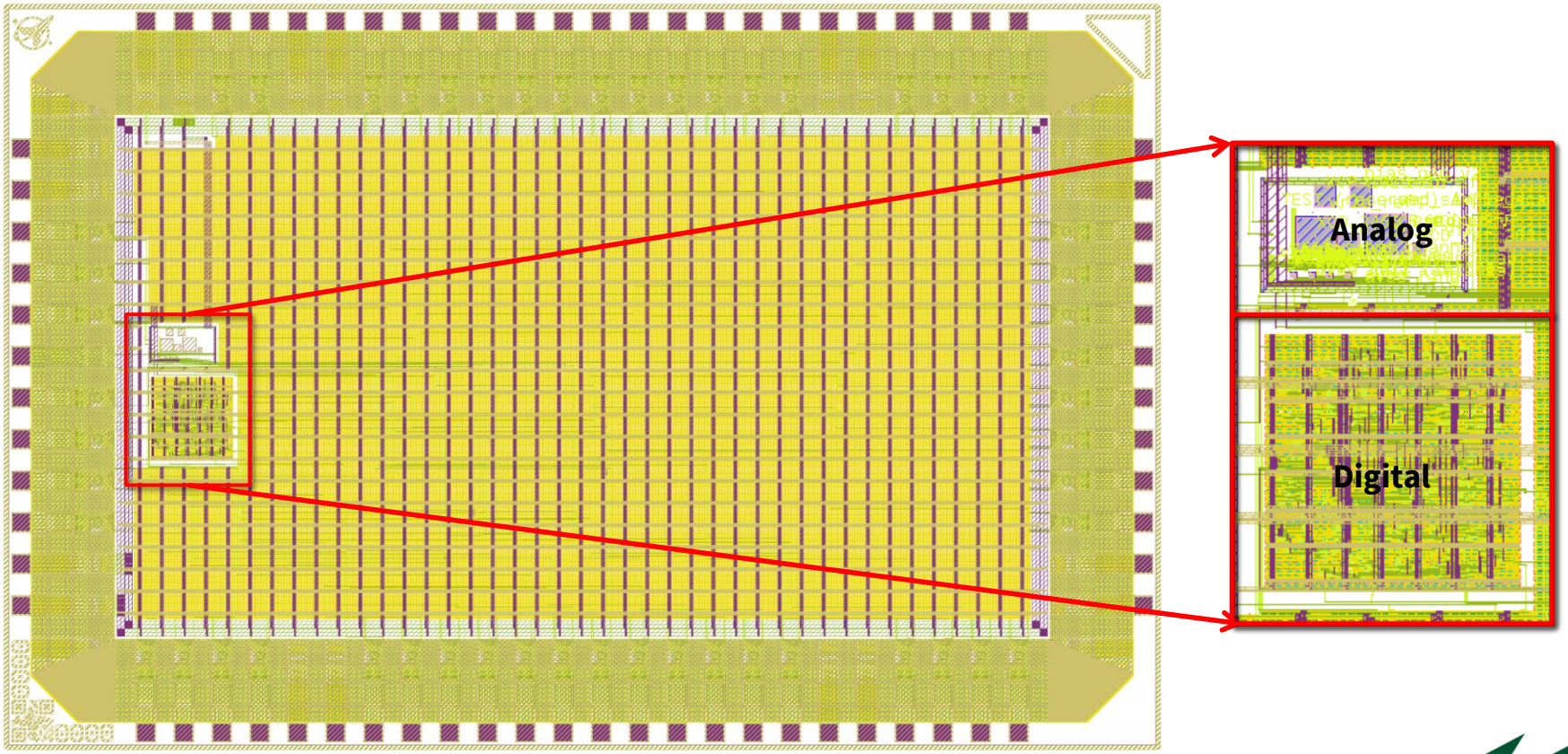


72 pads

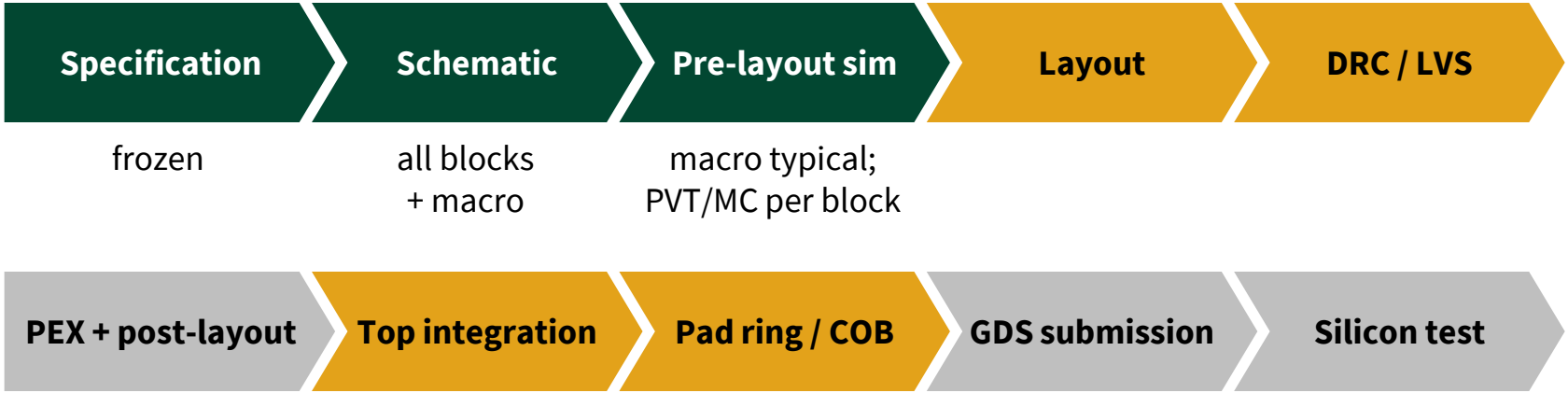
- signal input
- analog test
- analog supply
- digital
- core supply
- I/O supply
- secondary ESD

Analog 229 × 127 µm
Digital 292 × 310 µm

Top View of Current Chip



Progress So Far



done (run artifact) partial / demo open

~12 weeks to clean GDS

Open-source tools: xschem · ngspice · VACASK · KLayout · Yosys · OpenROAD · LibreLane · gdsfactory

Summary

Chip design, open to anyone: no NDA, no license fees, no gatekeepers



Limitless scope

Open-source EDA tools

Public repository

Agile, software-like flow



AI-assisted design

AI-friendly open tools

Agents do the rigorous tasks

Humans verify and guide



Global collaboration

No NDA: anyone can join

Every file open to review

Ports to newer open nodes

github.com/sykeisuke/asic_rd

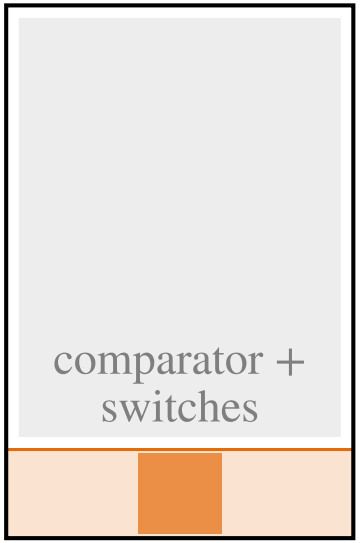


GitHub Repo



github.com/sykeisuke/asic_rd

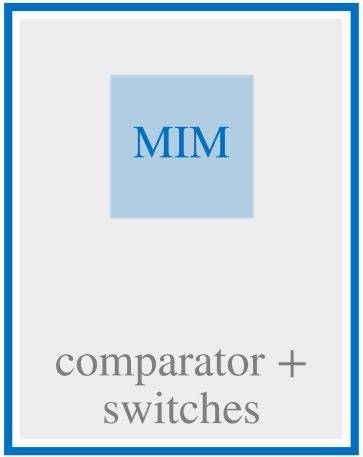
Hold Capacitor Choice



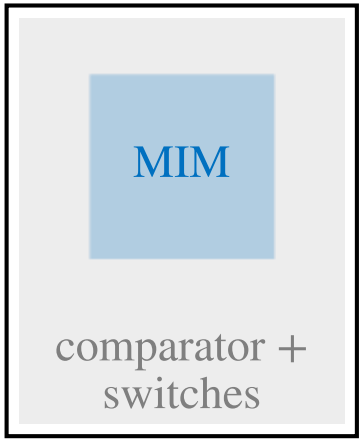
+126 µm²

MOM 15.6 fF
(M1–M4, beside)
cell 753 µm²
kT/C noise 0.088 LSB

chosen

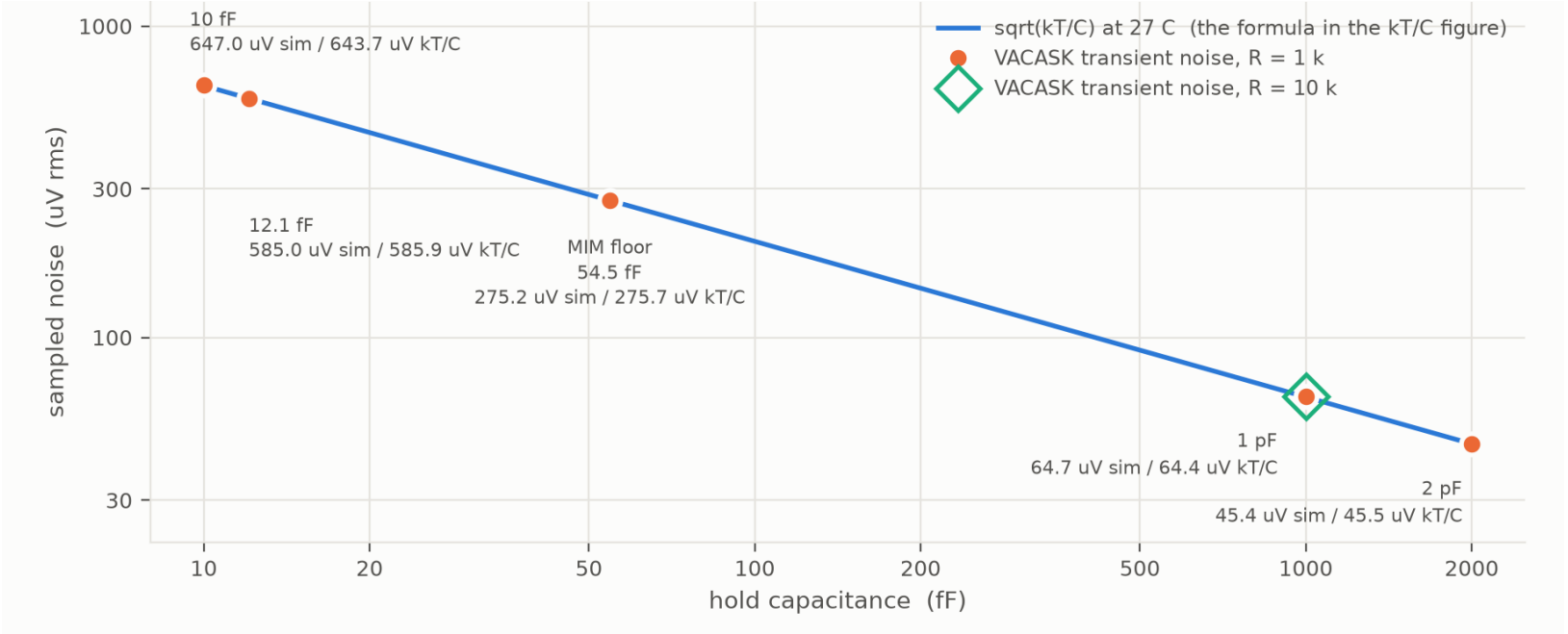


MIM 54.5 fF
(M4/M5, on top)
cell 627 µm²
kT/C noise 0.047 LSB

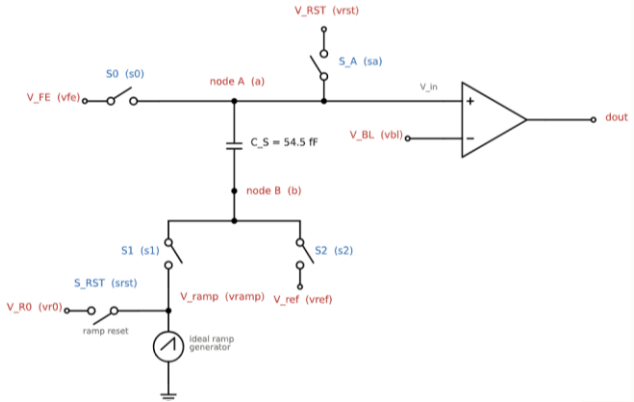


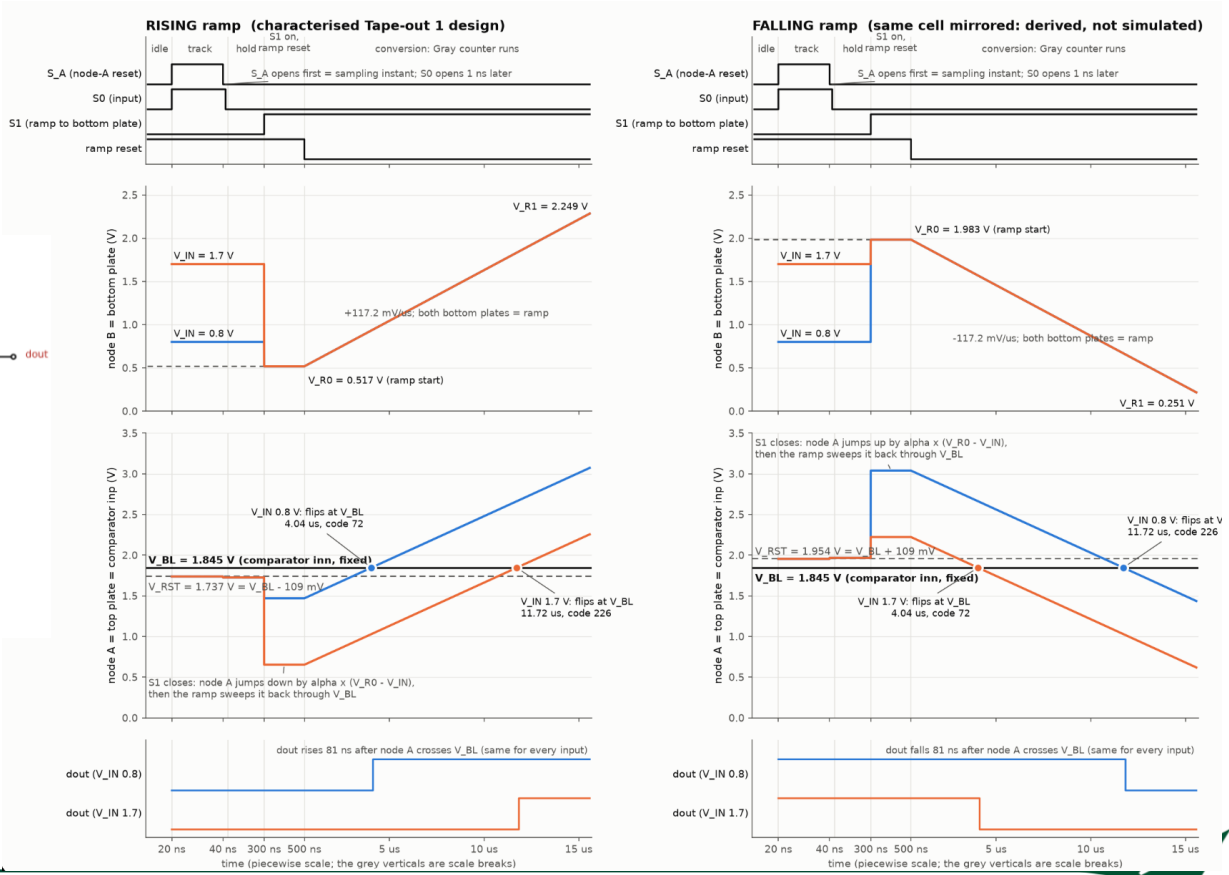
MIM 125 fF
(M4/M5, on top)
cell 614 µm²
kT/C noise 0.031 LSB

Cap vs kt/C noise: Verified with VACASK Tran noise sim

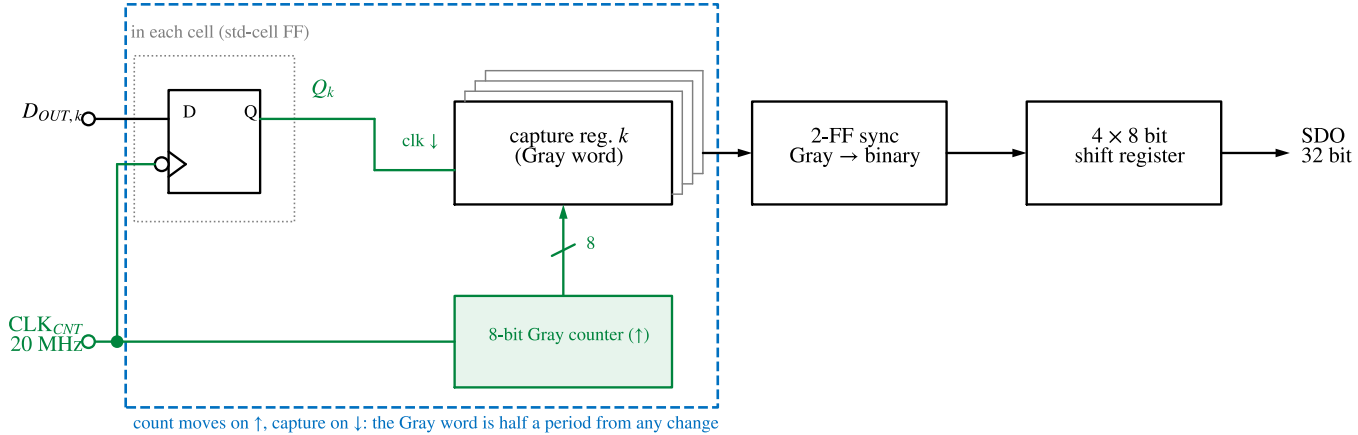


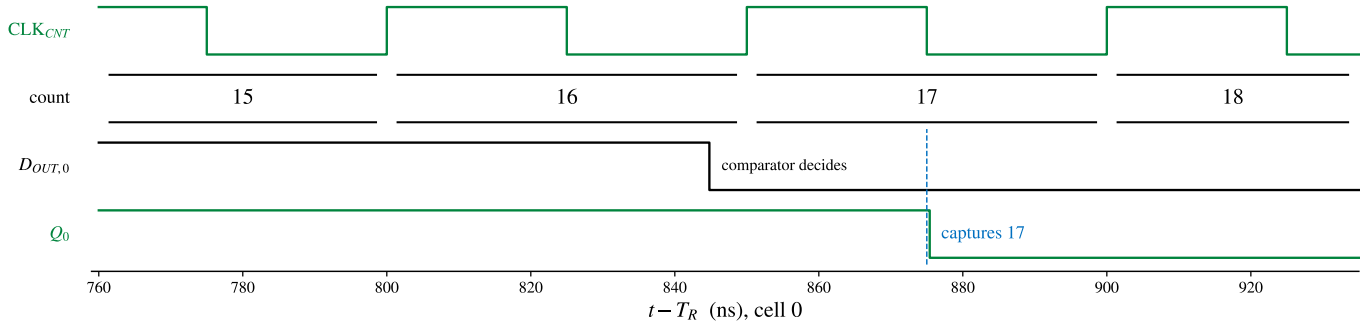
Bottom-plate sampling: Working and ramp



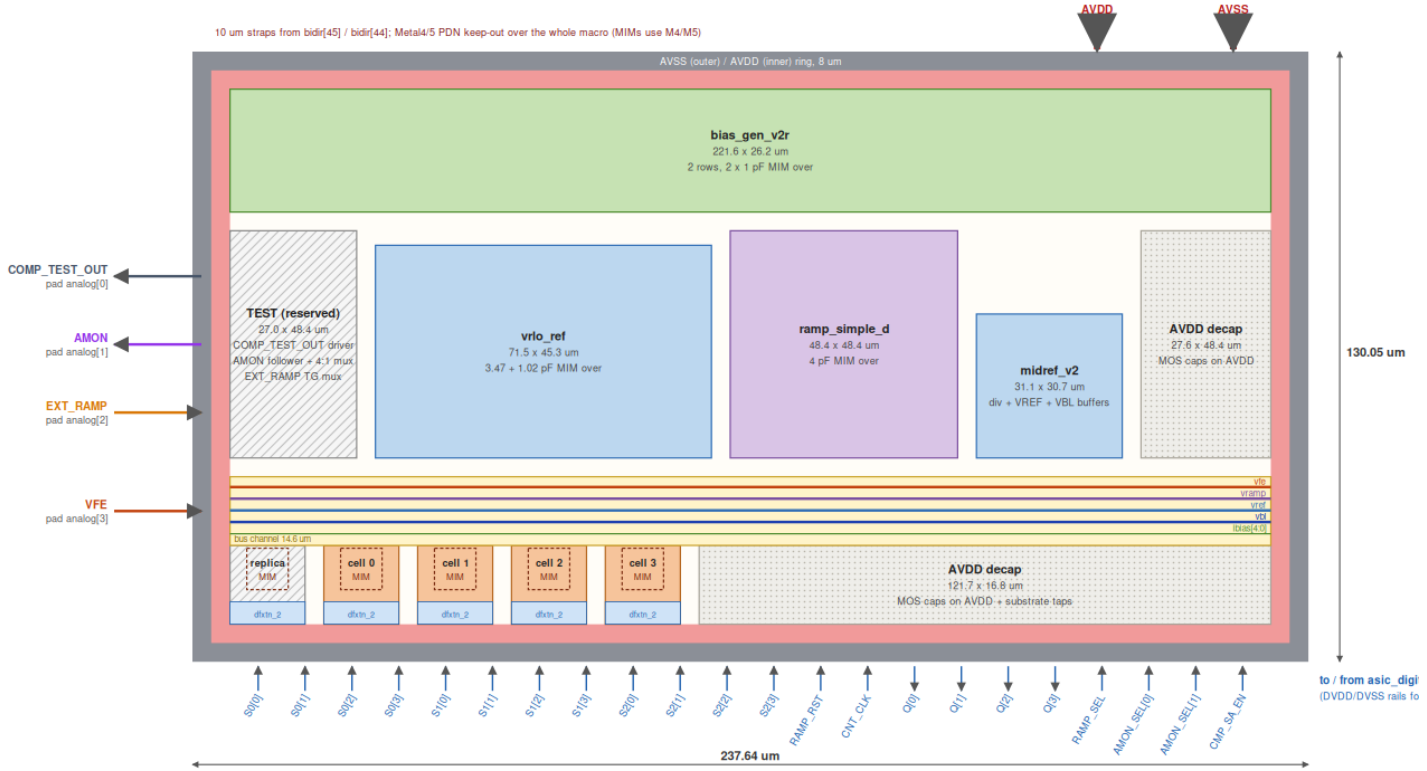


Digital Design

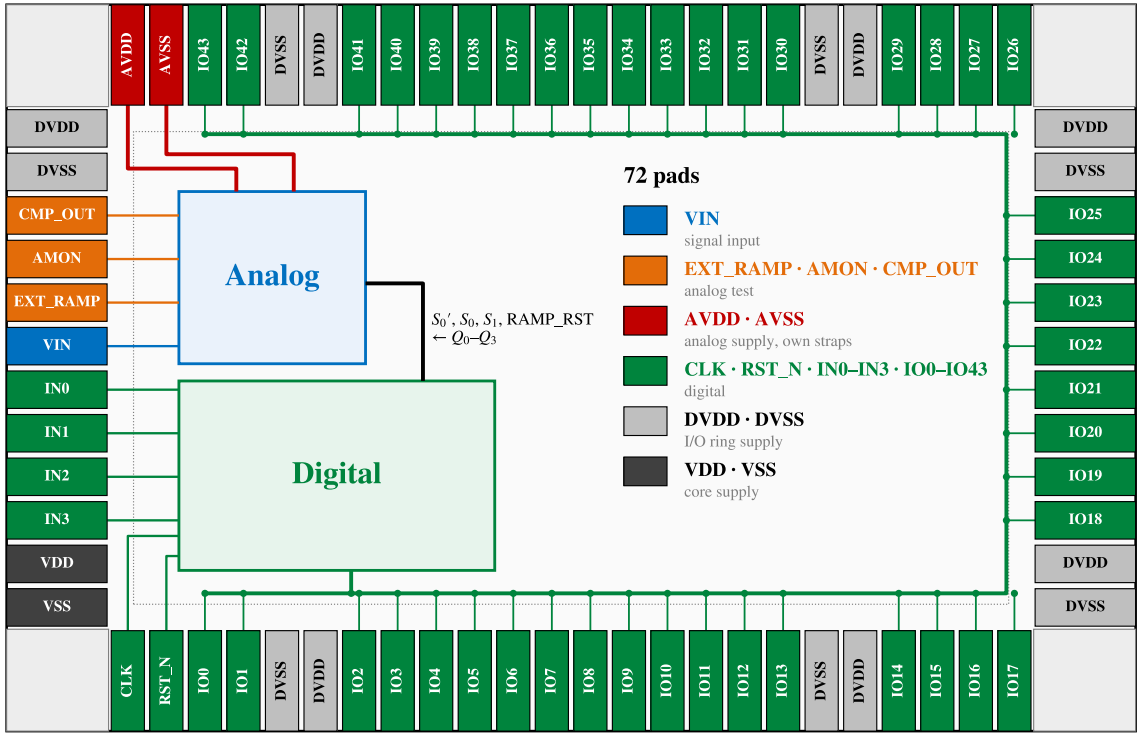




Analog Top


10 um straps from bidir[45] / bidir[44]; Metal4/5 PDN keep-out over the whole macro (MIMs use M4/M5)
AVDD
AVSS
AVSS (outer) / AVDD (inner) ring, 8 um
bias_gen_v2r
221.6 x 26.2 um
2 rows, 2 x 1 pF MIM over
COMP_TEST_OUT
pad analog[0]
AMON
pad analog[1]
EXT_RAMP
pad analog[2]
VFE
pad analog[3]
TEST (reserved)
27.0 x 48.4 um
COMP_TEST_OUT driver
AMON follower + 4:1 mux
EXT_RAMP TG mux
vrlo_ref
71.5 x 45.3 um
3.47 + 1.02 pF MIM over
ramp_simple_d
48.4 x 48.4 um
4 pF MIM over
midref_v2
31.1 x 30.7 um
div + VREF + VBL buffers
AVDD decap
27.6 x 48.4 um
MOS caps on AVDD
130.05 um
vfb
vramp
vref
vbl
ibias[4:0]
bus channel 14.6 um
replica
MIM
cell 0
MIM
cell 1
MIM
cell 2
MIM
cell 3
MIM
dfxtn_2
AVDD decap
121.7 x 16.8 um
MOS caps on AVDD + substrate taps
S0[0]
S0[1]
S0[2]
S0[3]
S1[0]
S1[1]
S1[2]
S1[3]
S2[0]
S2[1]
S2[2]
S2[3]
RAMP_RST
CNT_CLK
Q[0]
Q[1]
Q[2]
Q[3]
RAMP_SEL
AMON_SEL[0]
AMON_SEL[1]
CMP_SA_EN
237.64 um
to / from asic_digi
(DVDD/DVSS rails fo

Chip Top


AVDD
AVSS
IO43
IO42
DVSS
DVDD
IO41
IO40
IO39
IO38
IO37
IO36
IO35
IO34
IO33
IO32
IO31
IO30
DVSS
DVDD
IO29
IO28
IO27
IO26
DVDD
DVSS
CMP_OUT
AMON
EXT_RAMP
VIN
IN0
IN1
IN2
IN3
VDD
VSS
Analog
Digital
S_0', S_0, S_1, RAMP_RST
← Q_0–Q_3
72 pads
VIN
signal input
EXT_RAMP · AMON · CMP_OUT
analog test
AVDD · AVSS
analog supply, own straps
CLK · RST_N · IN0–IN3 · IO0–IO43
digital
DVDD · DVSS
I/O ring supply
VDD · VSS
core supply
DVDD
DVSS
IO25
IO24
IO23
IO22
IO21
IO20
IO19
IO18
DVDD
DVSS
CLK
RST_N
IO0
IO1
DVSS
DVDD
IO2
IO3
IO4
IO5
IO6
IO7
IO8
IO9
IO10
IO11
IO12
IO13
DVSS
DVDD
IO14
IO15
IO16
IO17

Comparator Sizing Choice

