Cryogenic Front-End ASICs in 65 nm CMOS for Low-Noise Readout of Charge or Light Signals in Noble Liquid Detectors

Prashansa Mukim (on behalf of the BNL Cold Electronics Team)

Contributions: Shanshan Gao, Gabriella Carini, Hucheng Chen, Grzegorz Deptuch, Jack Fried, Niccolo' Gallice, Dominik Gorni, Lingyun Ke, Wenrui Lin, Giovanni Pinaroli, Don Pinelli, Joe Pinz, Sergio Rescia, Antonio Verderosa, Chao Zhang

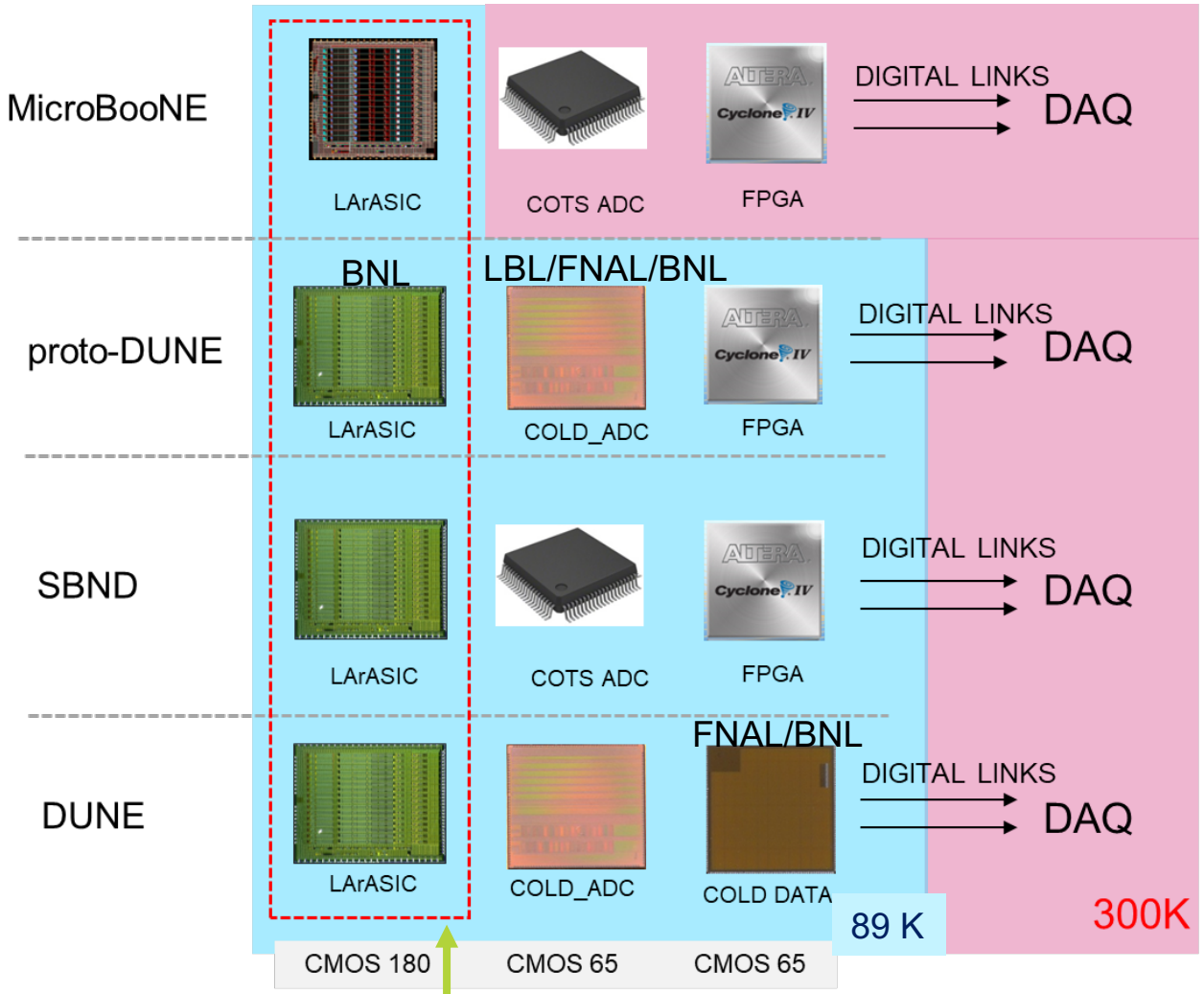
October 22, 2026

CPAD Workshop, Seattle

@BrookhavenLab

BNL Cryogenic Front-end ASICs

About a decade of development



Peaking time programmable between 500 ns and 3 µs

To meet the demands of next generation experiments -> cryogenic front-end ASICs in 65 nm CMOS

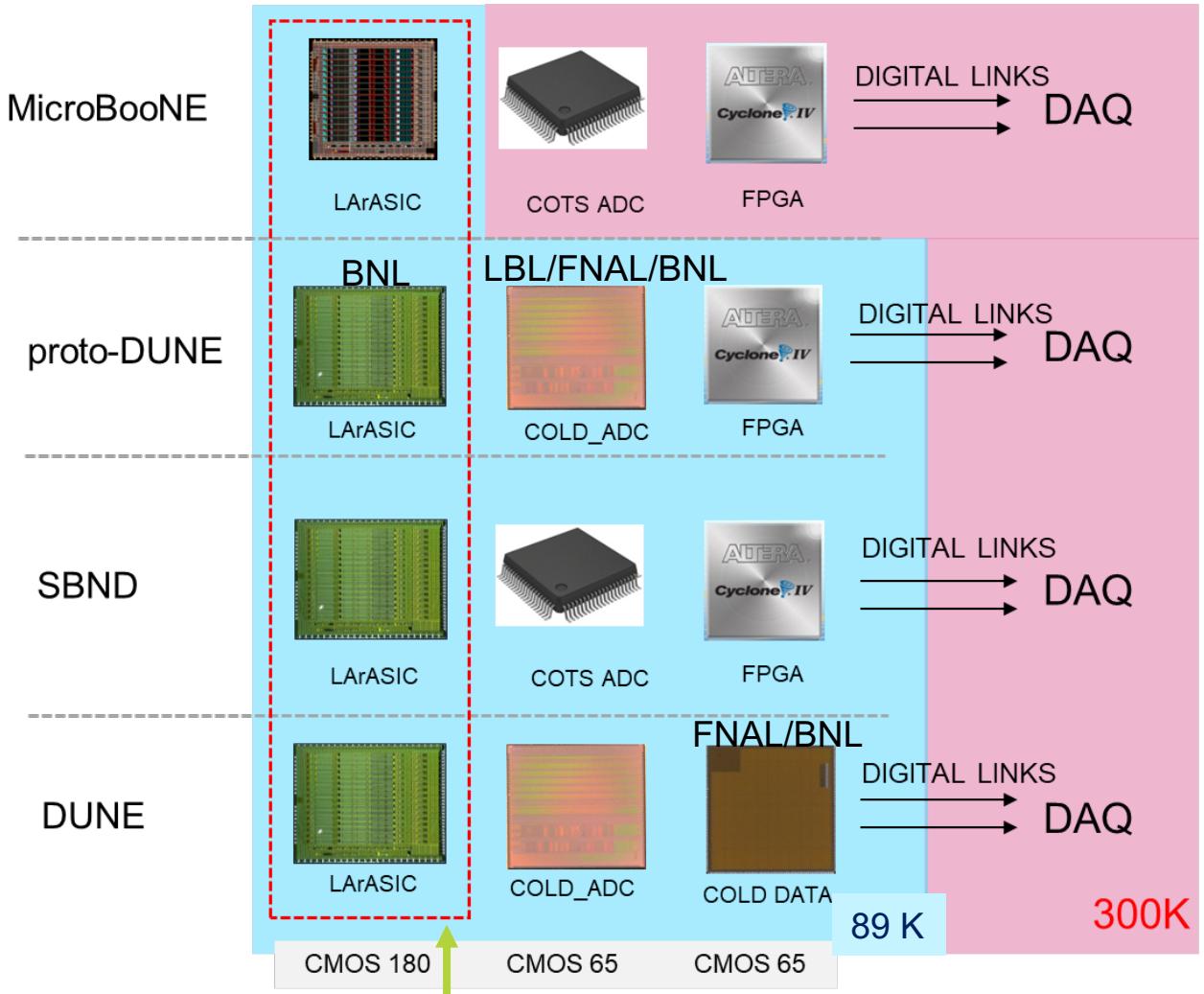
Primary functionality: CHARge aMplifer + Shaping Filter -> CHARMS ASICs

Version name	Features	Current status
CHARMS250V1	250 ns – 2 µs peaking time, input charge range up to 300 fC	Single channel ASIC designed, fabricated and characterized at 77 K, multi-channel ASIC being designed for MPW submission in FY27.
CHARMS250V2	250 ns – 2 µs peaking time, input charge range up to 10 pC	Feasibility studies and simulations completed, design advancing towards MPW submission in FY27.
CHARMS10V1	~10 ns – 250 ns peaking time, input charge range up to 300 fC	Feasibility studies planned in FY27.
CHARMS10V2	~10 ns – 250 ns peaking time, input charge range up to 10 pC	Feasibility studies planned in FY27 / FY28.

Brookhaven National Laboratory

BNL Cryogenic Front-end ASICs

About a decade of development



Peaking time programmable between 500 ns and 3 µs

To meet the demands of next generation experiments -> cryogenic front-end ASICs in 65 nm CMOS

Primary functionality: CHARge aMplifer + Shaping Filter -> CHARMS ASICs

Version name	Features	Current status
CHARMS250V1	250 ns – 2 µs peaking time, input charge range up to	Single channel ASIC designed, fabricated and characterized at 77 K, multi-channel ASIC being r MPW submission
CHARMS250V2	250 ns – 2 µs peaking time, input charge range up to 10 pC	Feasibility studies and simulations completed, design advancing towards MPW submission in FY27.
CHARMS10V1	~10 ns – 250 ns peaking time, input charge range up to 300 fC	Feasibility studies planned in FY27.
CHARMS10V2	~10 ns – 250 ns peaking time, input charge range up to 10 pC	Feasibility studies planned in FY27 / FY28.

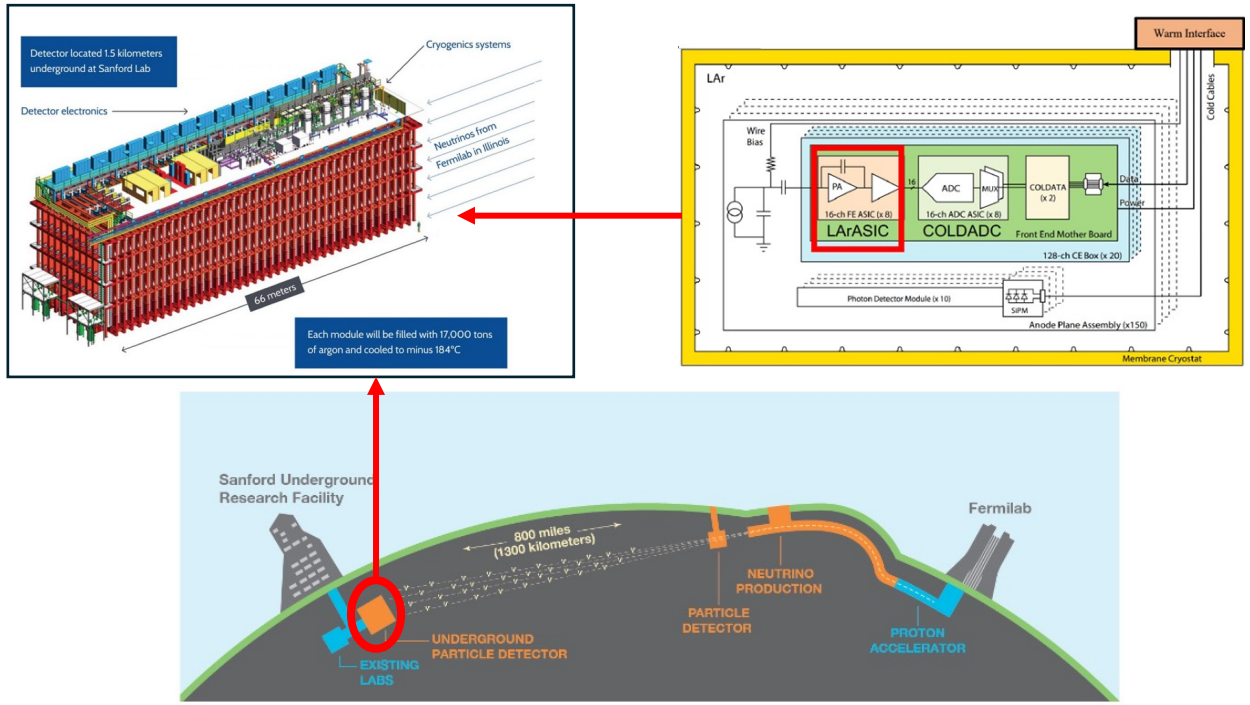
Covered in this talk

Brookhaven National Laboratory

Targets for CHARMS - DUNE

Deep Underground Neutrino Experiment:

- Major scientific experiment for studying neutrino/antineutrino oscillations, detect neutrinos emerging from exploding stars, search for signs of proton decay
- DUNE far detector (FD) located 1.5 km underground in South Dakota will operate with an intense neutrino beam generated at Fermilab
- DUNE Phase-II FDs will utilize four 10kTon liquid argon time projection chambers (TPCs) to detect ionization charge and scintillation light generated when incident neutrinos interact with argon atoms



Usage	Temperature	Detector Capacitance	Shaping Time	Dynamic Range
FD 3/4 charge readout	89 K	150 pF – 200 pF	250 ns – 2 µs	10 bits
FD 3/4 light readout	89 K	few nF (SiPMs)	10 ns – 250 ns	12-13 bits

Brookhaven National Laboratory

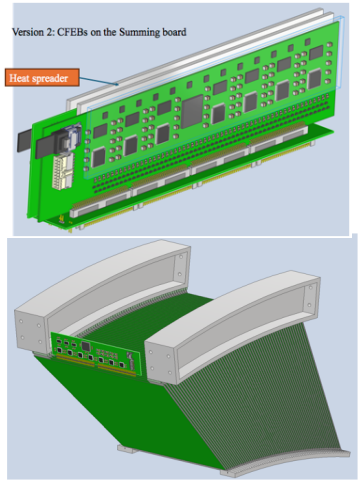
Targets for CHARMS - FCC-ee

Electron-Positron Future Circular Collider:

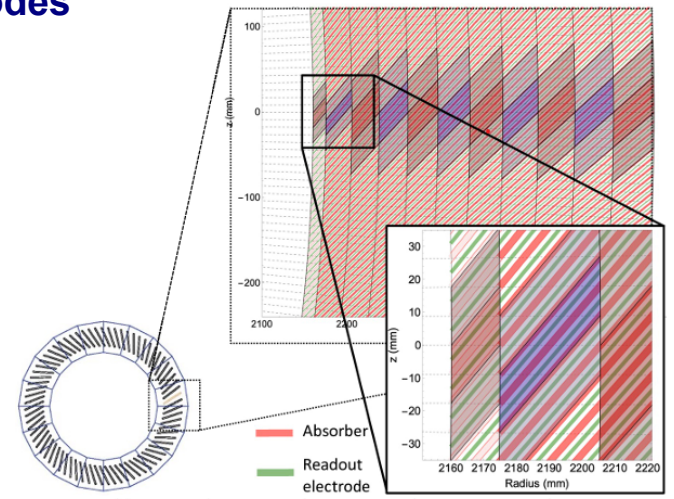
- Proposed to be constructed at CERN to serve as a general precision instrument for exploration of nature at the smallest scales
- Optimized to study with high precision the Z bosons, W pairs, Higgs bosons and top quark pairs
- **ALLEGRO (A Lepton coLlider Experiment with Granular calorimetry Read-Out)**, one of the proposed detectors, features a high granularity noble liquid electromagnetic calorimeter (ECAL) at its core

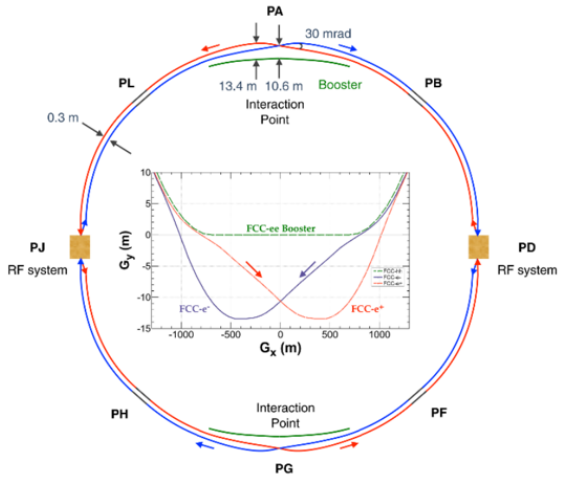
Usage	Temperature	Detector Capacitance	Shaping Time	Dynamic Range
Allegro	89 K	200 pF / 400 pF	200 ns	12 bits (4 fC – 10 pC)

Cold Front-End Boards Integrated on PCB Electrodes

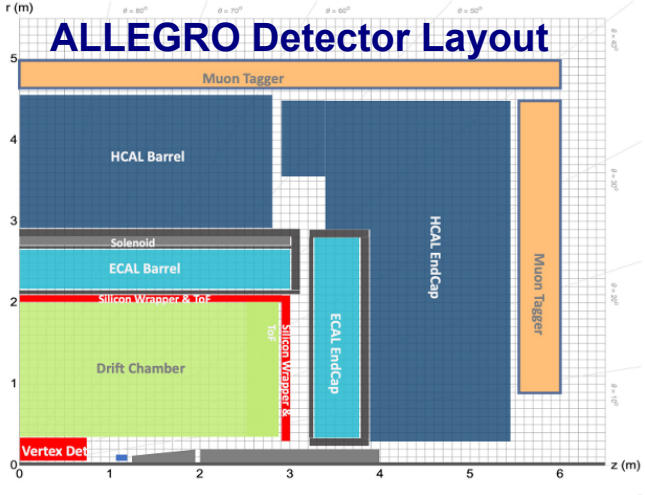


ALLEGRO Ecal Barrel Design





ALLEGRO Detector Layout



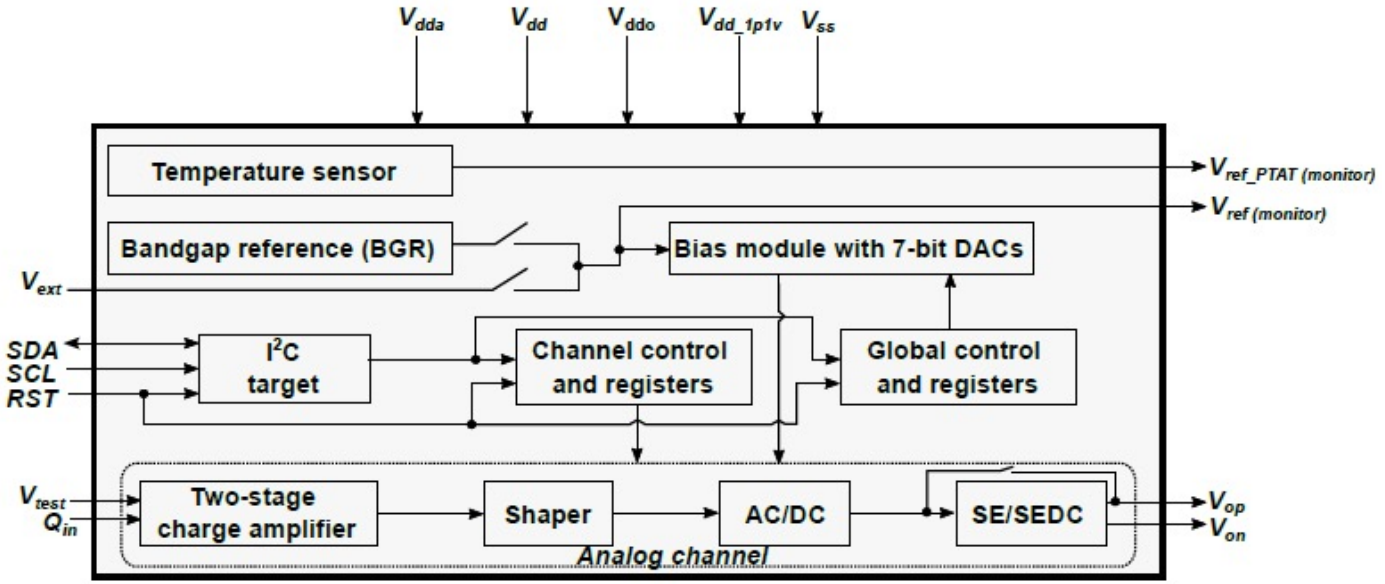
CHARMS250V1 specifications

Technology	65 nm CMOS: 1-poly, 9-metal
Supply voltage	1.8 V
Temperature range	77 K – 300 K (optimized for 89 K)
Number of channels	16
Maximum single-ended output swing	1.4 V peak to peak
Gain	4.7 mV/fC, 7.8 mV/fC, 14 mV/fC, 25 mV/fC
Full-scale input charge	300 fC, 180 fC, 100 fC, 56 fC
Baseline selection	200 mV (unipolar, collection mode), 900 mV (bipolar, induction mode)
Adaptive reset current	0.1 nA, 0.5 nA, 1 nA, 2 nA
Peaking time	250 ns, 500 ns, 1 µs, 2 µs
Output coupling	DC, AC
Output drive	Shaper, single-ended buffer, differential buffer
Integrated test capacitor	200 fF
Integrated pulse generator	10-bit DAC based
Configuration control	I^2C based for providing digital assistance (programmable gain, peaking time, baseline, RQI)

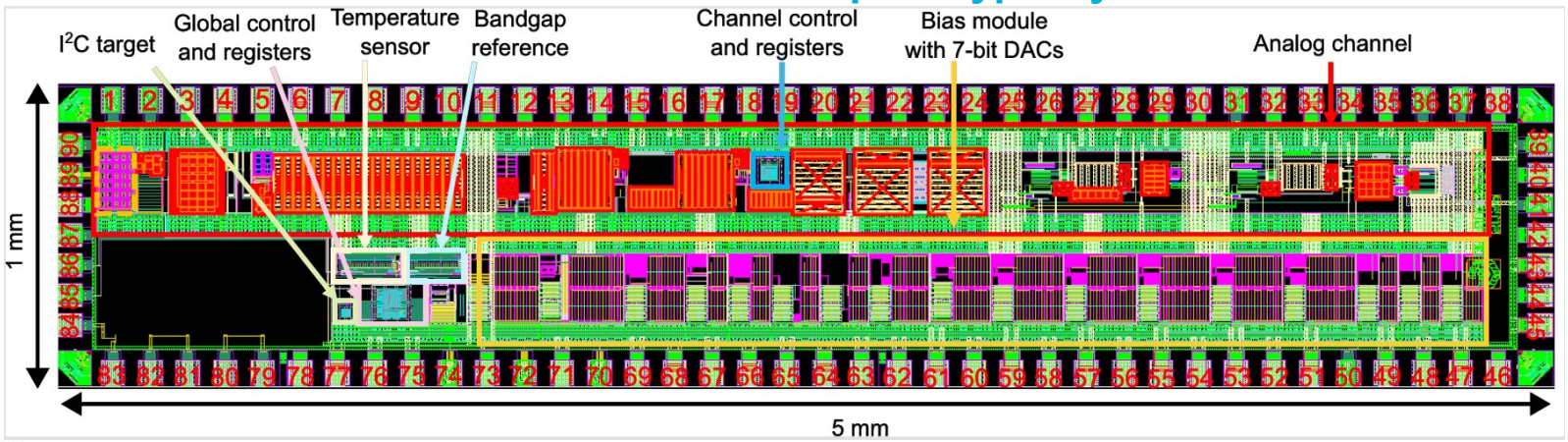
- Key features and challenges
  - ***65 nm*** CMOS with ***thick oxide*** → To limit gate leakage current and ***parallel noise contribution***
  - ***Low*** power consumption (6-11 mW per channel) → support detector electrodes with ***fine segmentations***
  - ***Cryogenic*** operation with ***long lifetime of electronics*** → achieve optimum ***SNR***

Single Channel Prototype: CHARMS250V1

CHARMS250V1 prototype block diagram



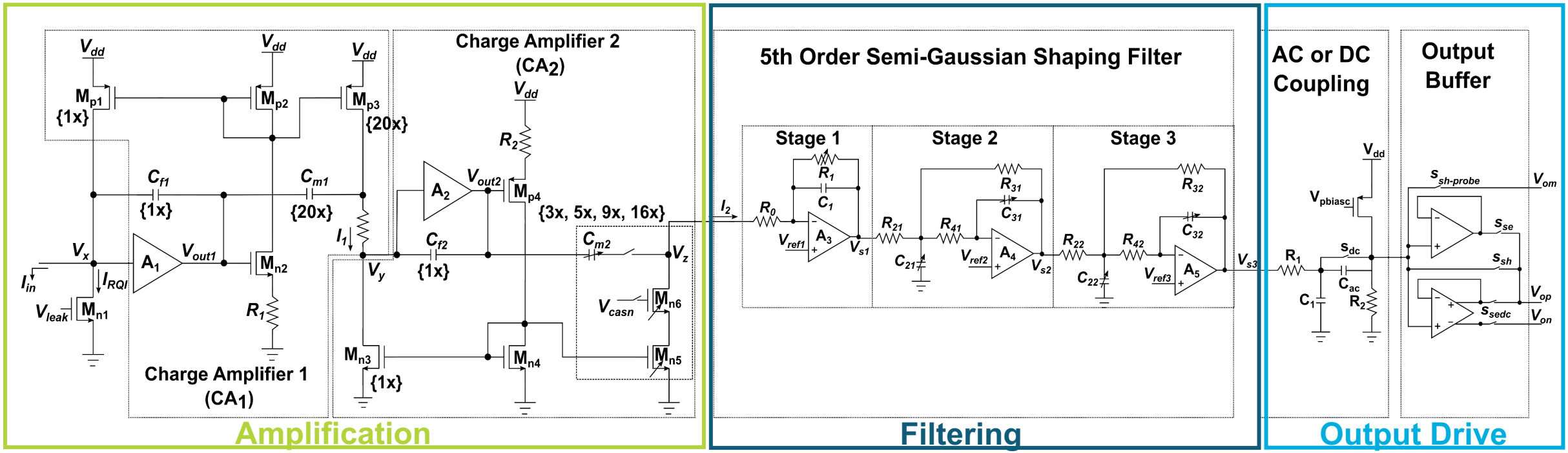
CHARMS250V1 prototype layout



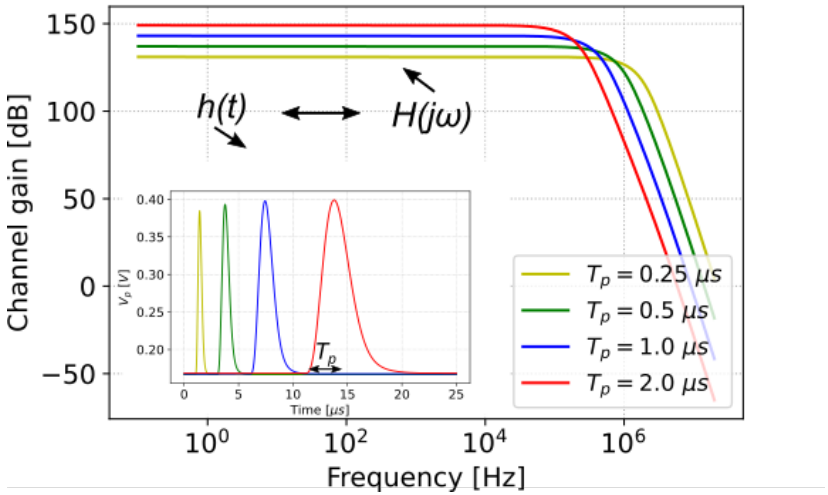
Submitted for fabrication in June 2025; received in October 2025.

Brookhaven National Laboratory

CHARMS250 Analog Channel Schematic and Impulse Response



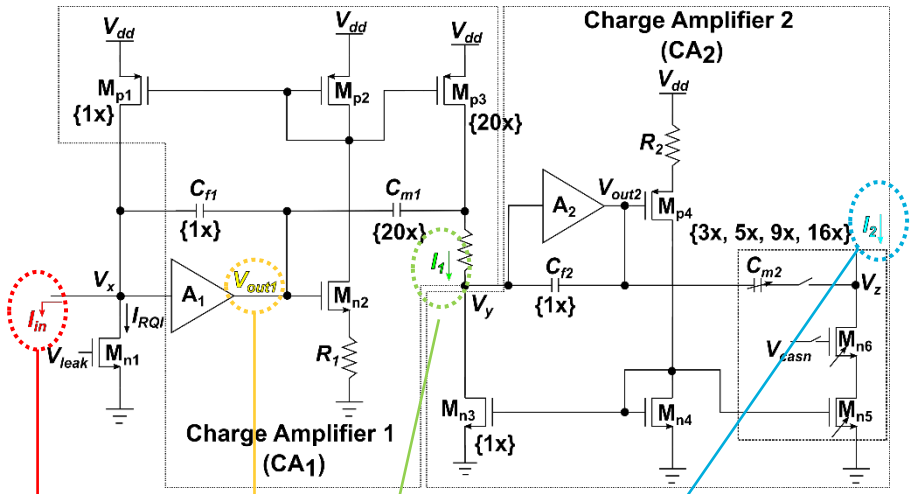
Impulse Response ->



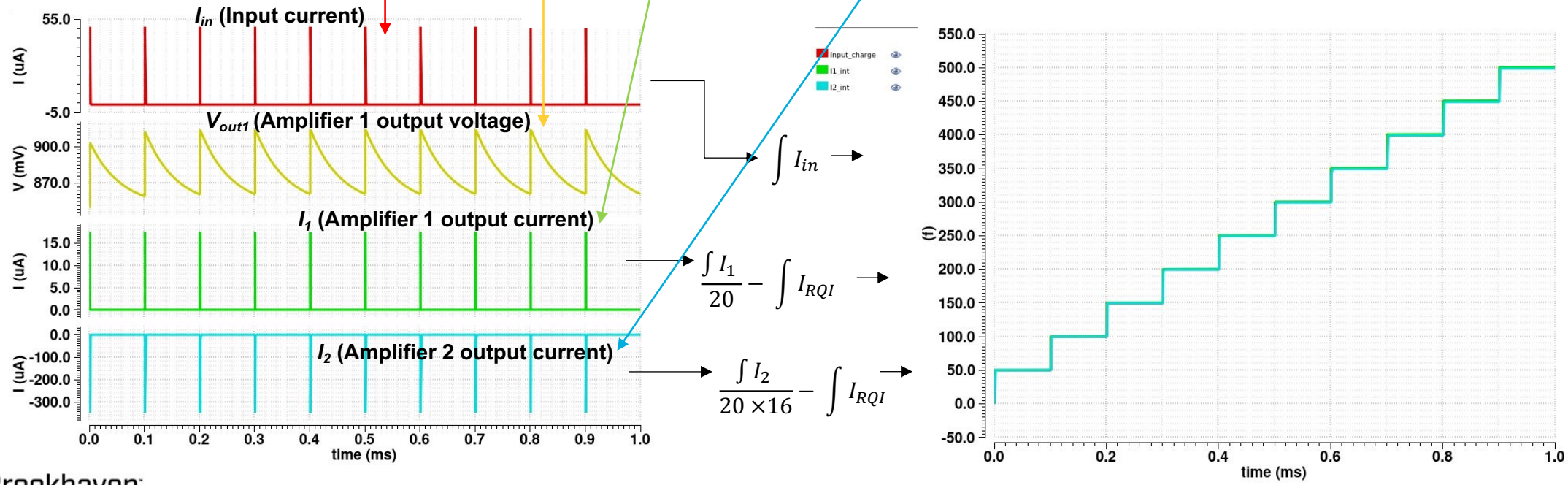
Peaking time (T_p)	Cut-of frequency (f_{3dB})	Sampling frequency ($f_s = 2/T_p$)	Gain change at f_s
0.25 µs	820 KHz	8 MHz	-79 dB
0.5 µs	411 KHz	4 MHz	-71 dB
1.0 µs	205 KHz	2 MHz	-68 dB
2.0 µs	102 KHz	1 MHz	-66 dB

Charge amplifier design and transient response

- Charge amplifiers use current-mirror based adaptive continuous reset (I_{RQI} = 100 pA, 500 pA, 1 nA or 2 nA)
- Pole-zero cancellation implemented in each stage

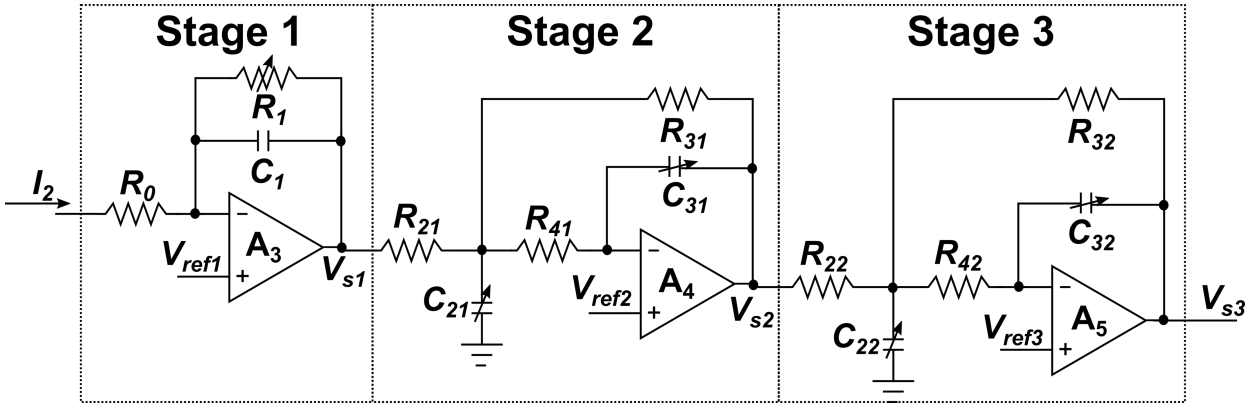


- A_1 and A_2: 3-stage amplifiers (> 100 dB gain for each, at both room and LAr temperatures)
- Charge gain provided by CSA_1 = 20
- Charge gain (programmable) provided by CSA_2 = 3 or 5 or 9 or 16
- **In the current design, C_{f1} = ~ 1 pF,C_{f2} = ~ 8 pF optimized for 300 fC maximum input charge**

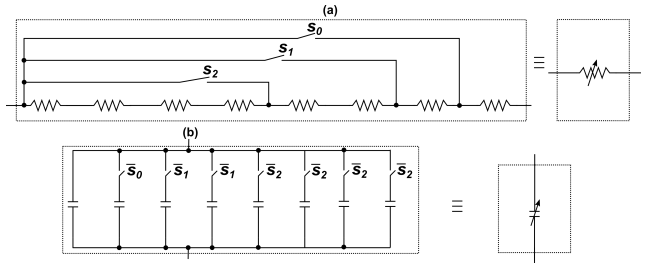


Ref: G. De Geronimo et. al., Front-End ASIC for a GEM based Time Projection Chamber

Shaping filter design



- Peaking time is programmable (0.25 µs – 2 µs)
- Lower series noise with longer shaping times
- Implemented shaper is a 5th order semi-gaussian filter with complex conjugate poles
- Semi-gaussian shaper has a faster return to baseline than a CR-RC^n shaping filter
- Faster tail lowers contribution of parallel noise
- Symmetric rising and falling edges also helpful for mitigating pile-up of events
- A_3, A_4, A_5 are two-stage miller compensated differential amplifiers
- V_{ref1}, V_{ref2}, V_{ref3} selected based on output baseline setting



Component values for CHARMS250

Resistor	Value (kΩ)	Capacitor	Value (pF)
R_0	0.3		
R_u (R_1)	7.5	C_1	11.9
R_{21}, R_{41}, R_{42}	18	C_u (C_{21})	5.9
R_{31}	60	C_u (C_{31})	1.39
R_{22}	36	C_u (C_{22})	5.5
R_{32}	39	C_u (C_{32})	1.13

$$V_{s1}(s) = -I_2(s)\frac{R_1}{(1+sC_1R_1)}$$

$$V_{s2}(s) = -V_{s1}(s)\frac{\frac{1}{R_{21}R_{41}C_{21}C_{31}}}{s^2 + s\left(\frac{1}{R_{21}C_{21}} + \frac{1}{R_{31}C_{31}} + \frac{1}{R_{41}C_{21}}\right) + \frac{1}{R_{31}R_{41}C_{21}C_{31}}}$$

$V_{s3}(s)$ is similar……

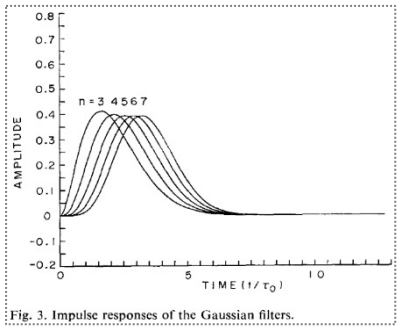
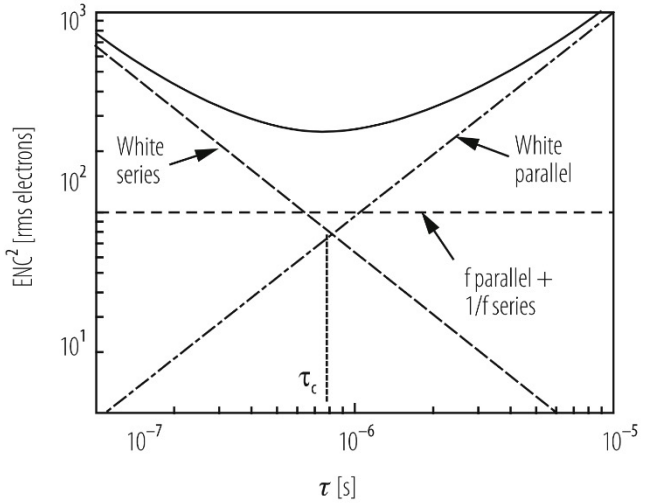


Fig. 3. Impulse responses of the Gaussian filters.

Ref: S. Ohkawa, M. Yoshizawa, K. Husimi, Direct synthesis of the Gaussian filter for nuclear pulse amplifiers.



Ref: Veljko Radeka, Signal Processing for Particle Detectors

Noise minimization strategy

$$ENC^2 = (C_d + C_{in})^2 \left(A_w v_n^2 \frac{1}{T_p} + A_f K_f \right) + A_p i_n^2 T_p$$

(Sum of white series noise, 1/f series noise and parallel noise components)

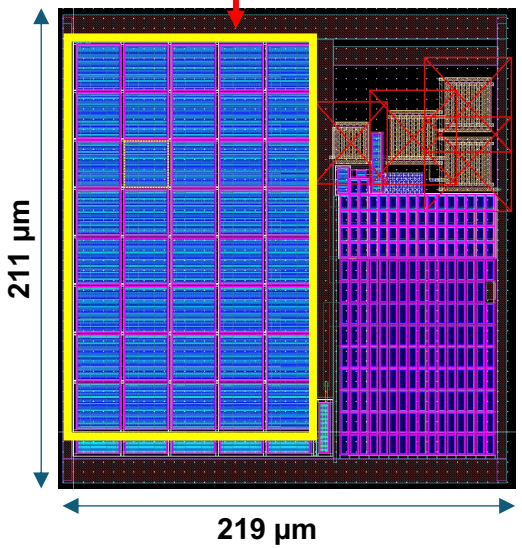
$$ENC_f^2 = K_f \frac{(C_d + C_g)^2}{C_g} N_f \Rightarrow C_g = C_d$$

$$ENC_w^2 = 4k_B T n \gamma \alpha_w \frac{(C_d + C_g)^2}{g_m(C_g)} N_f \Rightarrow C_g = \frac{1}{3} C_d$$

Input stage transistor sized to have C_g ~ 40 pF, optimal choice for minimizing noise with C_{det} ~ 150 pF with given power budget

	Minimum allowable transistor length	Input transistor length	Input transistor width
180 nm (LArASIC)	180 nm	270 nm	20 mm
65 nm (CHARMS250)	280 nm	400 nm	24 mm

Input transistor implemented with 30 copies of transistors of width of 20 µm and 40 fingers

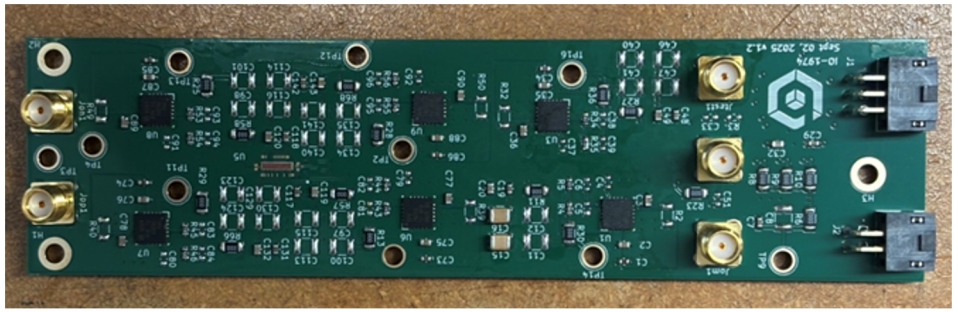


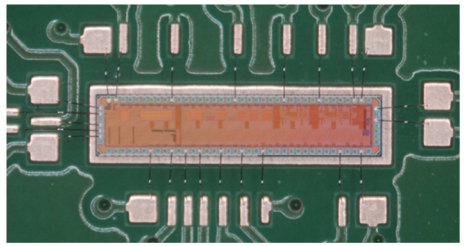
- **Input stage transistors for A_1 implemented using thick oxide (2.5 V) devices in 65 nm for CHARMS to limit leakage current and associated parallel noise**
- **Thin oxide device of the same dimensions has a gate leakage current of ≈ 20 nA, contributing almost 200 electrons to the ENC for 1 µs peaking time and triangular weighting function!**

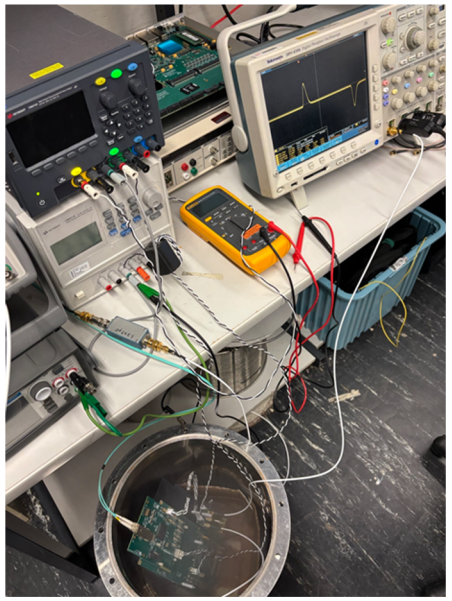
Brookhaven National Laboratory

Ref: [1] Angelo Rivetti, Front-End Electronics for Radiation Sensors
[2] Veljko Radeka, Signal Processing for Particle Detectors

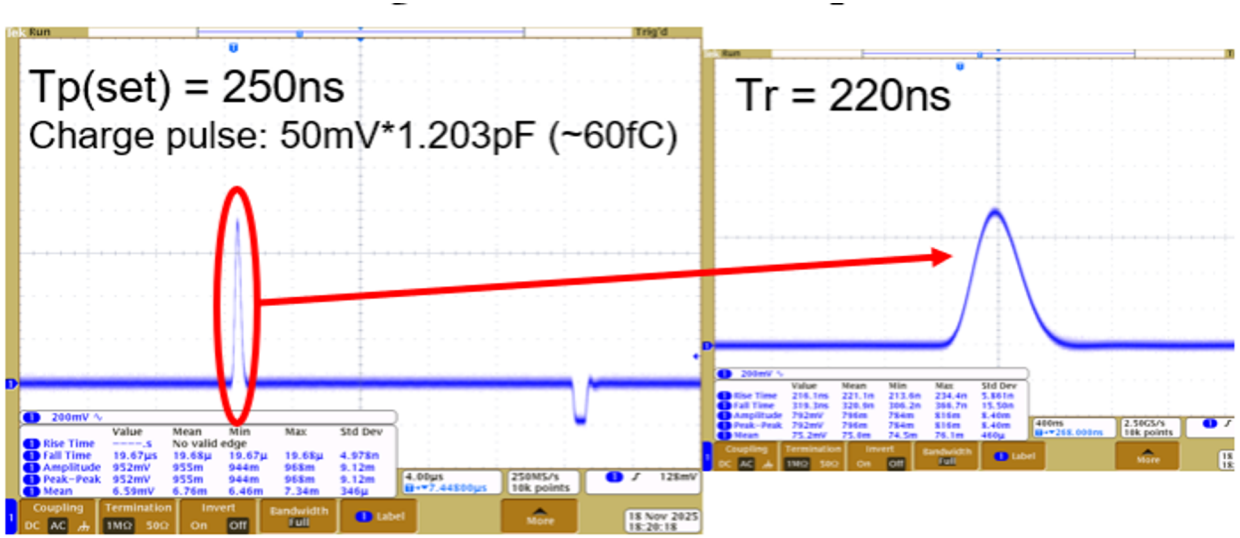
CHARMS250V1 Characterization Results

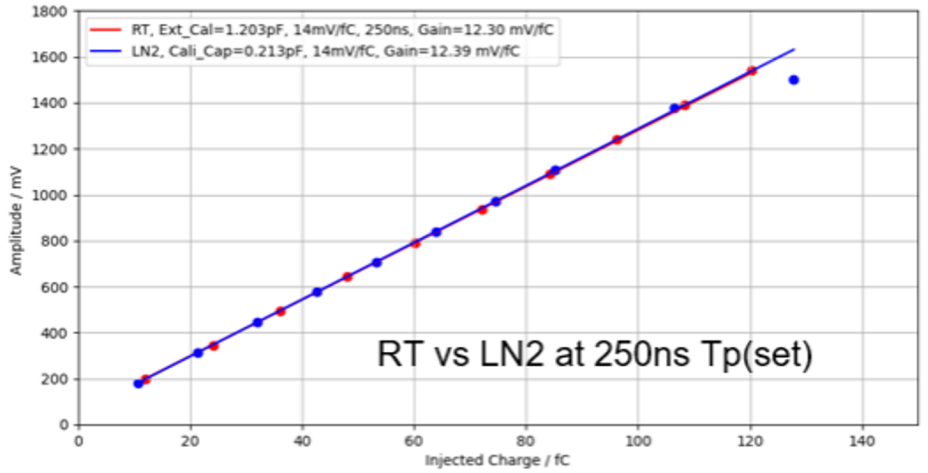






Test Setup



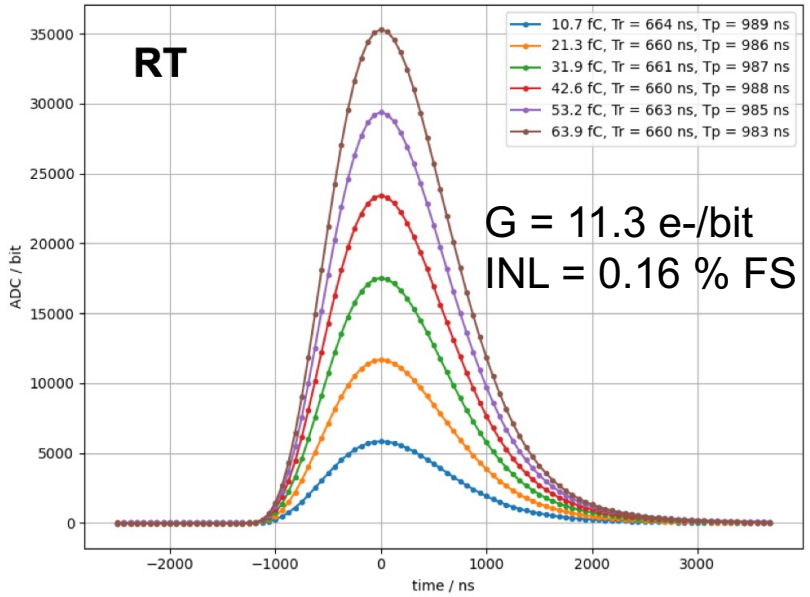


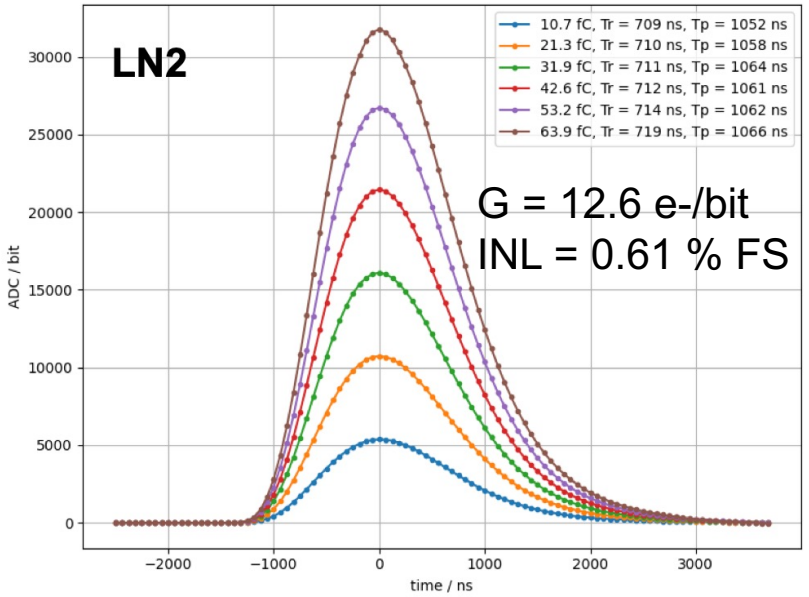
No significant gain change at liquid nitrogen temperature (LNT) compared to room temperature (RT) for 14 mV/fC gain

Brookhaven National Laboratory

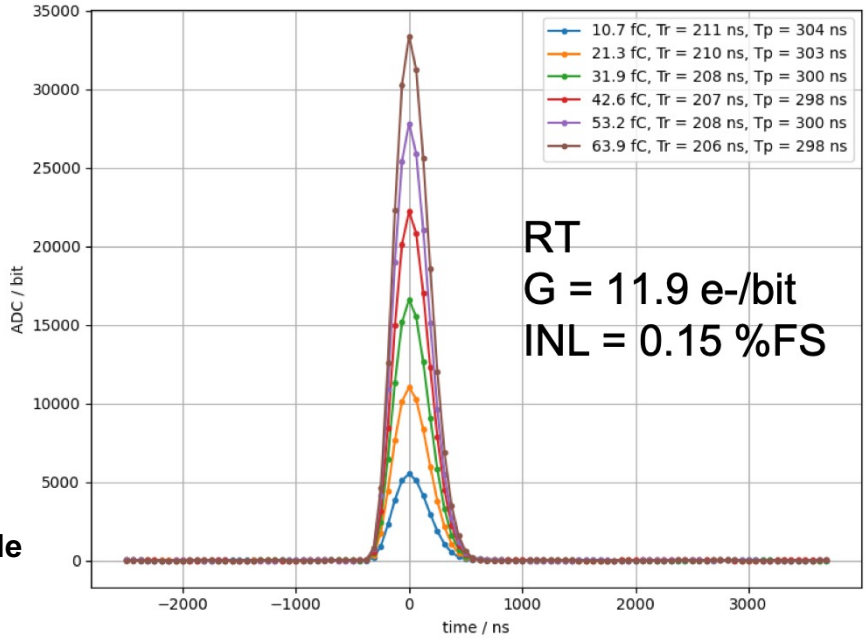
Measured Pulse Response Comparison at RT and LNT

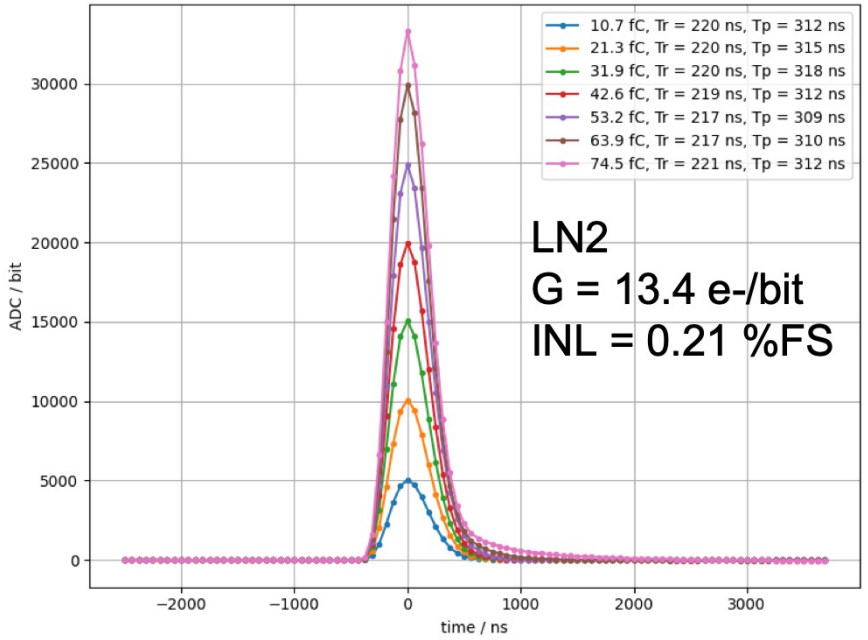
Gain: 14 mV/fC
Tp: 1 µs





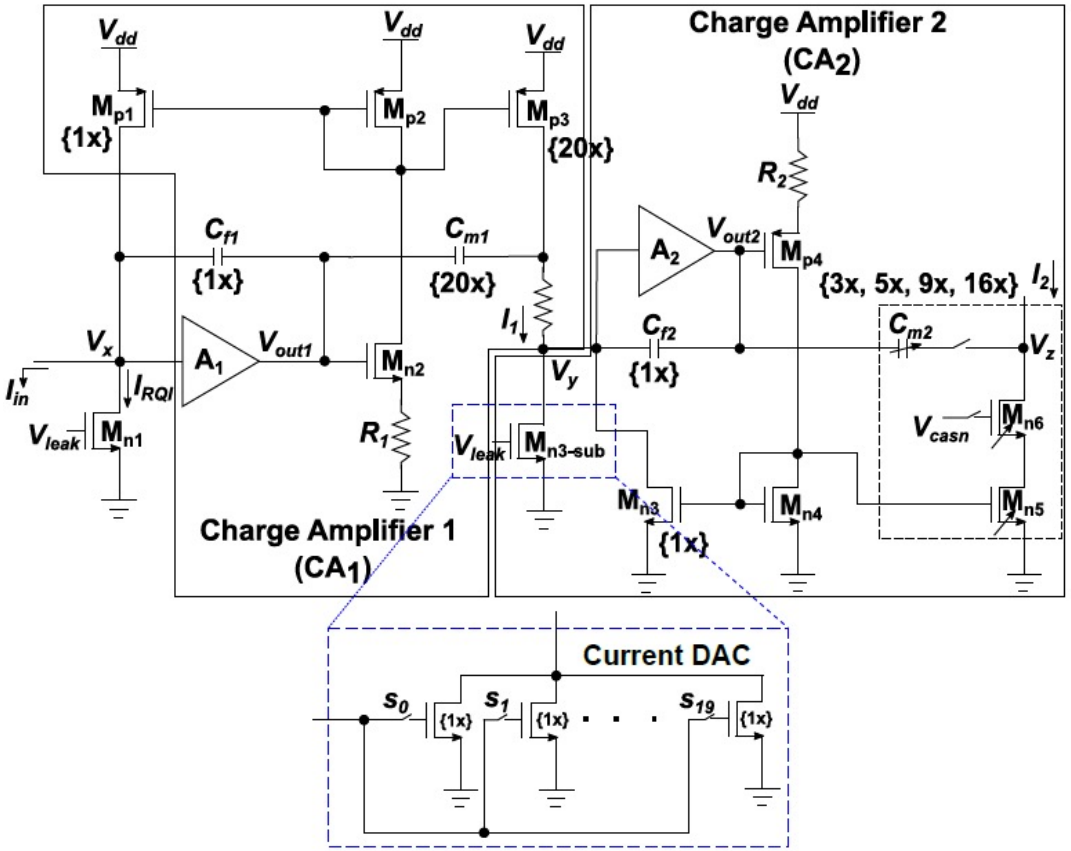
Gain: 14 mV/fC
Tp: 250 ns





Tr: 10%-90% amplitude
Tp: 5% to peak amplitude

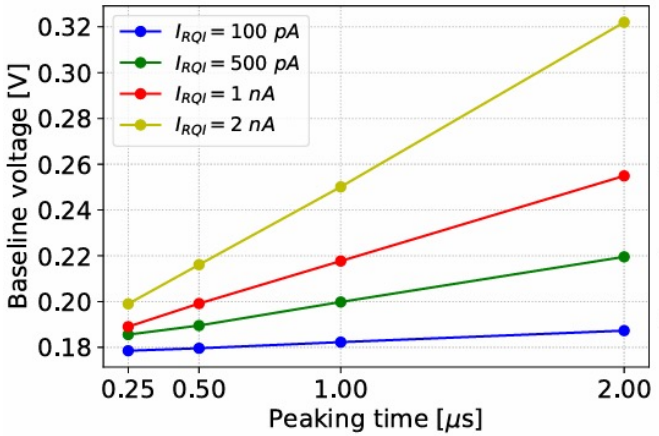
Programmable Baseline Adjustment Per Channel



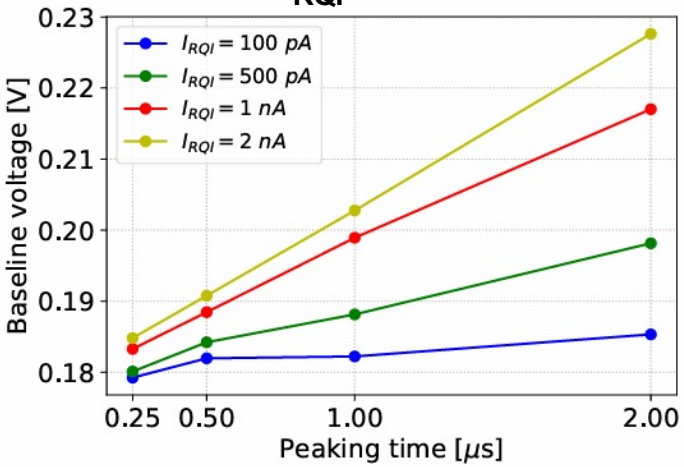
- Digitally programmable CA_2 I_{RQI} subtraction implemented.
- Allows independent baseline adjustment per channel, preserving headroom and full-scale input charge range.

Measured baselines at LNT

No I_{RQI} subtraction



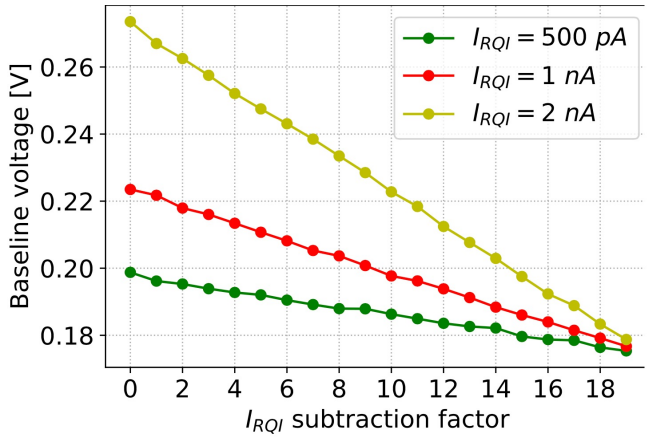
19x I_{RQI} subtraction



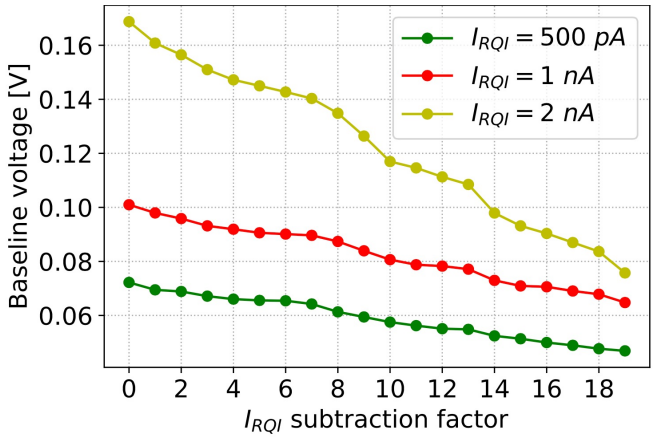
Baseline change reduced from ~140 mV to ~50 mV

Measured baseline as a function of the I_{RQI} subtraction factor

RT

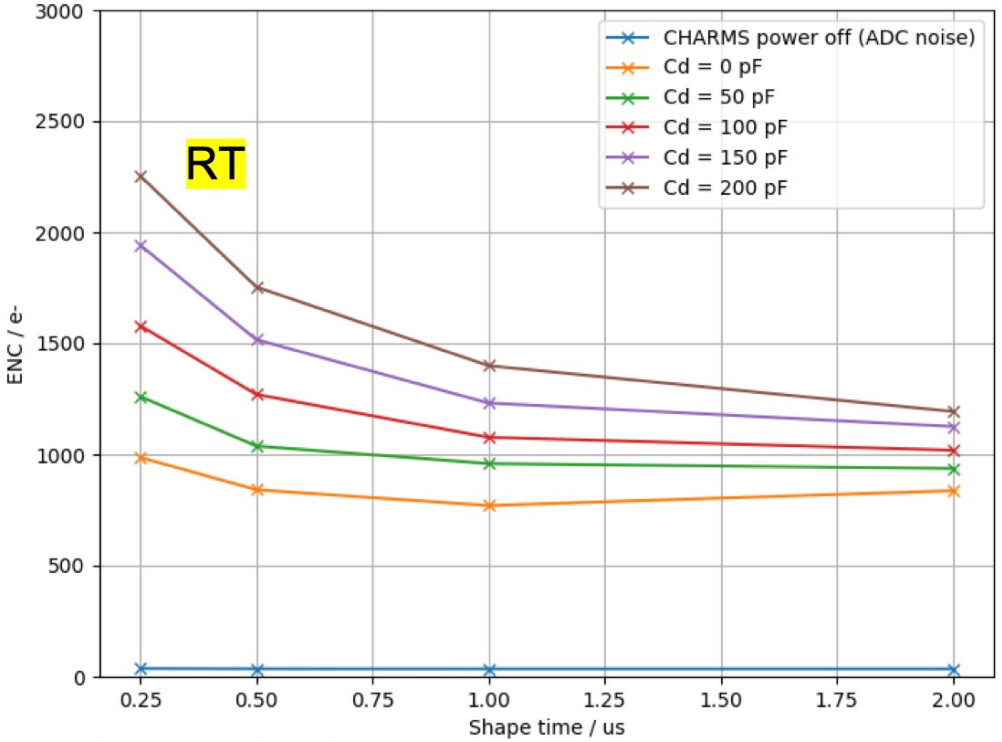


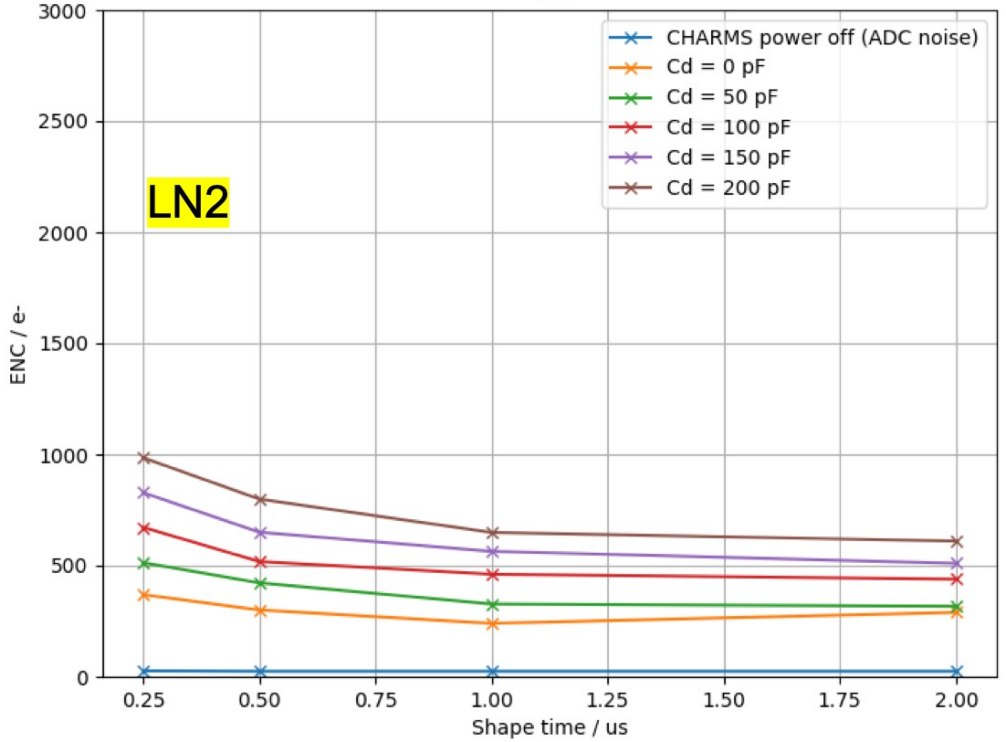
LNT

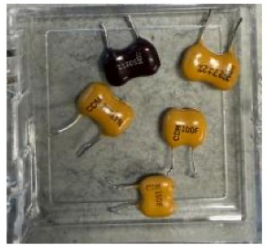


Higher non-linearity in baseline at LNT due to increased I_d variability in deep-subthreshold current DAC transistors

Measured ENC at RT and LNT (Gain: 14 mV/fC)







Mica caps as Cd

RT	14mV/fC			
Cd	250ns	500ns	1us	2us
ADC	36	35	34	34
0	986	841	770	836
50	1260	1037	958	936
100	1579	1270	1077	1019
150	1942	1516	1231	1125
200	2253	1753	1399	1193

LN2	14mV/fC			
Cd	250ns	500ns	1us	2us
ADC	26	24	24	24
0	369	300	240	289
50	513	422	327	317
100	672	518	461	439
150	828	650	564	510
200	985	799	649	610

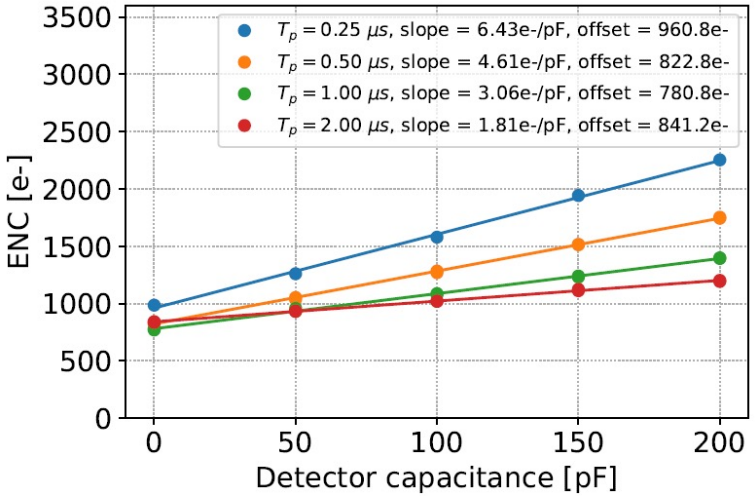
17

Brookhaven National Laboratory

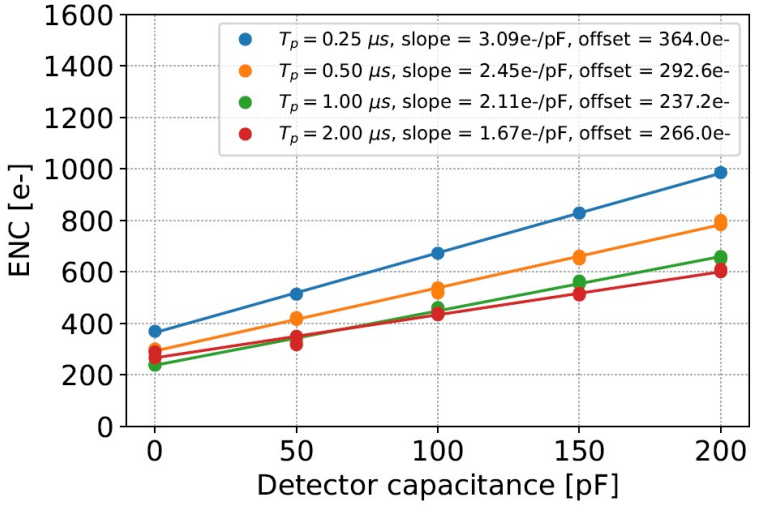
CHARMS250V1 noise at LNT within 10% of the LArASIC noise at LNT for the same C_d and peaking time

CHARMS250V1 Noise Projection, Power Consumption and Test Summary

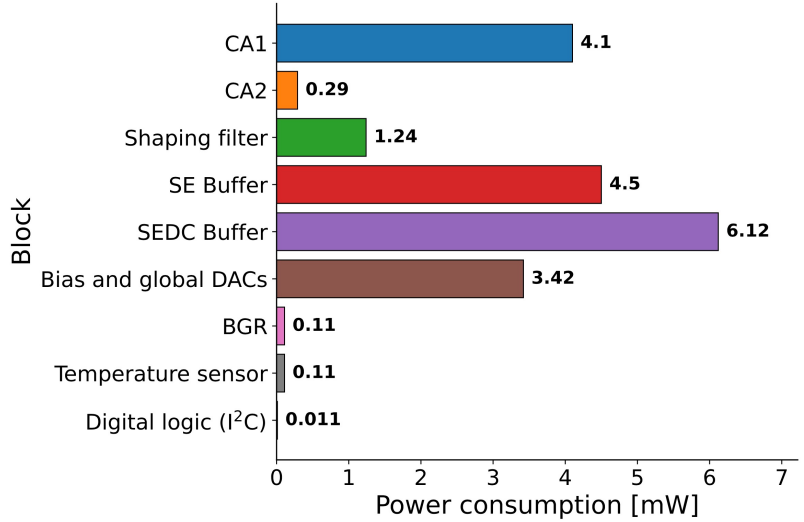
Measured ENC vs. Cd, RT



Measured ENC vs. Cd, LNT



Power consumption breakdown



Peaking Time	**250 ns**	500 ns	1000 ns	2000 ns
RT	**6.4**	4.6	3.1	1.8
LNT	**3.1**	2.5	2.1	1.7

Noise Projection (e-/pF)

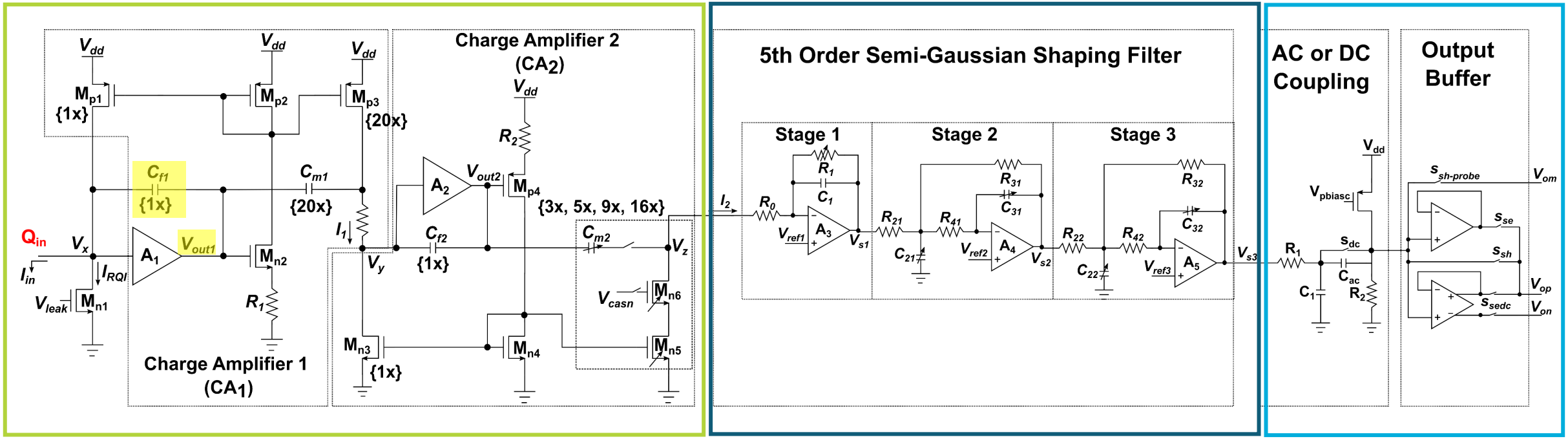
CHARMS250V1 meets most design expectations:

- **< 10 mW** per channel: preamplifier + shaper ~ 5.5 mW (from simulation) + other blocks (biasing, BGR, DAC etc.)
- Works at **77K** (-196 °C) – 300K
- **ENC of 564 e-** for 150 pF detector capacitance and 1 µs peaking time at 77 K
- **Good peaking time and linearity** (some degradation in linearity seen for large charges at LNT due to non-linear resistance of CA_2 gain selection network switches, to be fixed in next version of the chip)

Brookhaven National Laboratory

Extending the dynamic range of CHARMS250 to 10 pC (CHARMS250V2A and CHARMS250V2B)

Updates needed for extending the dynamic range to 10 pC for ALLEGRO

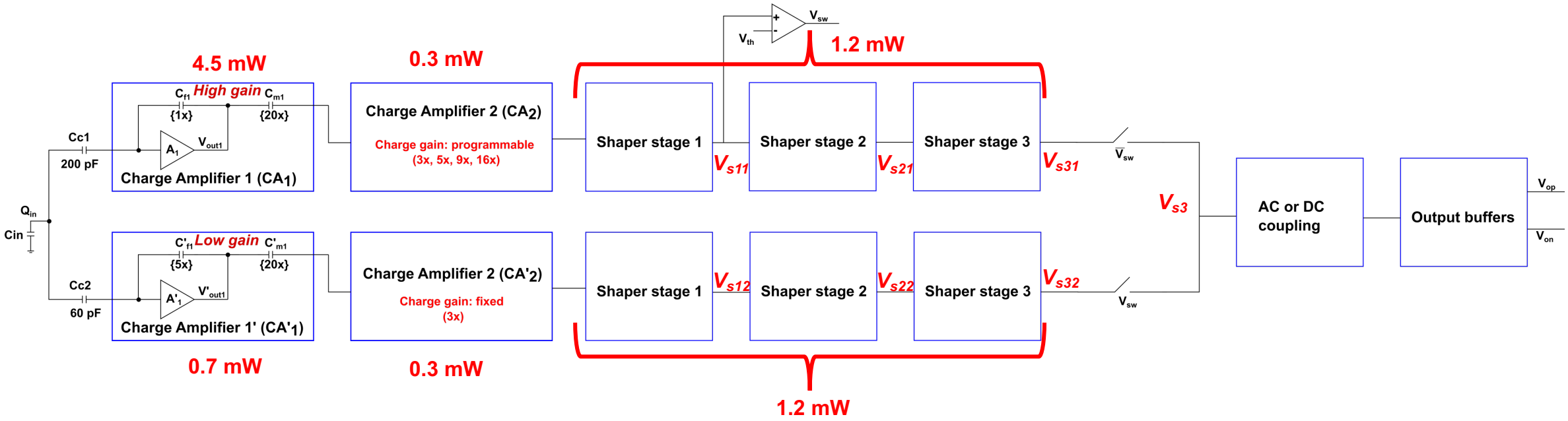


- Current front-end designed to process charges up to 300 fC, CA_1 charge gain = 20, minimum CA_2 charge gain = 3
- C_{f1} ~ 1 pF, C_{f2} ~ 8 pF, So for 300 fC Q_{in}, V_{out1} swing is ~ (300 fC/1pF) = 300 mV and V_{out2} swing is ~ (300 x 20 fC/8 pF) = 750 mV
- For larger values of Q_{in}, V_{out1} starts to saturate → **We need to increase C_{f1} (by 30x for ~30x increase in input charge range)**
- **By simply increasing Cf1, front-end saturation up to 10 pC can be prevented, but noise increases by 10x or more**

Brookhaven National Laboratory

CHARMS250V2A (Dual parallel gain paths) architecture

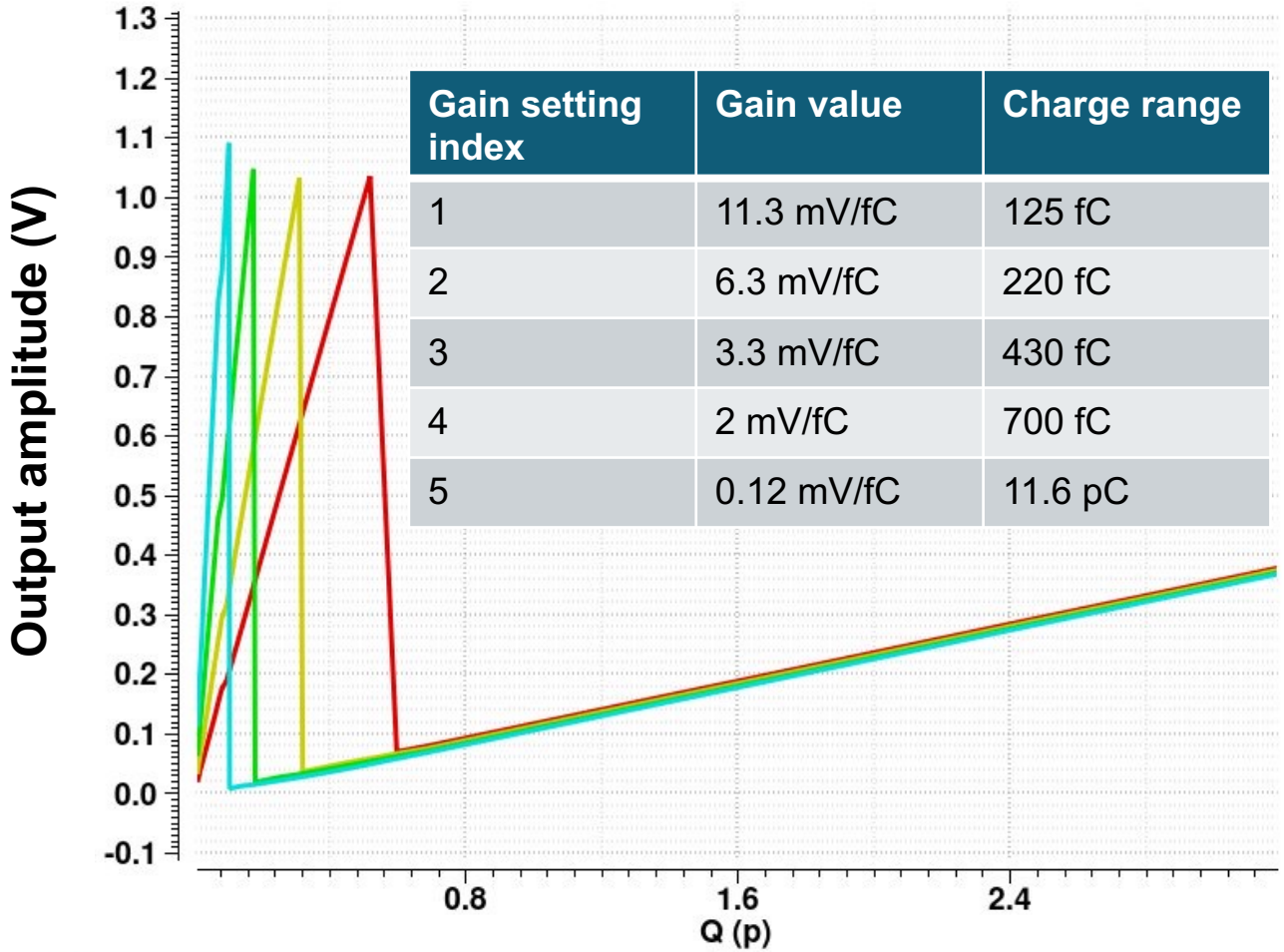
- Two parallel gain and shaping filter paths, combined ac-dc coupling and output buffer



- High gain path optimized for low noise; low gain path (note lower power consumption) output has higher noise but allows high dynamic range
- We need to read out two signals: amplified charge (voltage) pulse and Vsw (indicating which gain path was selected

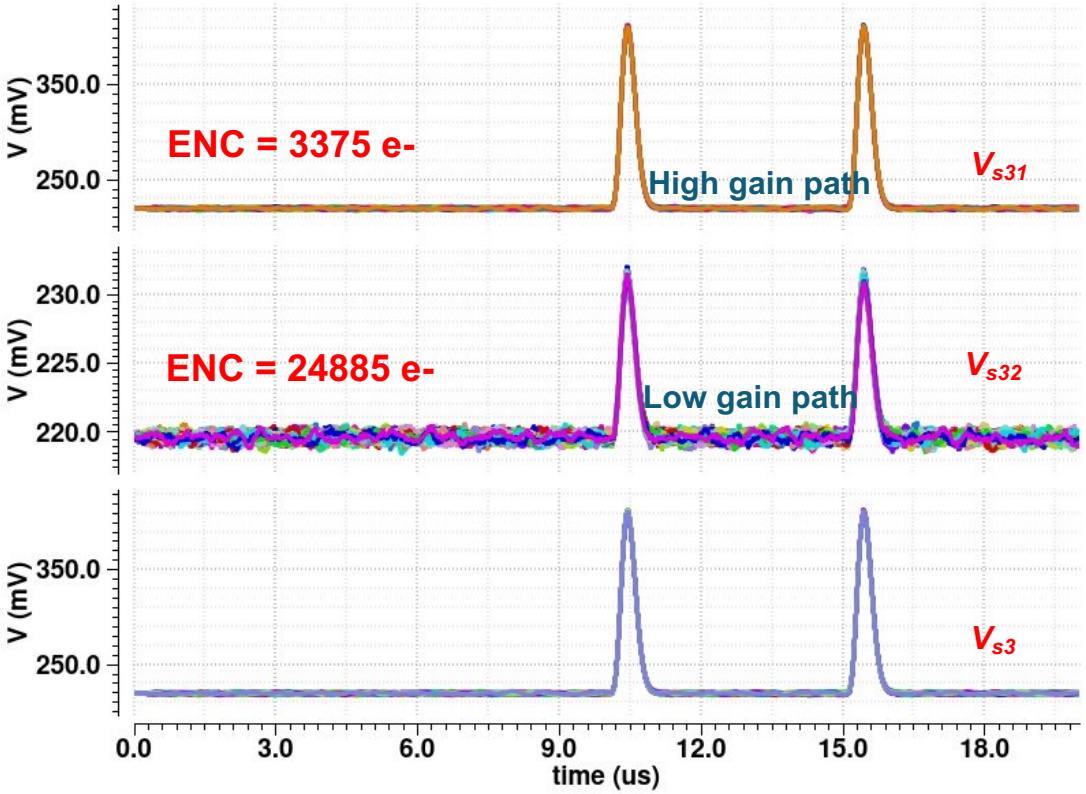
CHARMS250V2A transfer characteristics and simulated noise at RT

Input charge vs. output amplitude



Gain setting index	Gain value	Charge range
1	11.3 mV/fC	125 fC
2	6.3 mV/fC	220 fC
3	3.3 mV/fC	430 fC
4	2 mV/fC	700 fC
5	0.12 mV/fC	11.6 pC

T_p = 250 ns, C_d = 200 pF, Q_{in} = 100 fC

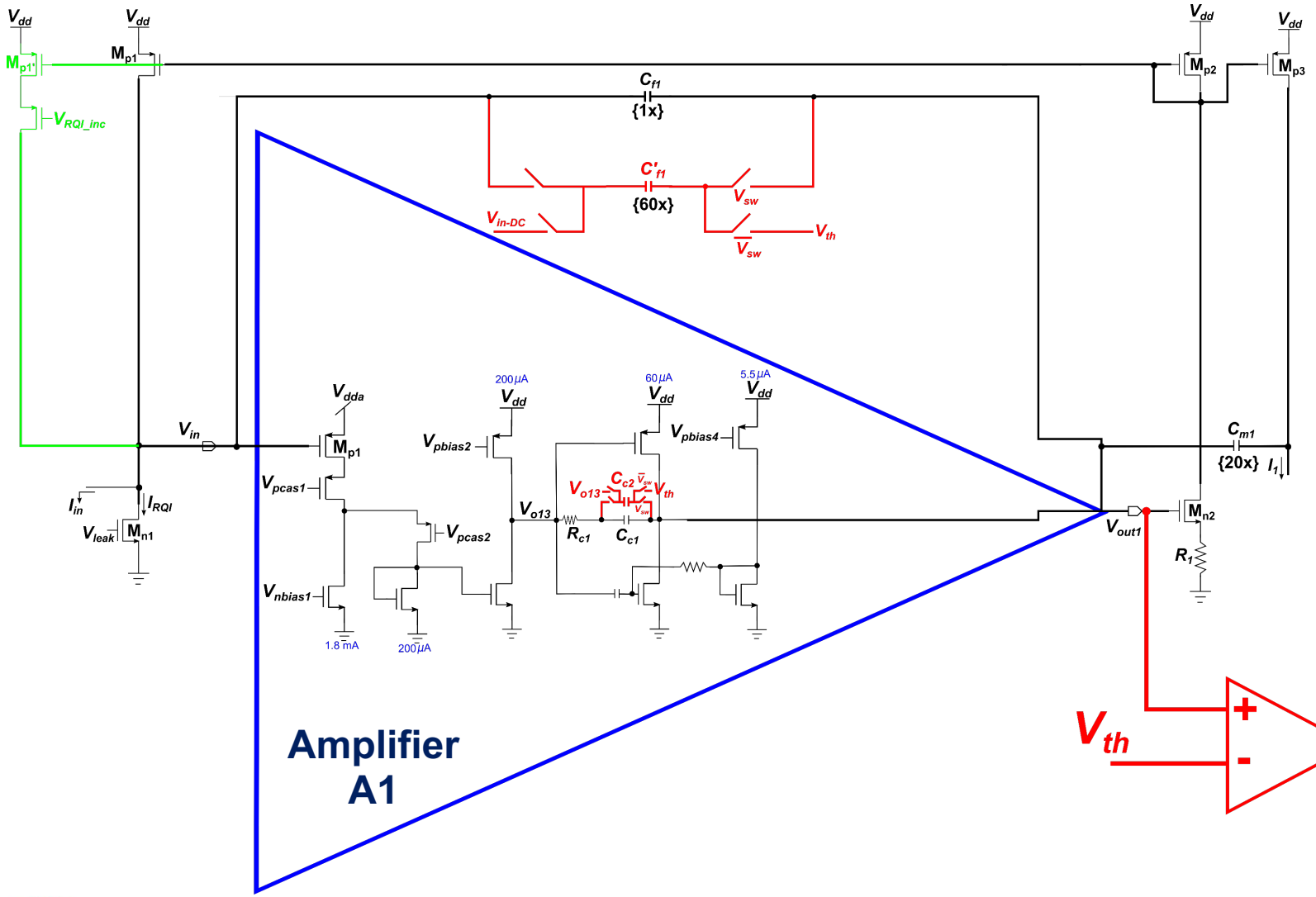


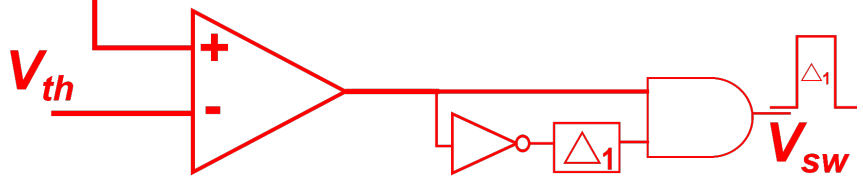
Corresponding SNR for:

- **MIP (4 fC): ~ 8**
- **Gain transition point (700 fC): ~176**

Brookhaven National Laboratory

CHARMS250V2AB (Dynamic feedback capacitance switching) architecture



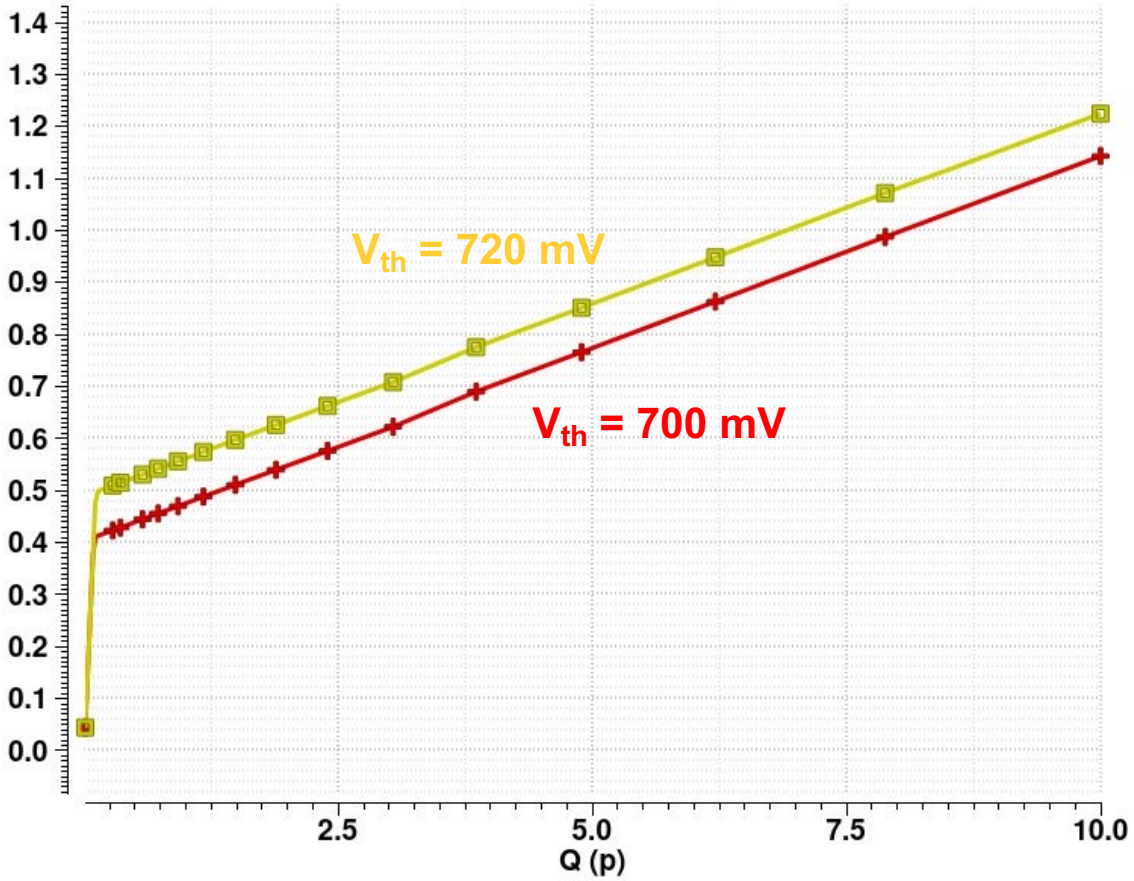


- CA1 updated to increase the feedback capacitance (by ~ 60x) when the amplifier A1 output crosses a threshold.
- Feedback capacitance returned to the original 1x value after a short interval (~ 1 µs).
- Compensation capacitance in A1 follows the same adjustment path as feedback capacitance to preserve stability.
- After event detection (threshold crossing) dynamic non-linear I_{RQI} increase implemented to allow baseline to be reset.

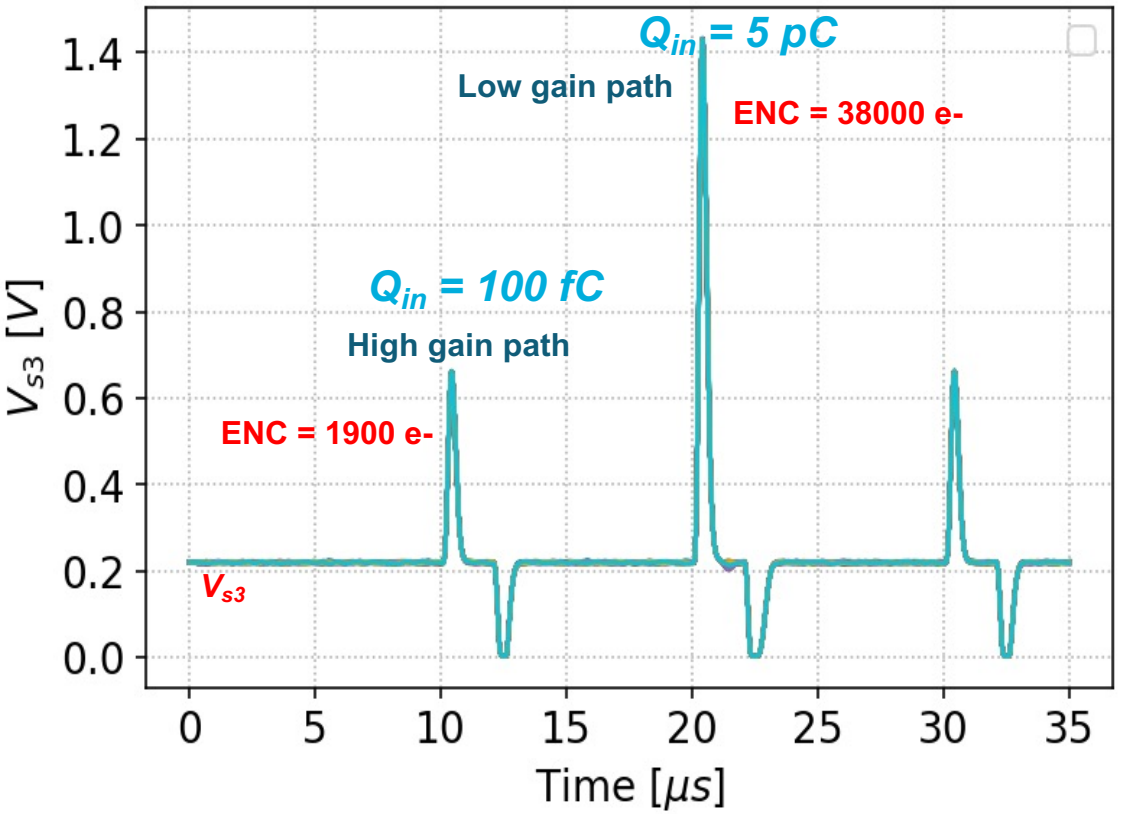
Brookhaven National Laboratory

CHARMS250V2B transfer characteristics and simulated noise at RT

Input charge vs. output amplitude



C_d = 200 pF



Corresponding SNR for:

- **MIP (4 fC): ~ 13**
- **Gain transition point: 15**

Brookhaven National Laboratory

Summary

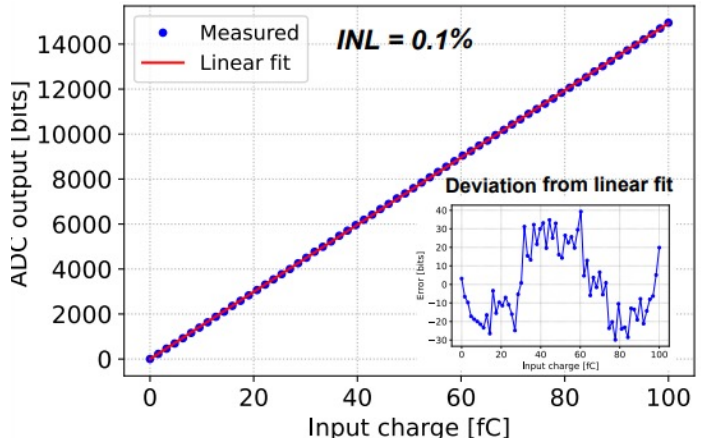
- CHARMS family of low-noise cryogenic analog front-end ASICs in 65 nm being developed at BNL.
- CHARMS250V1 prototype fabricated and characterized at BNL; shows good noise performance down to 77 K; multi-channel CHARMS250V1 so be submitted for fabrication in early 2027.
- Two front-end architectures to extend the full-scale input charge range of CHARMS250V1 to 10 pC being developed:

	CHARMS250V2A	CHARMS250V2B
Architecture	Dual parallel gain paths	Dynamic feedback capacitance switching
# of inputs	2 (if coupling capacitor external)	1
# of outputs	2 (signal, enabled path)	1
ENC (Cin = 200 pF, T_p = 250 ns, room temperature)	High gain mode: 3.4k e-	High gain mode: 1.9k e-
	Low gain mode: 24k e-	Low gain mode: 38k e-
Power per channel (amplifier + shaping filter)	8.2 mW	6 mW

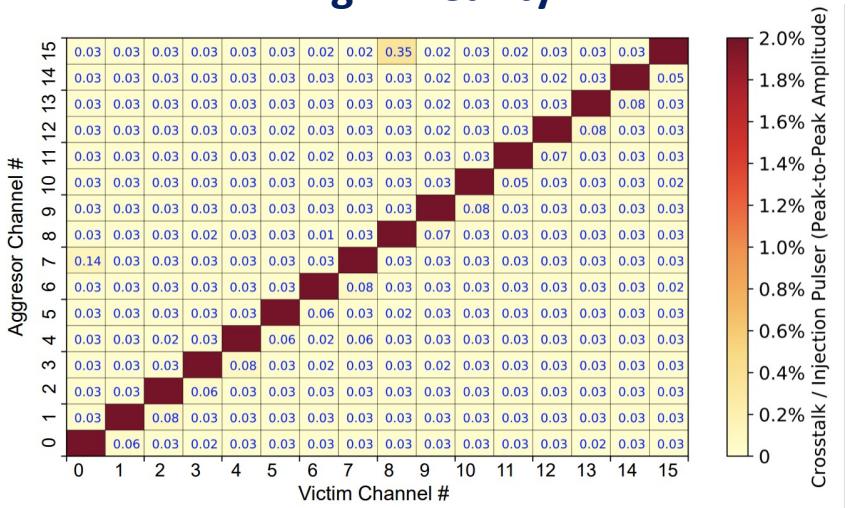
- Both CHARMS250V2A and V2B design prototypes to be fabricated in early 2027.
- Future work includes R&D for CHARMS10 with wide-dynamic range and shortest peaking time down to 10 ns.

Backup Slides

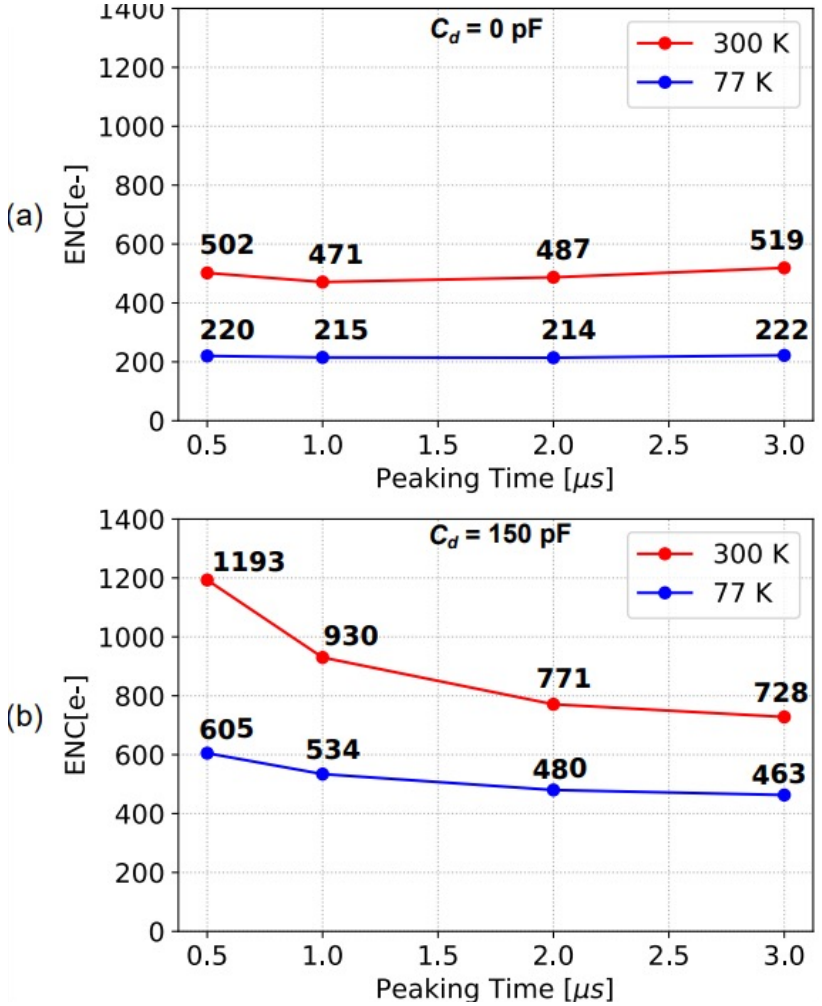
LArASIC measurement results



High linearity



Low crosstalk (mean: 0.04%)



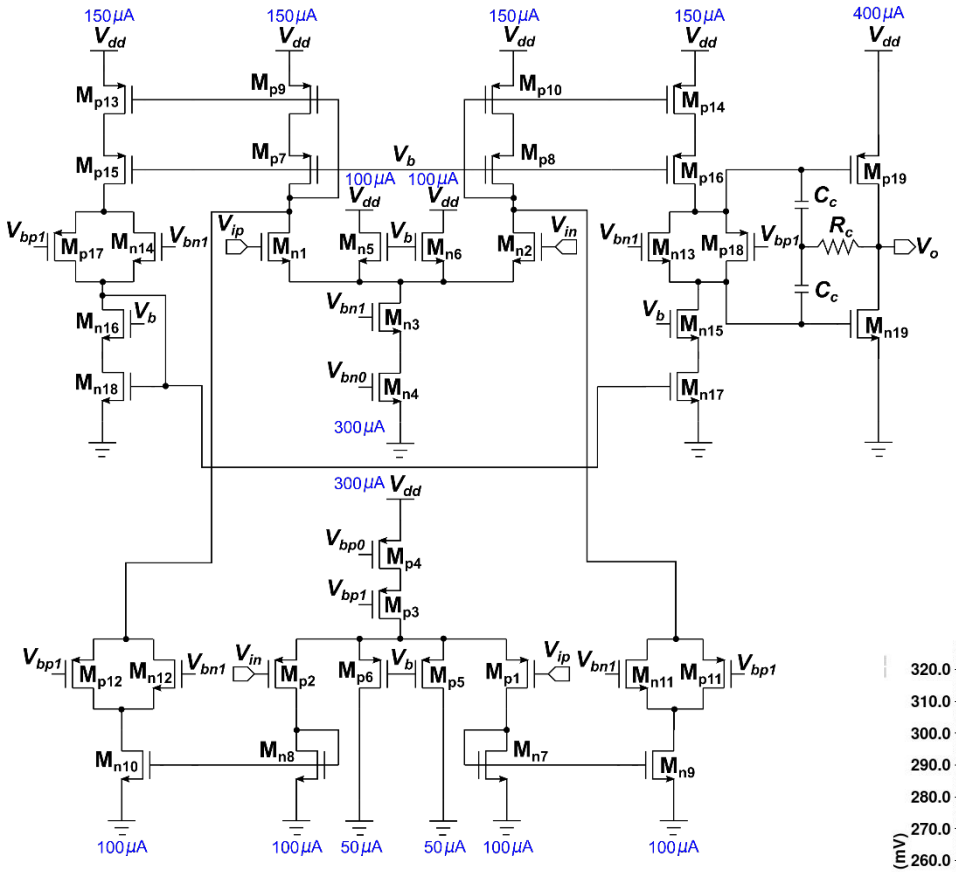
Low noise

Temperature	Baseline	Power consumption (mW)		
		Buffers off	SE on	SEDC on
300 K	200 mV	5.6	9.0	10.7
77 K	200 mV	5.3	8.8	10.8
300 K	900 mV	5.8	9.5	10.6
77 K	900 mV	5.5	9.1	10.5

Power consumption

Brookhaven National Laboratory

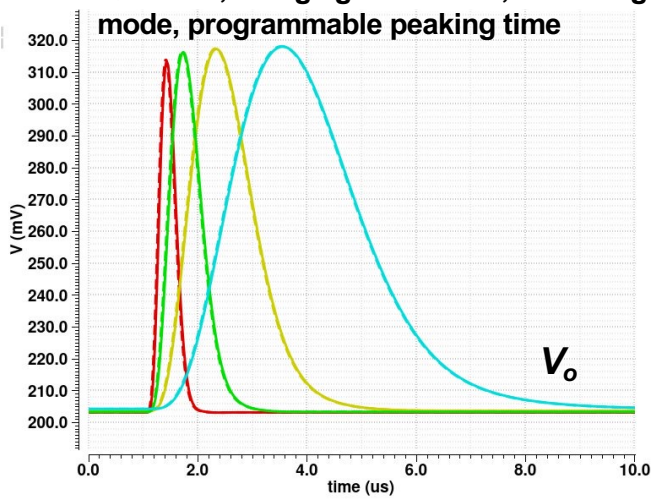
Output buffer design – single ended (SE) buffer



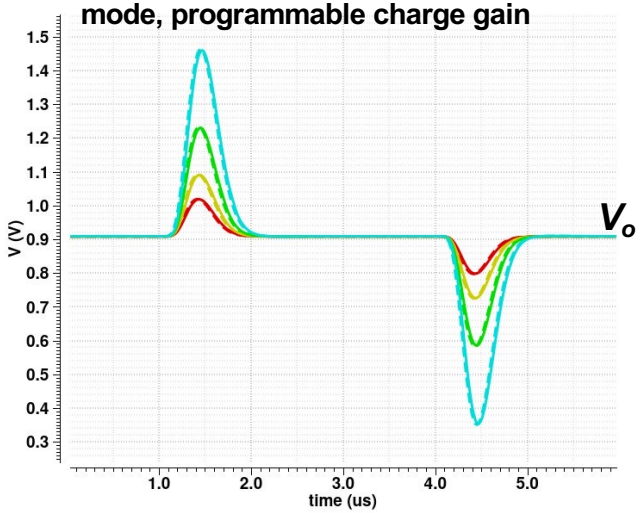
- Based on a folded-cascode current-mirror based operational transconductance amplifier
- Comprises of parallel NMOS and PMOS input pairs to support rail-to-rail operation
- Monticelli class-AB output stage used
- High open-loop DC gain (> 110 dB at LArT) ensures minimal introduction of distortions in the output signal
- Suitable to drive tens of pF of capacitance load (chip-to-chip trace)

SE Buffer impulse response with 100 pF load

Q = 25 fC, charge gain = 20 x 3, collecting mode, programmable peaking time

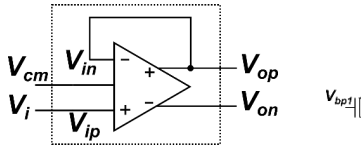


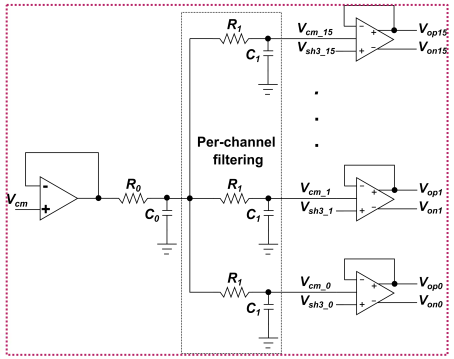
Q = 25 fC, peaking time = 250 ns, non-collecting mode, programmable charge gain



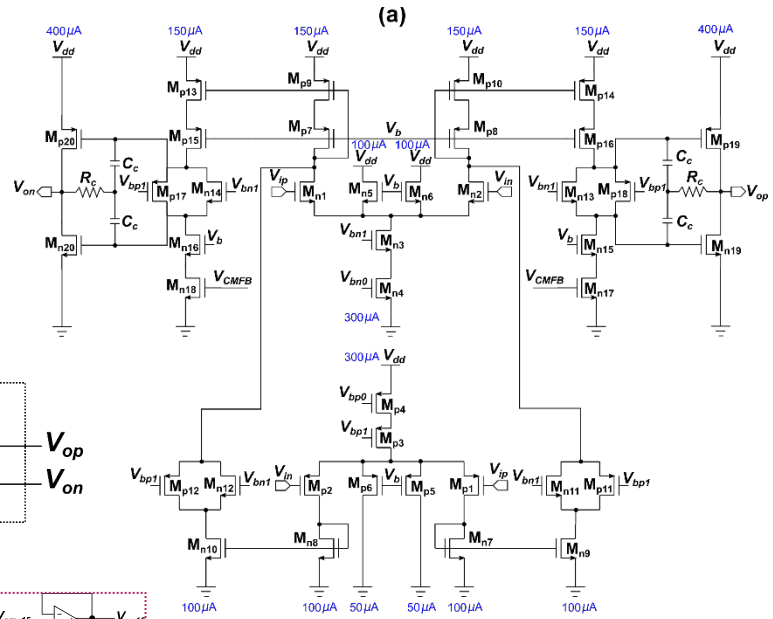
Brookhaven National Laboratory

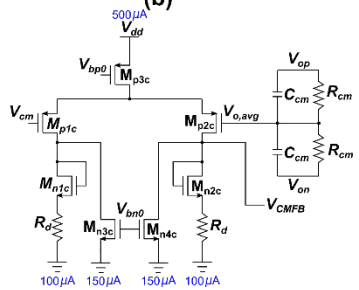
Output buffer design – single ended (SEDC) buffer





Main loop



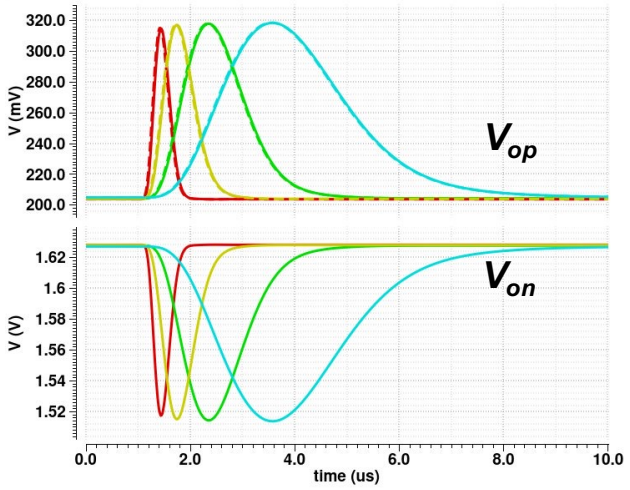


CMFB loop

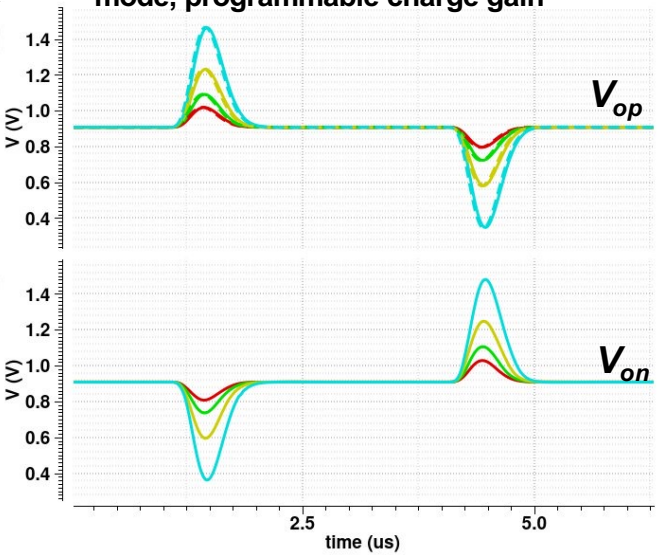
- Simpler, more compact and power-efficient compared to resistor or 3-operational amplifier based SEDC designs
- Circuit implementation similar to SE buffer, but core is fully-differential (inputs and outputs)
- Noise transferred from common-mode input signal (V_{cm}) to the output with 6 dB gain
- Global and local noise filtering implemented for V_{cm}
- Both common-mode and differential paths have high open loop DC voltage gains (> 110 dB) and comparable bandwidths (≈100 MHz) at LArT
- Helps with crosstalk cancellation

SEDC Buffer impulse response with 100 pF load

Q = 25 fC, charge gain = 20 x 3, collecting mode, programmable peaking time

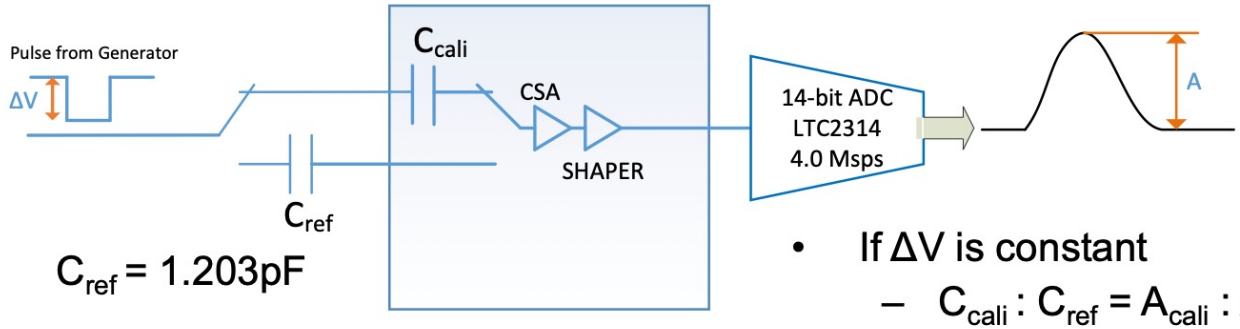


Q = 25 fC, peaking time = 250 ns, non-collecting mode, programmable charge gain

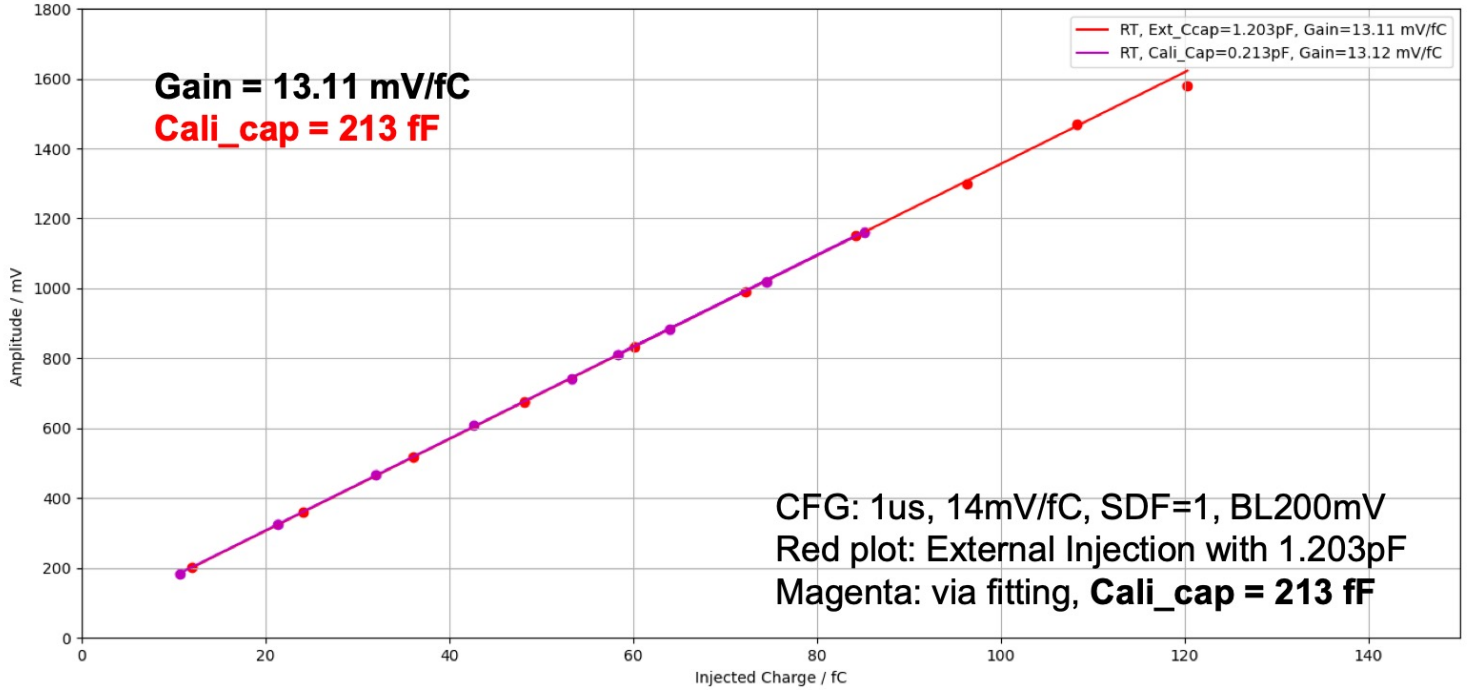
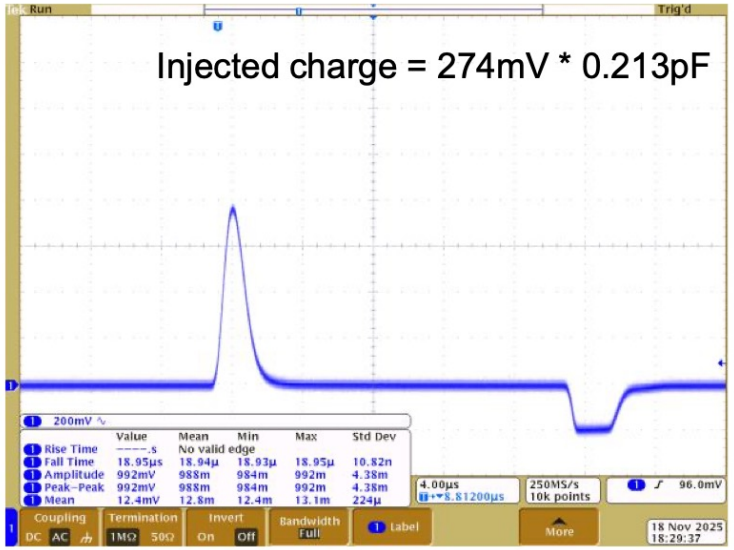
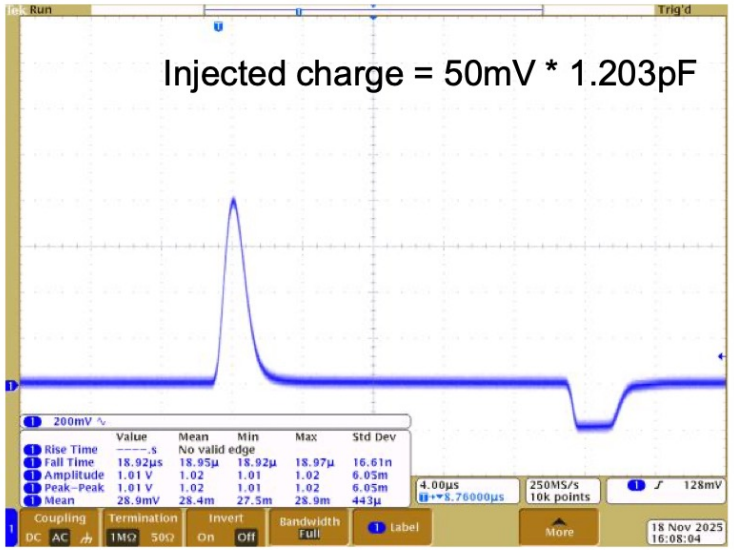


Brookhaven National Laboratory

Embedded Calibration Capacitor measurement



C_{ref} = 1.203pF

- If ΔV is constant
  - $C_{cali} : C_{ref} = A_{cali} : A_{ref}$

C_{cali} is MIM (Metal-Insulator-Metal) capacitor, low temperature coefficient .