
LArPix and Related Developments in Scalable Electronics for Noble Liquid Detectors

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3D LArTPC Readout Concept: LArPix

Concept:

- Use grid of charge-collecting pixels/pads for anode
- Uniquely identify signals on each pixel
- Provides true 3D imaging of TPC ionization

Technical Challenges:

High channel density:

$O(100k)$ pixels/ m^2 of anode area

Low noise:

<1000 e⁻ equivalent noise charge (ENC)

Low power / Cryo-compatible:

Stringent limits on heat load in cryogenic environment, $O(10)$ W/ m^2

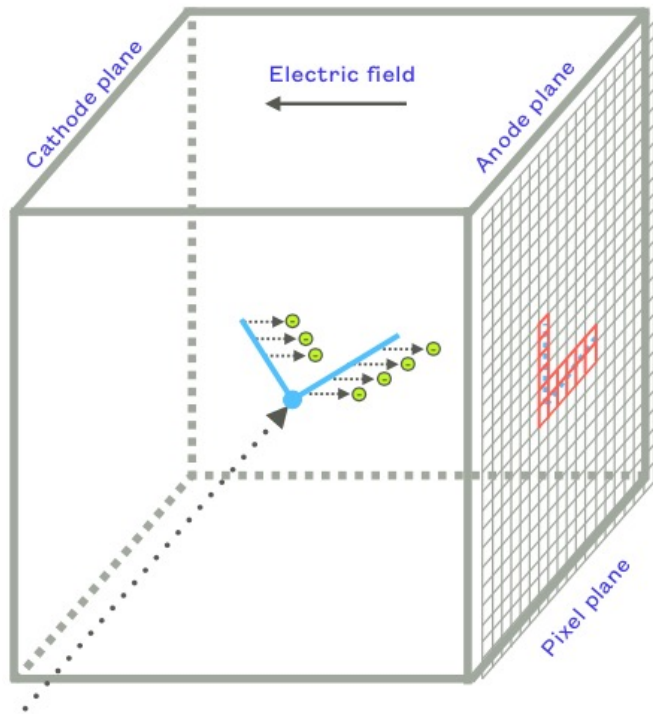
Electronics behavior stable & predictable at LAr temp (87 K)

Digital multiplexing:

Must reliably transmit $O(10k)$ pixel signals through few wires

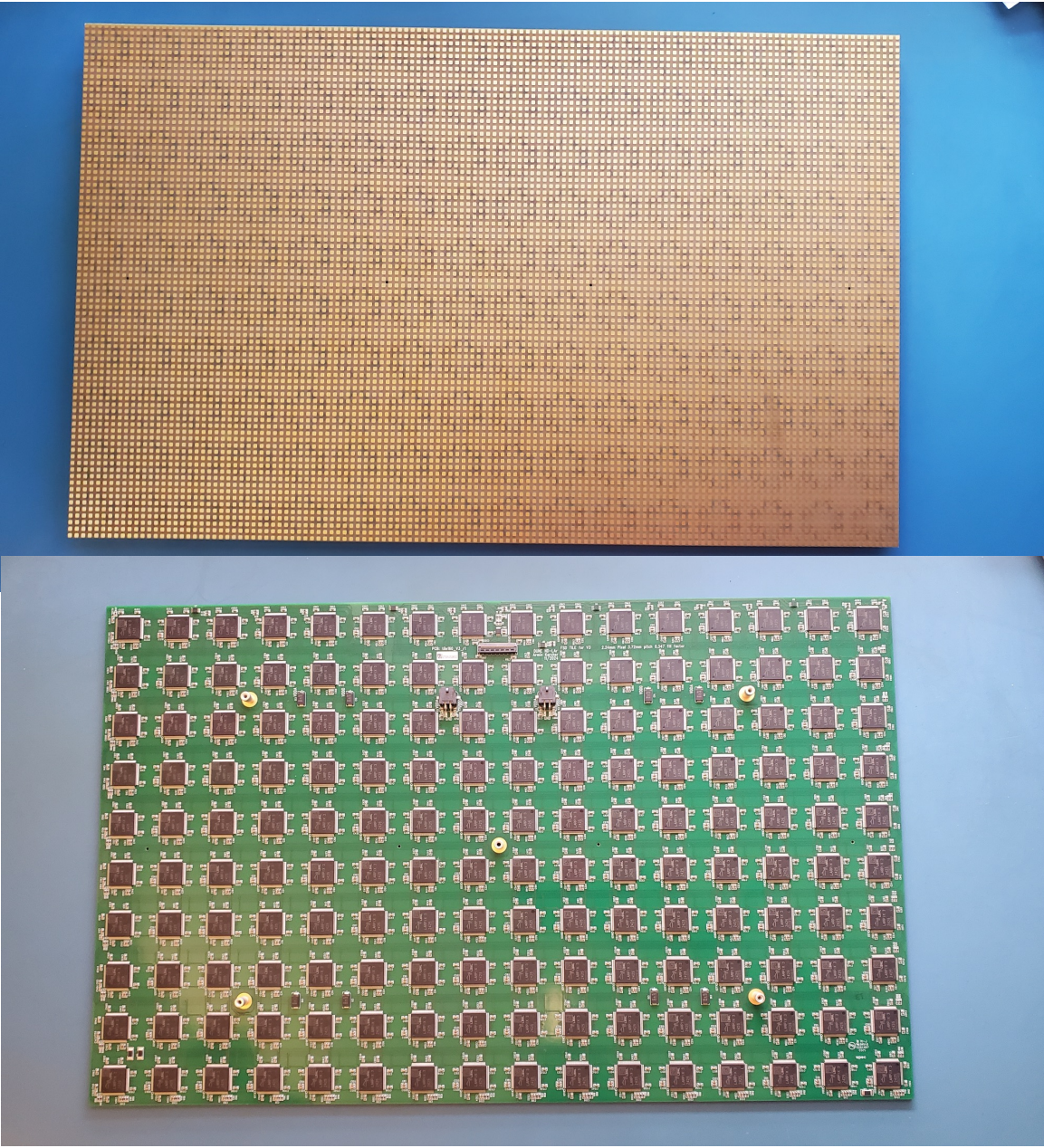
Scalability:

Design and production method must scale to $\sim 10^7$ pixels to be viable for the DUNE Near Detector



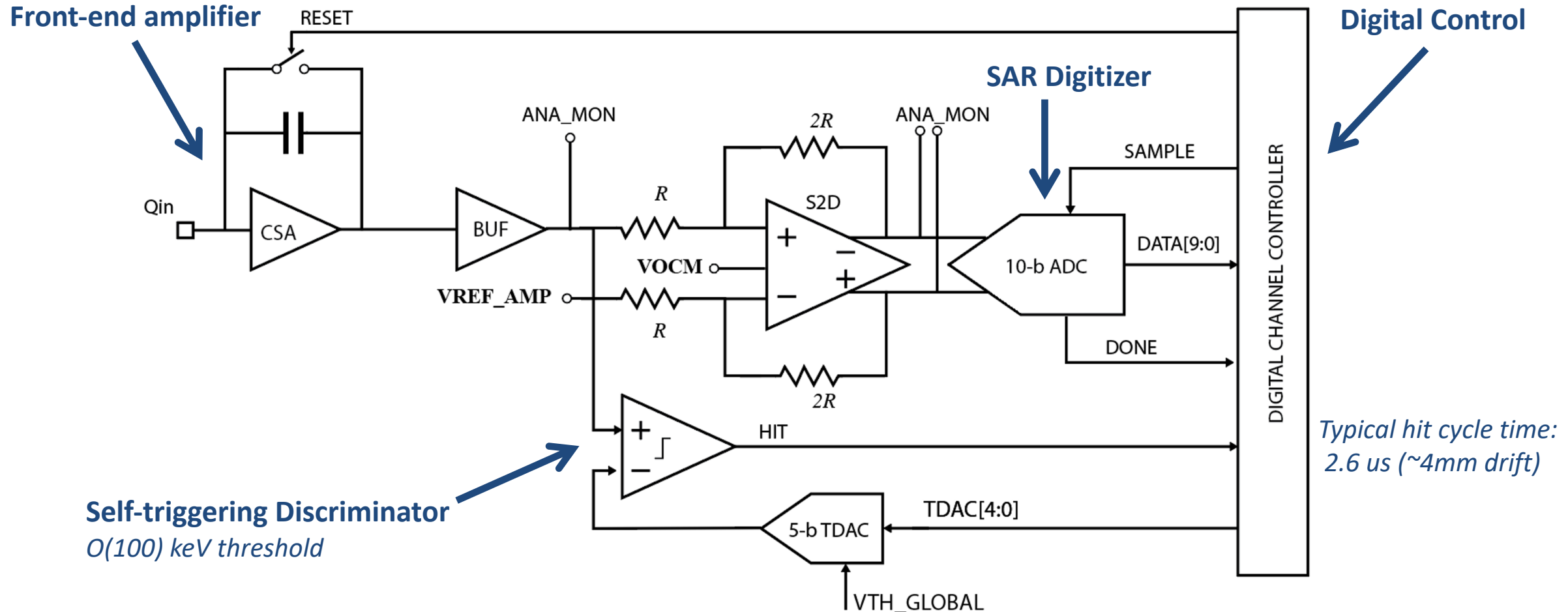
3D Pixel TPC

10k-channel LArPix prototype pixel anode tile



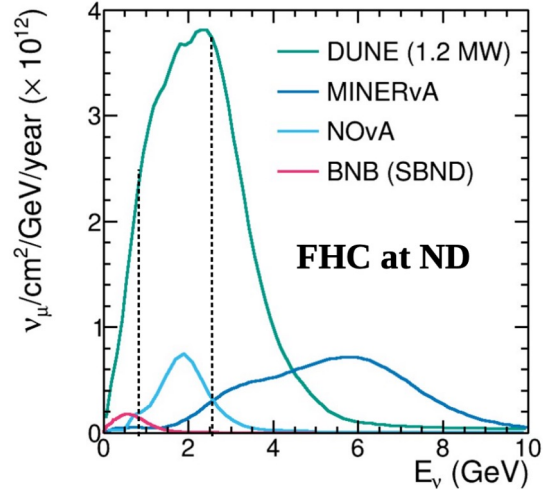
LArPix Concept

Approach: Integrating Amplifier with Self-triggered Digitization and Streaming Readout



Achieve low power: avoid digitization and readout of mostly quiescent data.

LArPix and The DUNE Liquid Argon Near Detector (ND-LAr)



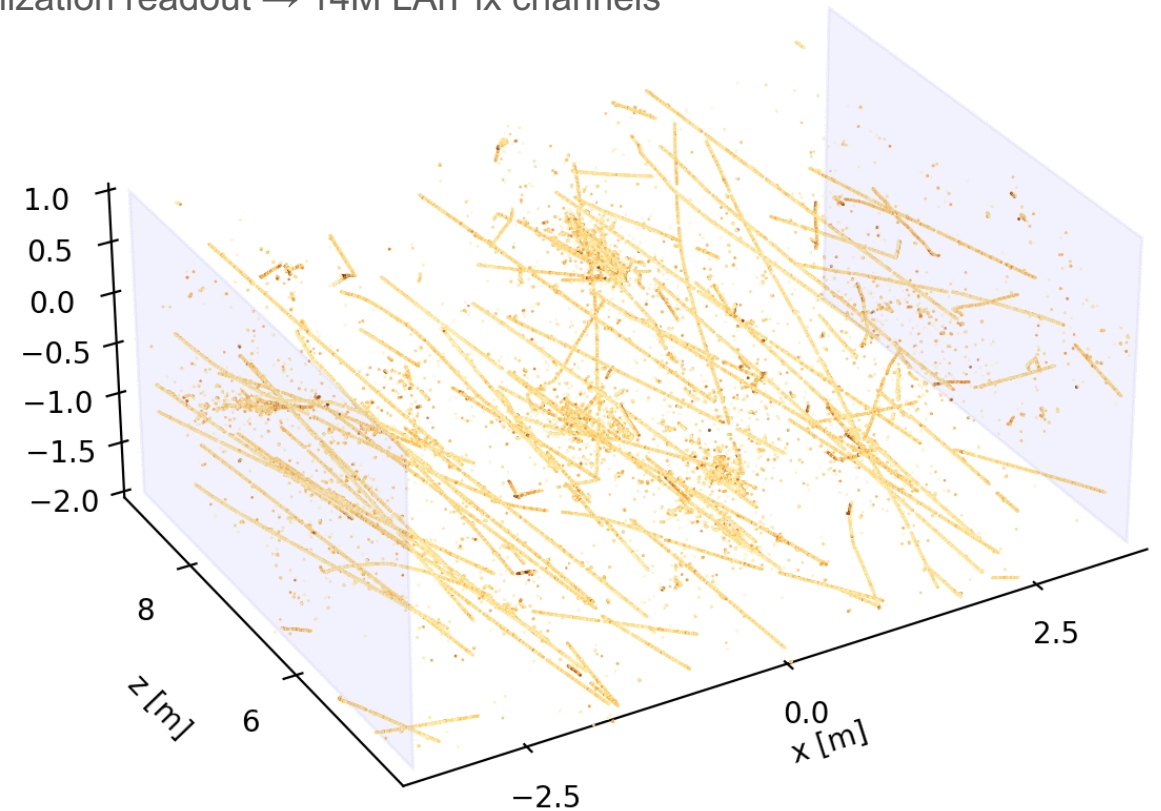
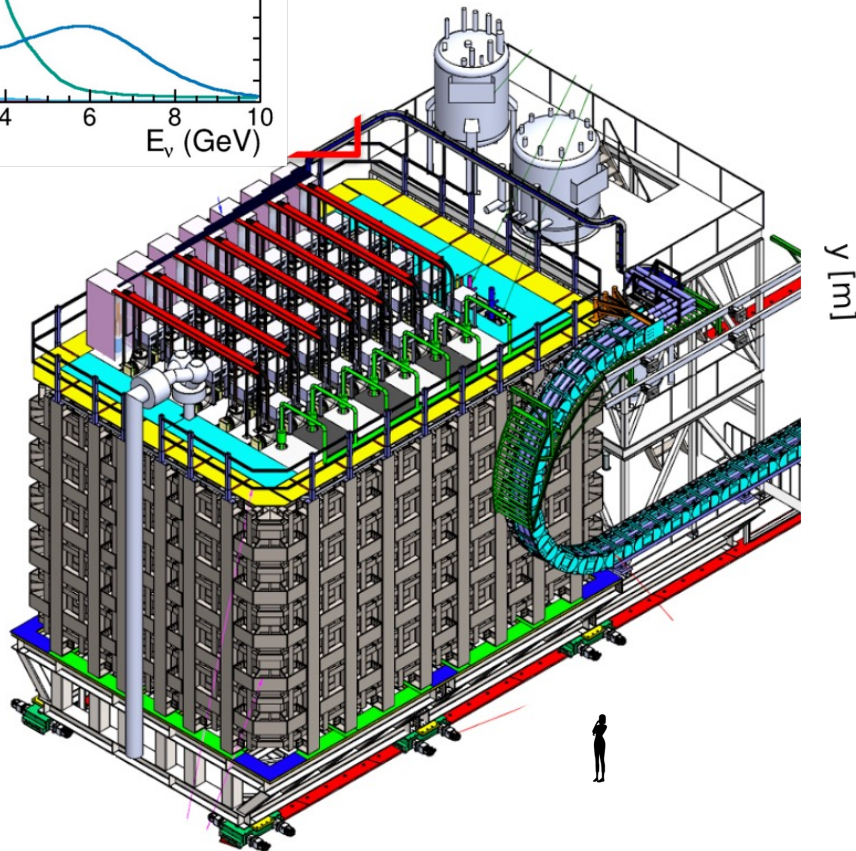
Neutrino Pileup:

- LBNF beam intensity results in $O(100)$ interactions visible in ND-LAr per 10 μs beam pulse.
(Compare to ionization readout time of $\sim 300\mu\text{s}$ and scintillation readout time of $\sim 10\text{ns}$)

Pileup Mitigations:

- Optically segmented (70 regions) with $\sim 30\%$ optical coverage per segment
- Native 3D pixelated ionization readout $\rightarrow$ 14M LArPix channels

Engineering
model of
ND-LAr
detector



*LBNF Beam Pulse Simulation in ND-LAr (May 2025)
(DUNE Work-in-Progress)*

DUNE ND-LAr Prototype: 2x2 Demonstrator

Description:

- Four mid-scale Pixelated LArTPC modules, 2.4 tons total, >300k pixels
- Includes upstream/downstream steel/scintillator trackers, repurposed from MINERvA experiment
- Located in underground hall in NuMI neutrino beam at FNAL

Run #1: First antineutrinos *July 8-12, 2024*

- Collected initial ~40k antineutrino interactions in 4.5 days

Run #2: Tuning and Calibration Studies *Oct-Dec, 2025*

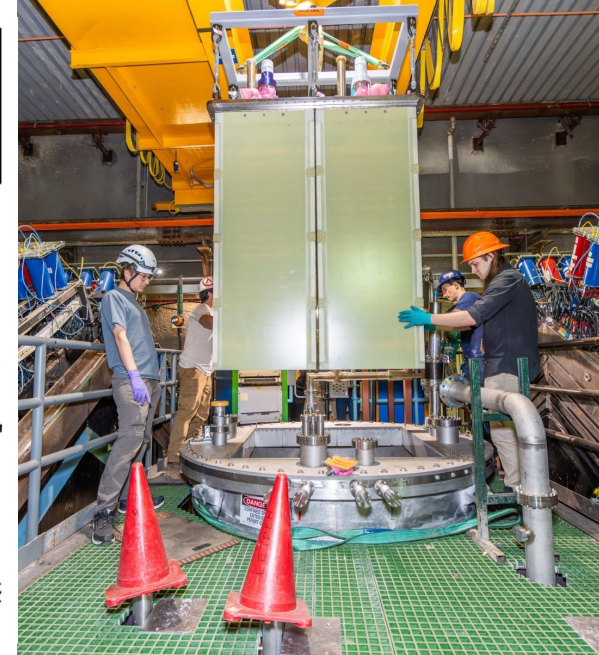
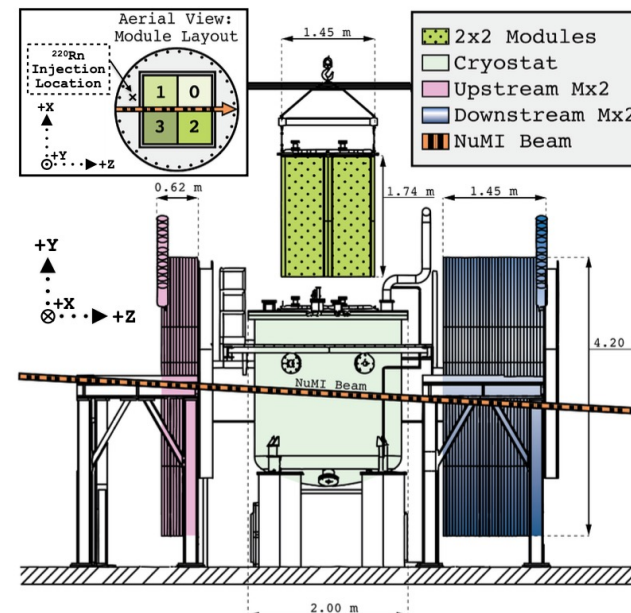
- Improved tuning of pixel and scintillation light readout systems
- Performed Calibrations:
 - External sources: ^{22}Na , ^{60}Co , ^{88}Y , AmBe, DT Generator
 - ^{220}Rn injection

Run #3: Return of the NuMI neutrino beam *Oct. 2026 → 2027*

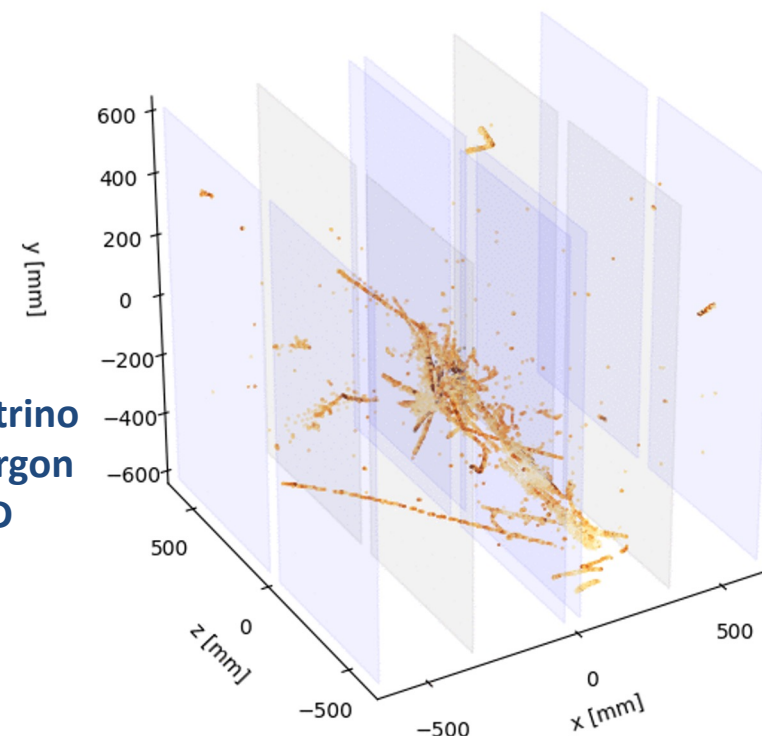
- Detector refilled/recommissioned over past month
- Neutrino beam returned **yesterday** (Oct. 21).
- Expect beam through early 2027 ($\sim 2 \times 10^{20}$ protons-on-target)

Performance of a Modular Ton-Scale Pixel-Readout Liquid Argon Time Projection Chamber
Instruments **2024**, 8(3), 41

Operation of a Modular 3D-Pixelated Liquid Argon Time-Projection Chamber in a Neutrino Beam
Instruments **2026**, 10(1), 18



Example antineutrino interactions on argon imaged in true 3D during Run #1



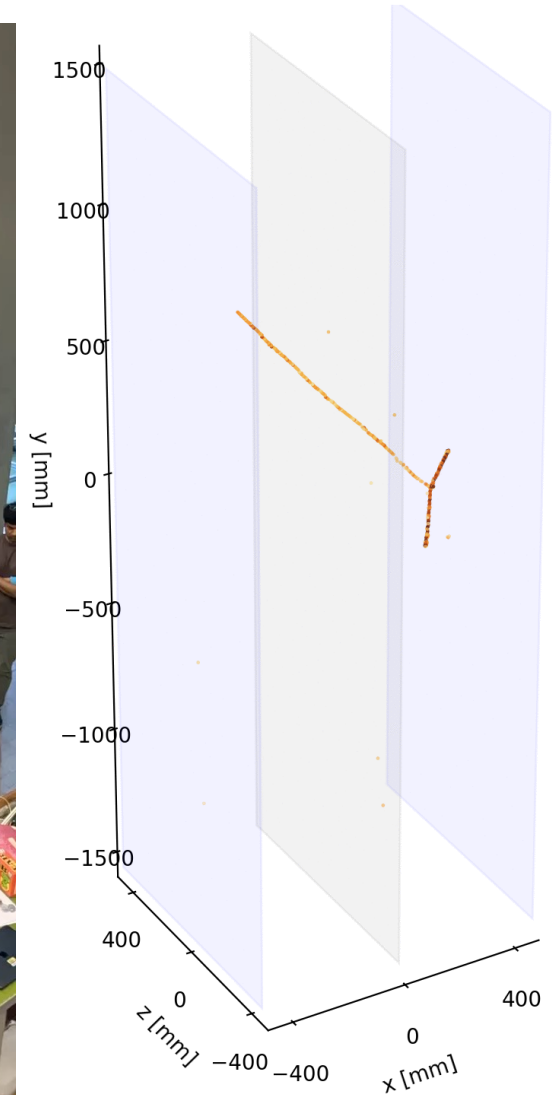
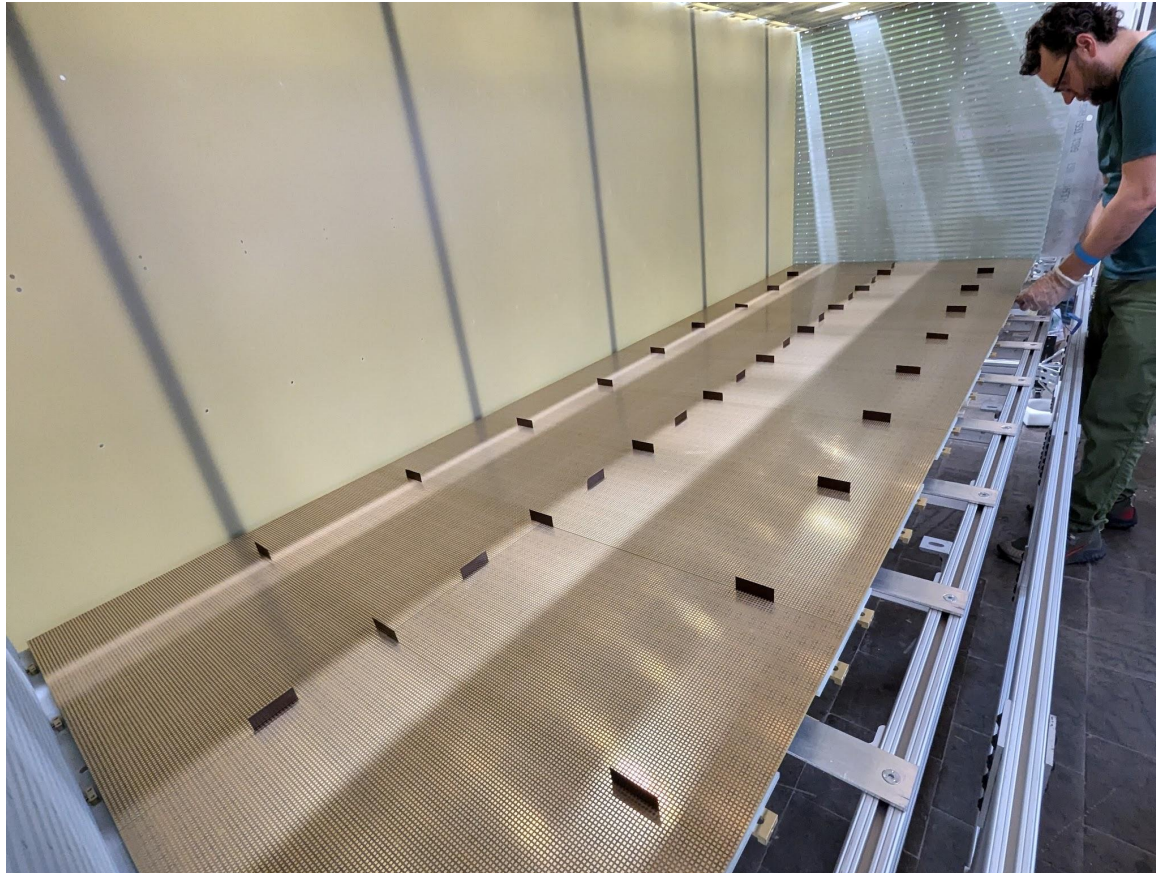
ND-LAr Full-Scale Demonstrator @ Univ. of Bern

Example cosmic ray images

Event 132, ID 132 - 2024-11-06 21:02:59 UTC

Full-Scale Demonstrator:

- Built/operated first full-sized ND-LAr TPC module in late 2024
- Used 40 LArPix-v2d tiles, >400k pixels



Developments in System Reliability: Hydra-I/O

Designed for robust I/O and control architecture

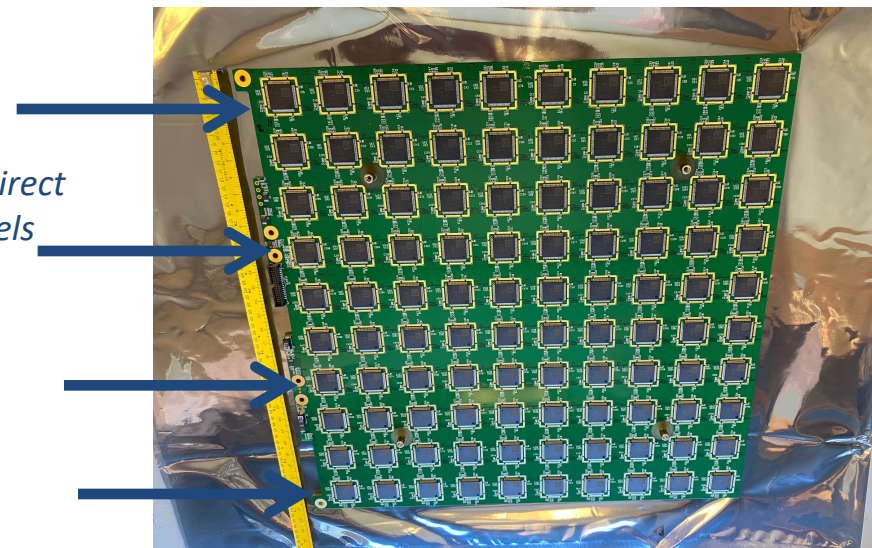
Difficult to access & repair electronics within large LAr cryostats

Hydra-I/O prevents tile failure due to single-chip errors

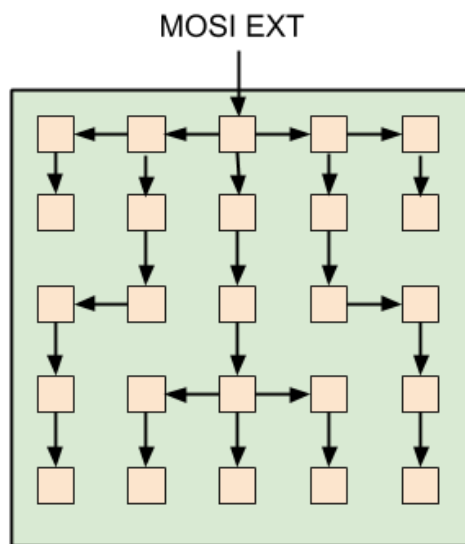
- I/O can occur between any neighboring chips on pixel tile
- Network is built by programming I/O connections between neighboring ASICs

Successfully exercised with LArPix-v2 chip in 2x2 Demonstrator Program

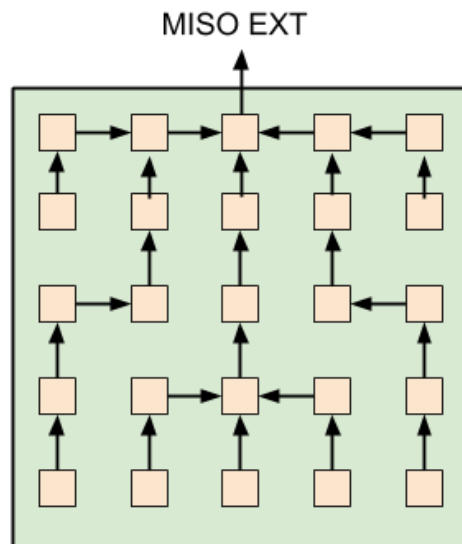
Four chips have direct off-tile I/O channels
(10 MHz, < 7 m)



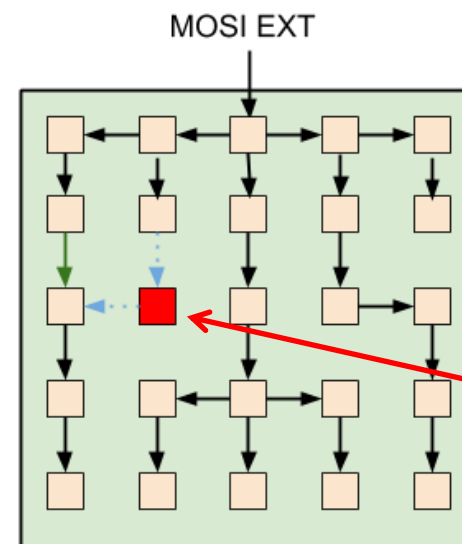
Example: 5 x 5 Pixel Tile



Upstream configuration commands



Downstream data flow



Example failed chip.

Network reconfigured to avoid failed ASIC

Major Lessons from the LArPix-v2 Era

Cryo-compatibility

- Established a design that meets requirements for cryo-operation (performance at 87 K, heat management to avoid boiling LAr)
- Vast majority of performance quality issues identified at room temp; few new problems emerge at LAr temp

Reliability

- System design sufficiently reliable to field two multi-ton LArTPCs
- Hydra-I/O successfully mitigates issues from problematic chips and unreliable I/O channels

Scalability

- Demonstrated a scalable design, fully produced by leveraging standard ASIC and PCB production processes.
- Developed testing program, identifying areas for improvement in advance of production
- Achieved target of O(10) cents per channel for full-system production cost

Signal Fidelity:

- Refined anode grounding to mitigate microphonic-related noise at tile-to-tile boundaries
- Must consider small (but non-negligible) signals from ionization e- collected by other pixels
- Need 10-bit ADC in order to reduce quantization noise (250 e- least-significant-bit) and capture 250k e- maximum signal.

LArPix-v3: Honing in on the ND-LAr final design (2025-2026)

Final (v3c) channel structure

v3 Strategy:

- Multiple minor iterations in quick succession to accelerate pace of prototype-based verification

Increase the LArPix dynamic range:

v3a:

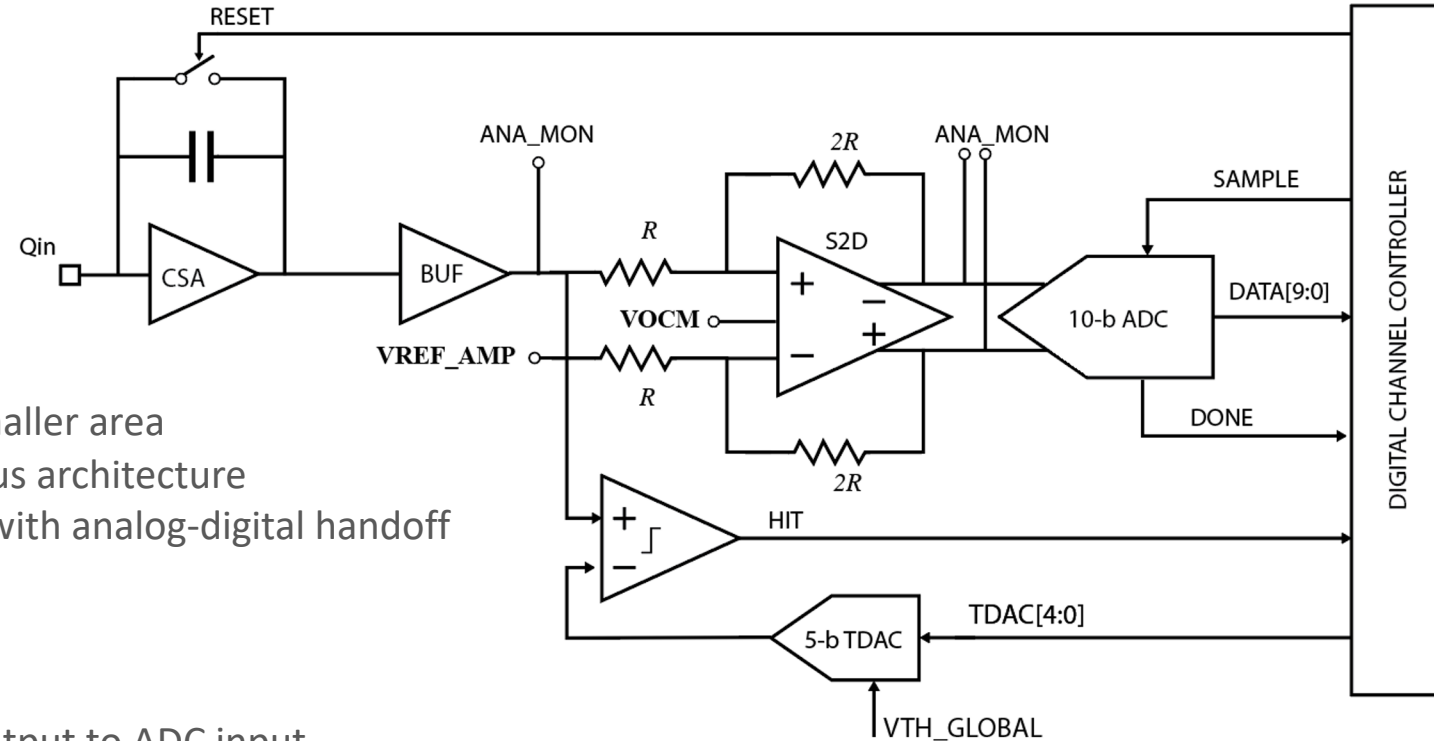
- Replace the 8-bit SAR ADC with a 10-bit SAR
- Differential: Meets power & performance targets in smaller area
- Asynchronous: Faster conversion time than synchronous architecture
- Results: 10-bit ADC successful, with only minor issues with analog-digital handoff

v3b:

- Addressed analog-digital handoff (FIXED)

v3c:

- Add Single-to-Differential (S2D) buffer to match AFE output to ADC input



Resolve issues with data loss:

v3b: Restructure digital core to simplify internal state machines. -> *More significant re-write than originally planned.*

- Results: Simplified code, but **did not resolve data loss** (insufficient validation of significant RTL revision)

v3c: Minor refinements of digital core to fully address data loss.

- Implemented much more significant design verification, code coverage now ~90%; one new subtle bug identified and resolved.
- Completing top-level integration, final verification ← **We are here**

LArPix-v3c: Improvements in ASIC Design Verification

Core Verification: T. Prakash, P. Zarkos, K. Papadopoulou, D. Gnani (LBNL Eng Division); J. Hoff (FNAL)

- Relies on targeted test design and execution using traditional ASIC design toolkits
- Digital: Constrained-random test bench
 - Single-chip and 3x3 multi-chip test bench environments
 - Implemented code coverage and functional coverage tracking
 - Daily automated regression test suite
- Analog & Mixed Signal:
 - 4-corner simulation of gain, BW, phase margin, noise, and power for key amplifier and buffer blocks
 - Mixed signal channel simulation with analog and compiled RTL
 - Full analog-on-top chip-level simulation

New FPGA-based Verification: N. Patras (LBNL Computing Division)

Joint with NIFTY program (see upcoming slide)

- Implement LArPix digital design on an FPGA
- 3 x 3 network of LArPix ASICs in a single FPGA
- Enables higher-speed execution of subset of LArPix digital tests
- Identified rare deadlock issue in v3c design, and verified fix

New RTLSwarm Verification: K. Gosine, Y. Mei (UTA)

See CPAD talk by K. Gosine!

- Implements clock-accurate RTL model of LArPix on a CPU, with inter-chip communication parallelized on a CPU cluster
- Enables digital tests of full-sized network of LArPix ASICs (160 chips)
- Independently identified v3b data loss issues, and verified v3c fixes

Pixelating a DUNE Far Detector

Goal

Demonstrate LArPix 'Charge Readout Plane' compatible with DUNE Far Detector design

LArPix in CERN NP02 'Cold Box':

- Install 3m x 3.4m LArPix anode (614k pixels) in CERN Vertical Drift Cold Box
- Demonstrate performance and interfaces
- Target: Collect ~1 week of cosmic ray test data in Nov. 2026

Next Step: ProtoDUNE Run-III

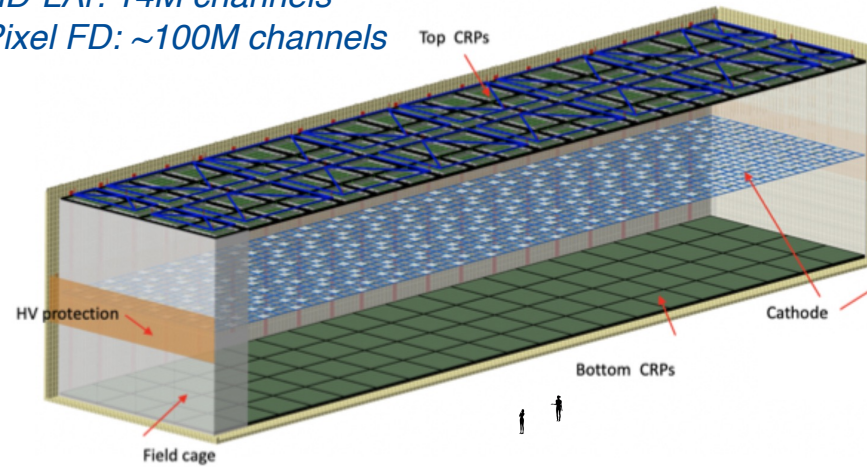
- Install LArPix anode in ProtoDUNE, operate in ~2029
- Develop MADCAP cryo-data multiplexer
- Endorsed by DUNE Collaboration

*See CPAD talk
by R. Huang!*

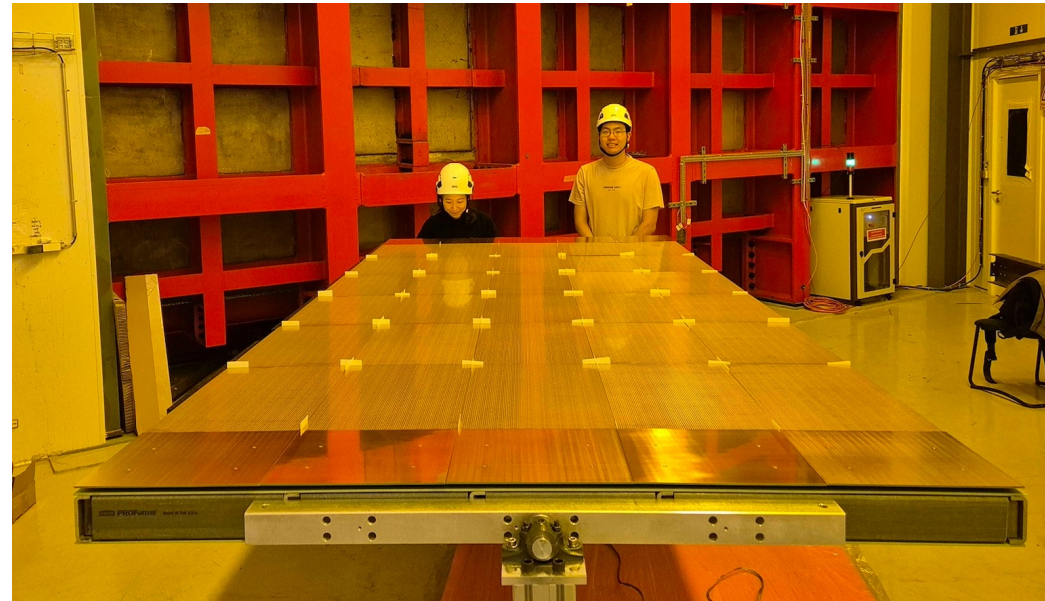
DUNE Vertical-Drift Far Detector Design (~15 kton)

ND-LAr: 14M channels

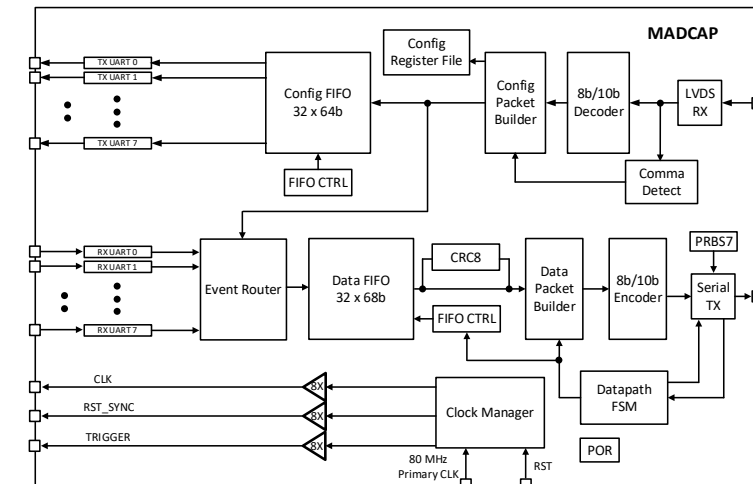
Pixel FD: ~100M channels



Composite Frame Assembly (@Univ. of Bern)
and Cryo-test (@ Grenoble)



Pixel Tile Installation on Composite Frame
(@ CERN Neutrino Platform)



MADCAP-v1 Cryo-Multiplexer ASIC
(in collab with INFN M-B)

Pixel TPC Kits supporting Detector R&D

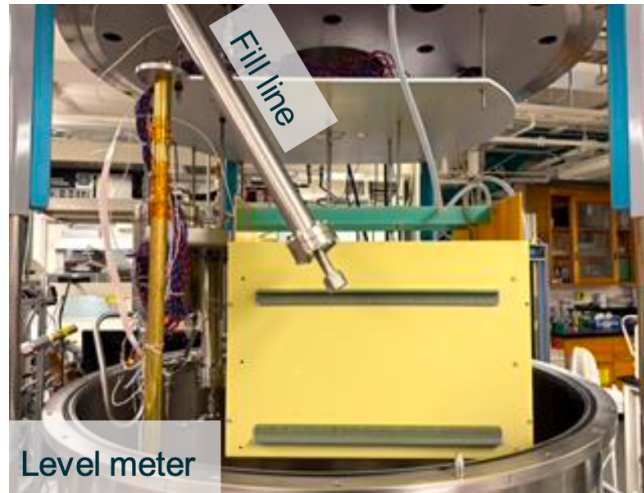
*CERN DRD2:
WP 4.3, Task G1.D3*

Fabricated multiple TPC kits in support of distributed R&D:

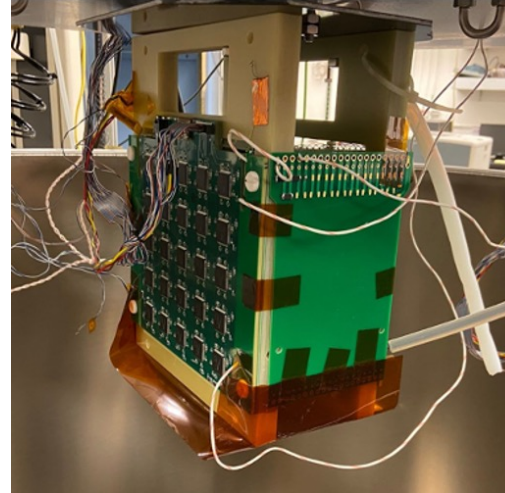
- Small kit: 15 cm x 15 cm anode, 10 cm drift, 1600 pixels
- Large kit: 32 cm x 48 cm anode, 48 cm drift, 10k pixels
- Both include complete readout system
- Requires: Cryogenics system with sufficient e- lifetime

Recent Applications:

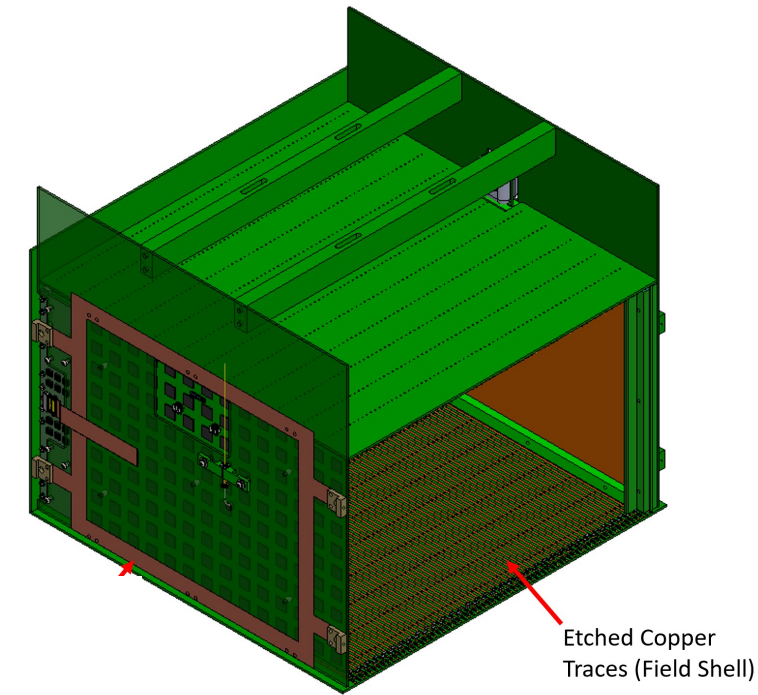
- Validation tests of LArPix-v3 ASIC (@ Berkeley Lab)
- Tests of photosensitive dopants (@ Fermilab)
- Development of Radon injection for calibration (@ CSU)
- Test of UV-laser calibration (@SLAC)
- Prototyping of anode shield plane for signal shaping (@ Berkeley Lab)



Small (1.6k-pixel) TPC Kit



**Large Kit
installed in
test cryostat
@ LBNL**



Large (10k-pixel) TPC Kit



TPC Kit Example: Anode Shield R&D

Goal:

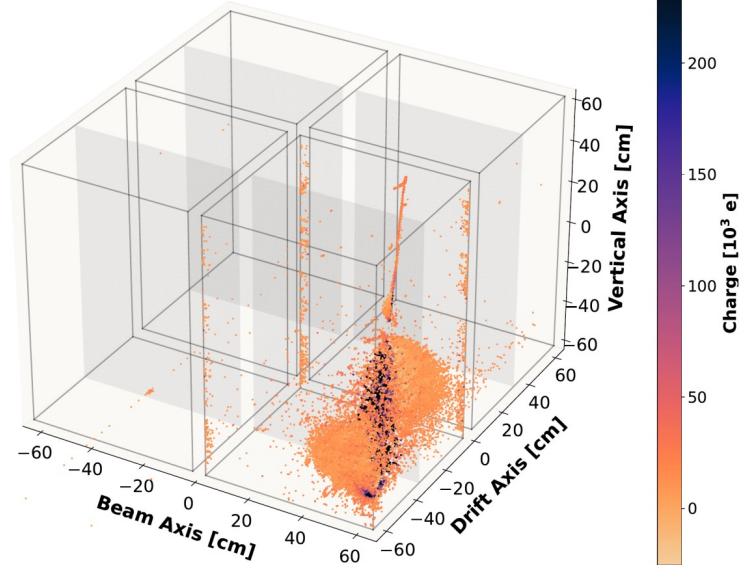
- Reduce signal induction from e^- drift to very near field (few-mm)
- Significant pre-triggering observed during very large particle showers

Details:

- Add copper-clad & perforated PCB in front of anode tile
- Bias to ~ -1 kV to ensure ionization e^- collected on anode

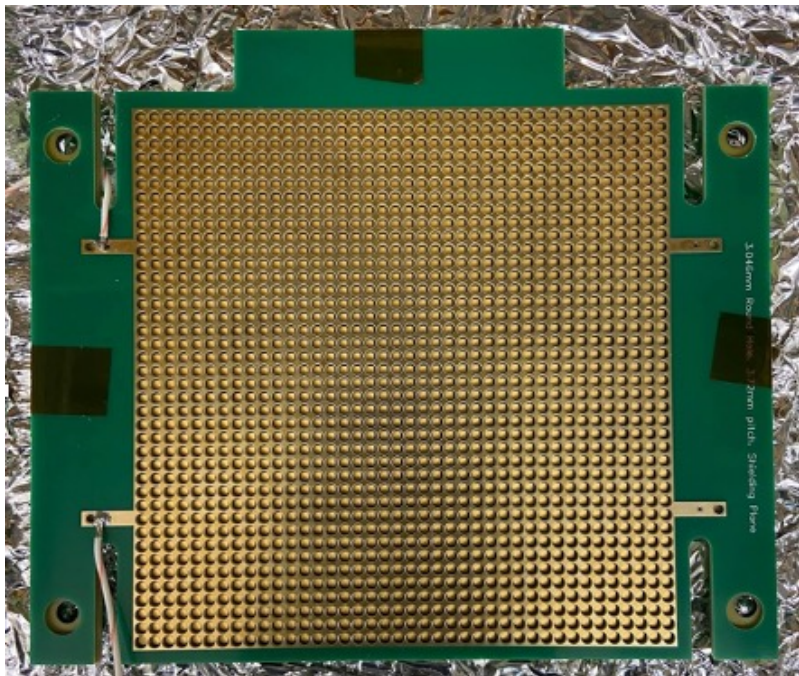
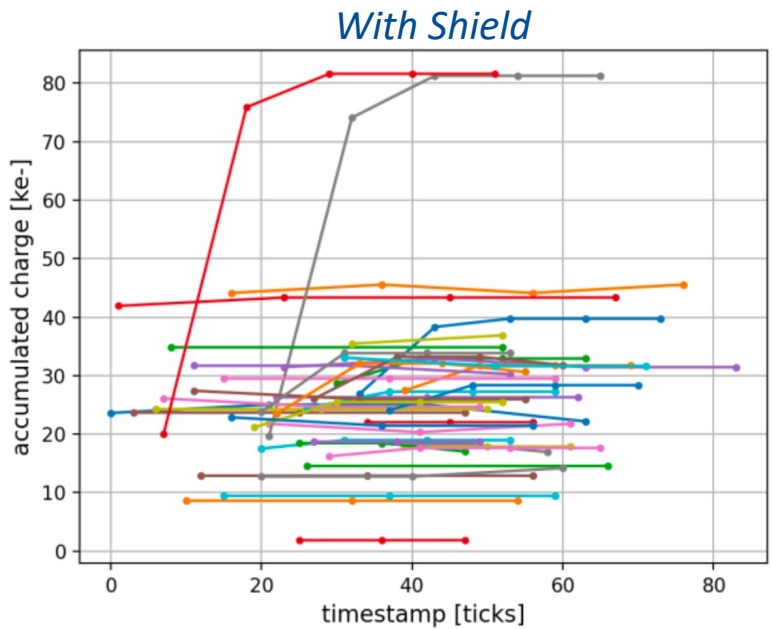
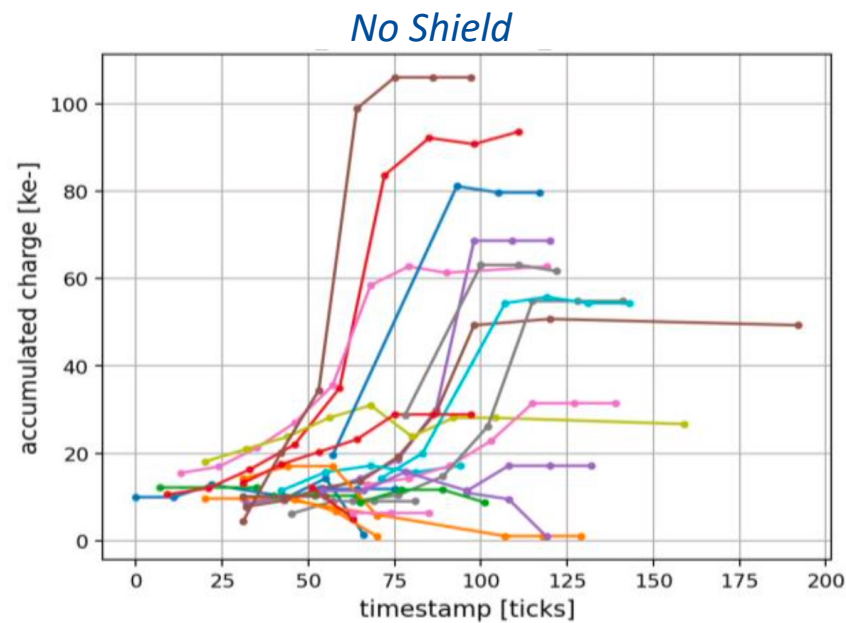
Key Challenges:

- HV discharge risk, leakage currents, scalable manufacturing



Pretriggering during large cosmic shower in 2x2 Demonstrator

Prototype Shield Plane (from HKUST) on 1.6k-pixel Tile



Data shows expected sharpening of time profile of integral charge on pixel from muon tracks

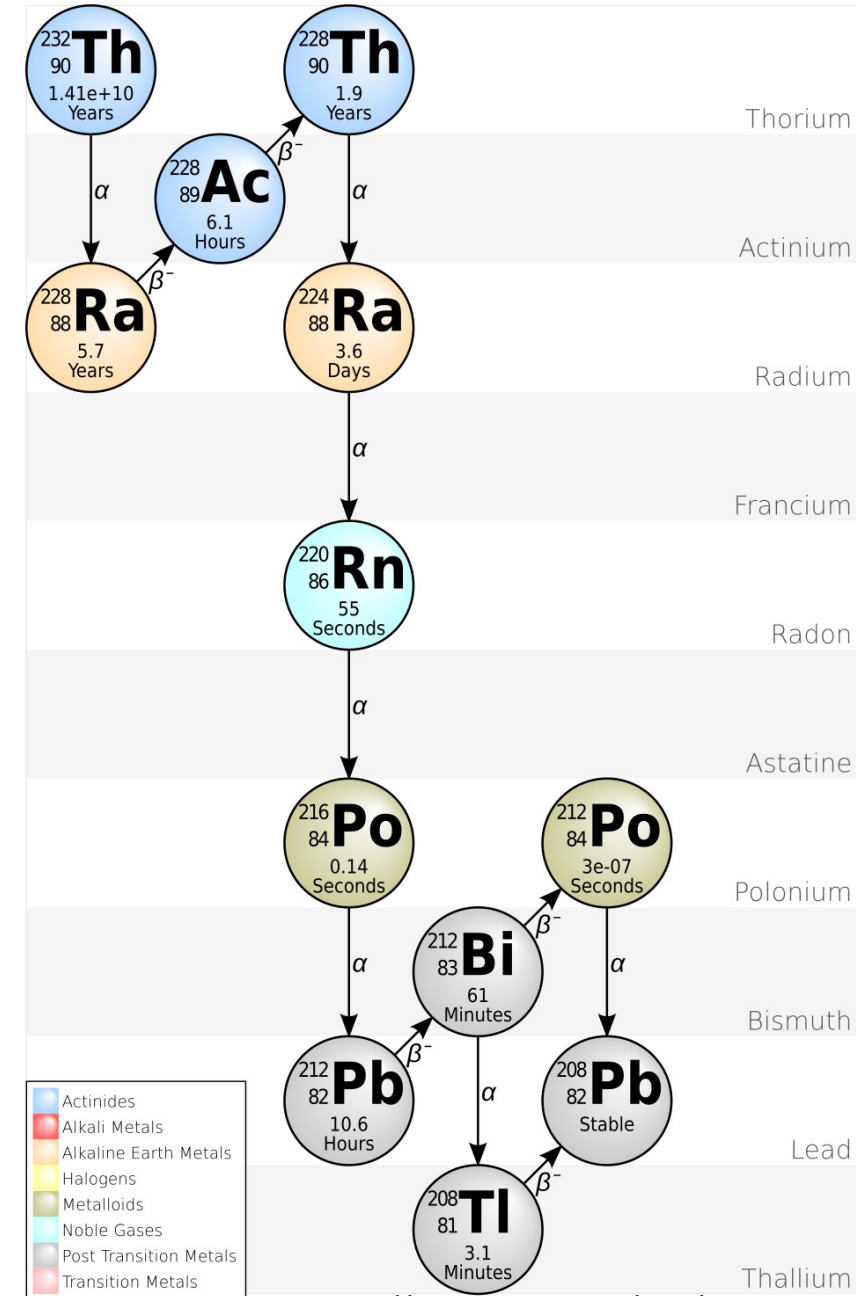
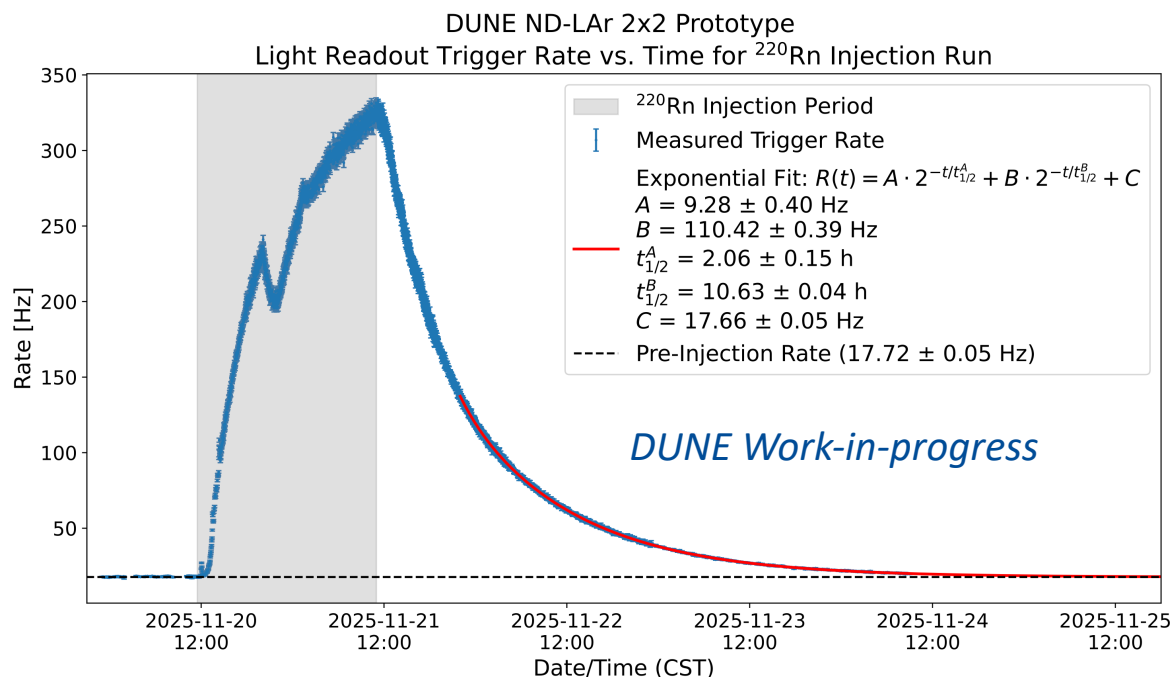
TPC Kit Example: Radon Injection R&D

Purpose:

- Facilitate full-volume detector calibration using ^{220}Rn daughters
- Longest-lived unstable daughter: ^{212}Pb , $t_{1/2} = 10.6$ hours
- Effort driven by Mooney group at CSU

Process:

- Developed and validated the injection system using large TPC kit at CSU
- Successfully used the injection system during Run #2 of the 2x2 Demonstrator



https://en.wikipedia.org/wiki/Decay_chain

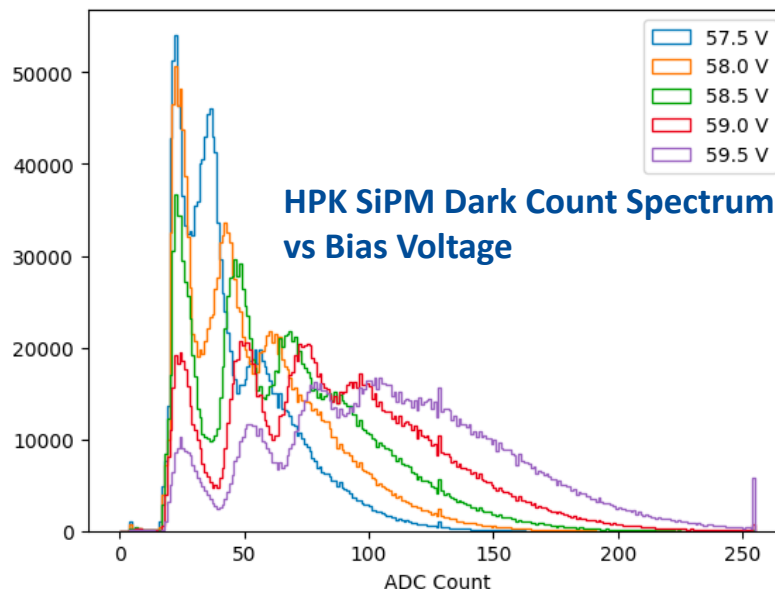
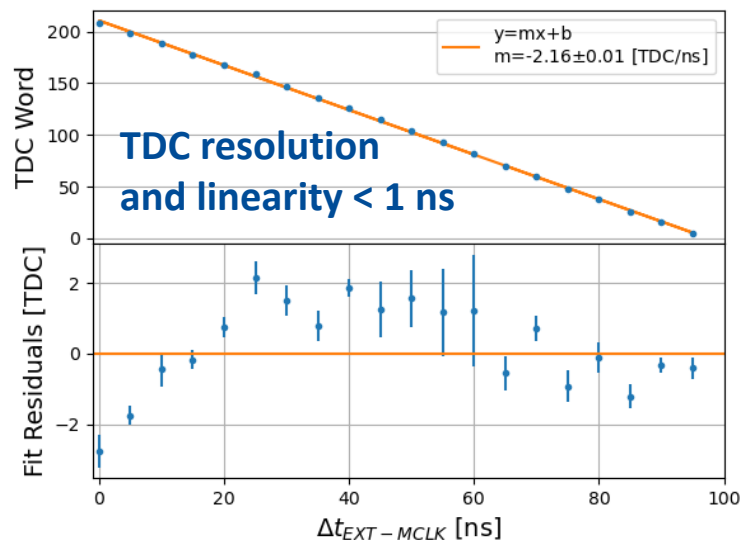
LArPix Variants: LightPix

LArPix Platform:

Provides scalable readout electronics system for detectors with $O(10)$ to $O(10^7)$ channels

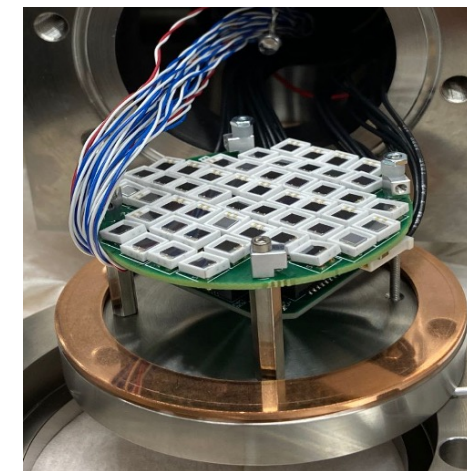
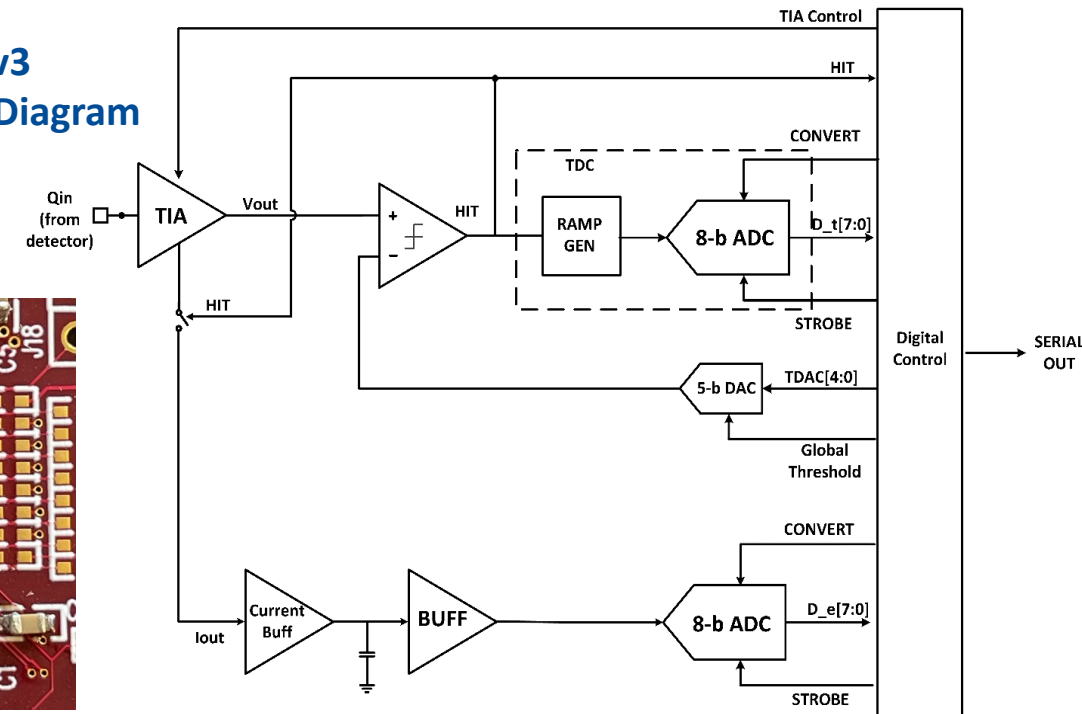
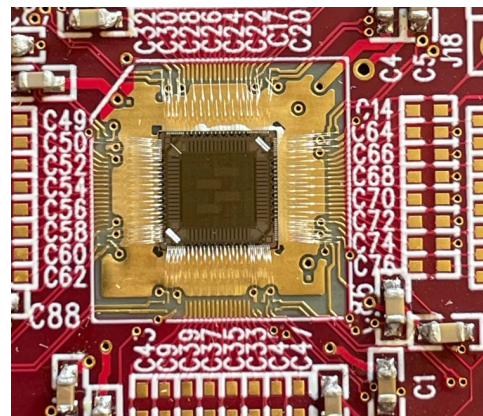
LightPix: *CERN DRD2: WP 4.3, Task G2.D4*

- Highly-granular cryo-compatible scalable SiPM readout
- Designed for high-channel counts, low occupancy
- LightPix-v3: captures arrival time with sub-ns precision and integral intensity measurement (over ~ 1 μ s)
- Collaborating with MIT and Univ. of Bern for testing



LightPix-v3 Channel Diagram

LightPix-v3 ASIC



GHe neutron detector with 300-channel LightPix Readout
(McKinsey Group, UC-Berkeley)

LArPix Variants: QPix and NIFTY

LArPix Platform:

Provides scalable readout electronics system for detectors with $O(10)$ to $O(10^7)$ channels

QPix: *CERN DRD2: WP 1, Task G1.D1*

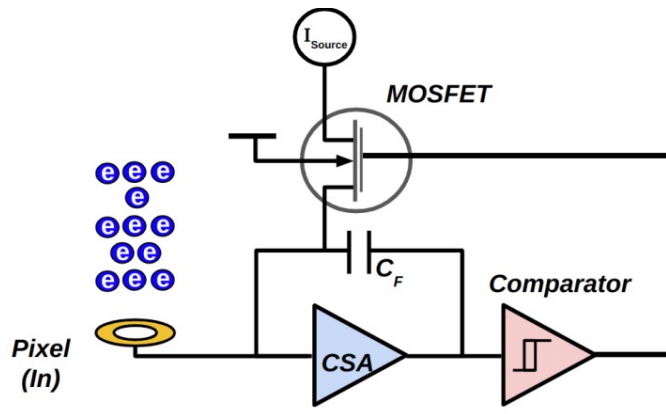
- Charge-replenishment based front-end, in collab with QPix team (UTA, et. al.)
- Exploring integration of QPix front-end into LArPix system

NIFTY:

- Hardware AI: Network Intelligence for Fault Tolerance
- Exploring novel techniques for dynamic data routing
- Simulated expected data loads/profiles
- Explored candidate algorithms for adaptive data routing
- ASIC design launched, targeting prototype later this year

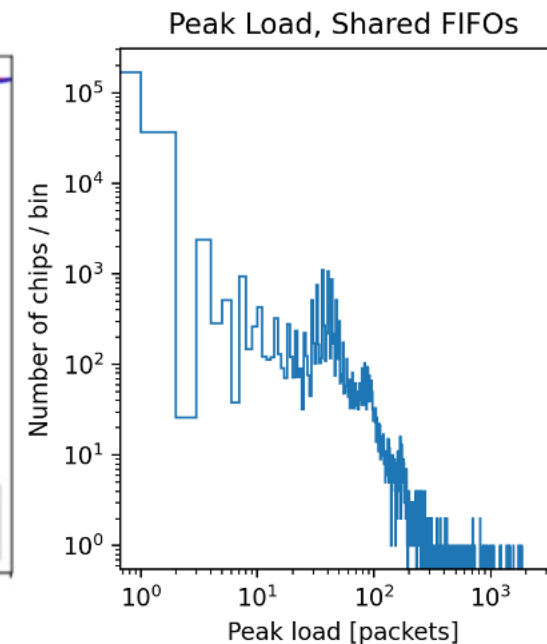
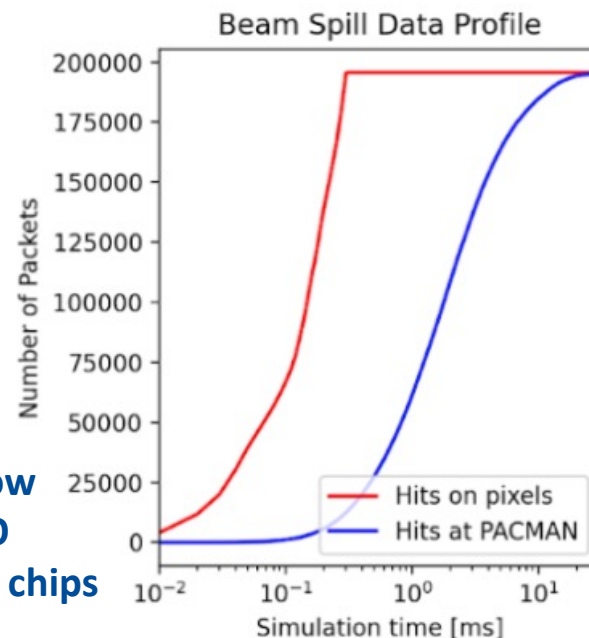
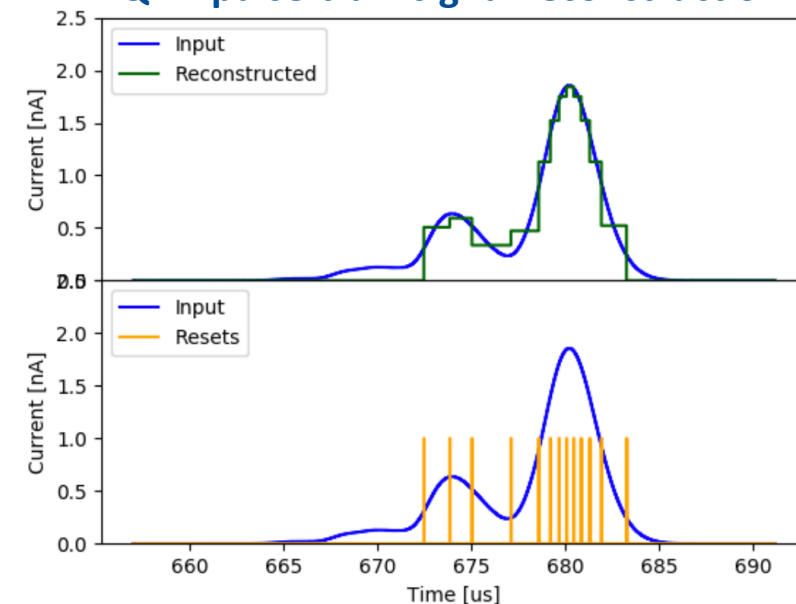
See CPAD talks by R. Carney, T. Heim, and posters by C. Ceravolo, D. Fellers!

Simulated data flow through Hydra-I/O network of LArPix chips



QPix charge-replenishment front-end concep

QPix pulse-train signal reconstruction



Simulated peak loads on LArPix memory buffers during DUNE beam pulse.

LArPix Development Team



Summary

LArPix:

- True 3D pixelated charge readout for LArTPCs
- Low-noise, low-power, cryogenic-compatible
- Self-triggering:
 - 100% live, independent of light system
 - Inherently low data volumes (no signal from inactive pixels)
 - Suitable for rare, low-energy physics searches
- Scalable anode design leverages commercial fabrication
- ~1 million channels deployed in two multi-ton prototypes
- Finalizing the design for use in the DUNE Near Detector

Related Efforts:

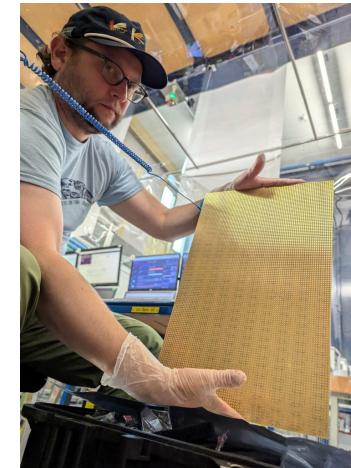
- **DUNE Phase-II:**
 - Exploring adaptation for use in future DUNE Far Detector
 - 600k-pixel prototype to operate at CERN this summer
- **Pixel LArTPC Kits:** Supporting generic detector R&D
- **LightPix:** Scalable cryo-compatible readout for SiPMs
- **NIFTY:** Adaptive data routing for improved reliability

Potential technologies for future high-granularity detectors

LArPix-v3 ASIC



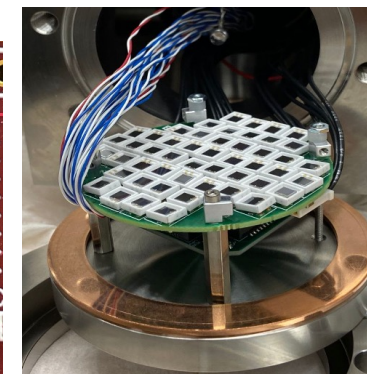
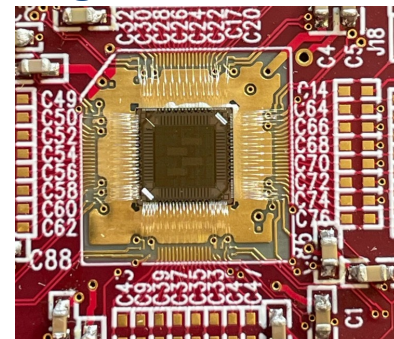
10k-pixel tile



10k-pixel TPC Kit

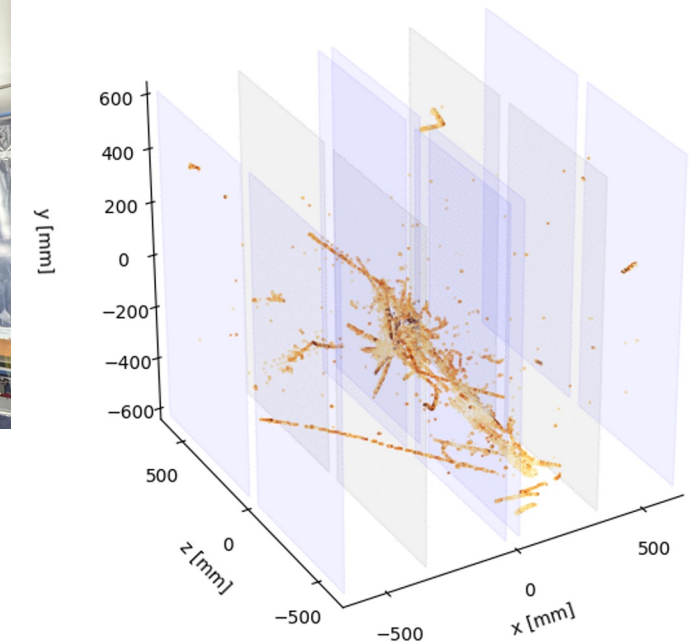


LightPix-v3 ASIC



GHe detector w/LightPix Readout

Antineutrinos in true 3D



Pixel Detector R&D for DUNE Phase II