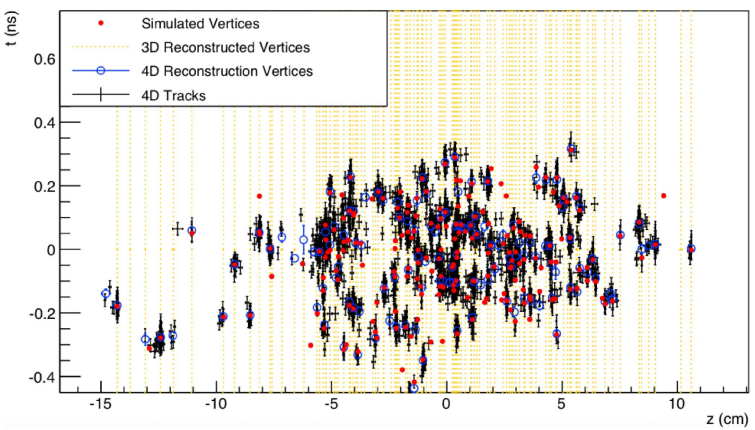
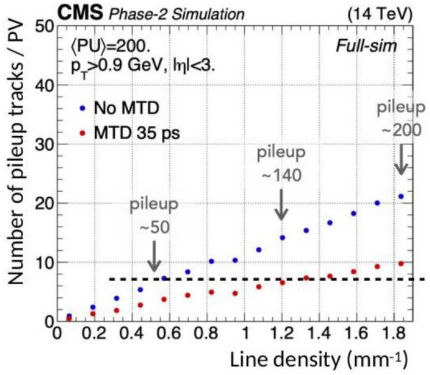
Final validation of the ETROC2 for the CMS MTD Endcap Timing Layer upgrade

Jongho Lee on behalf of ETROC Team

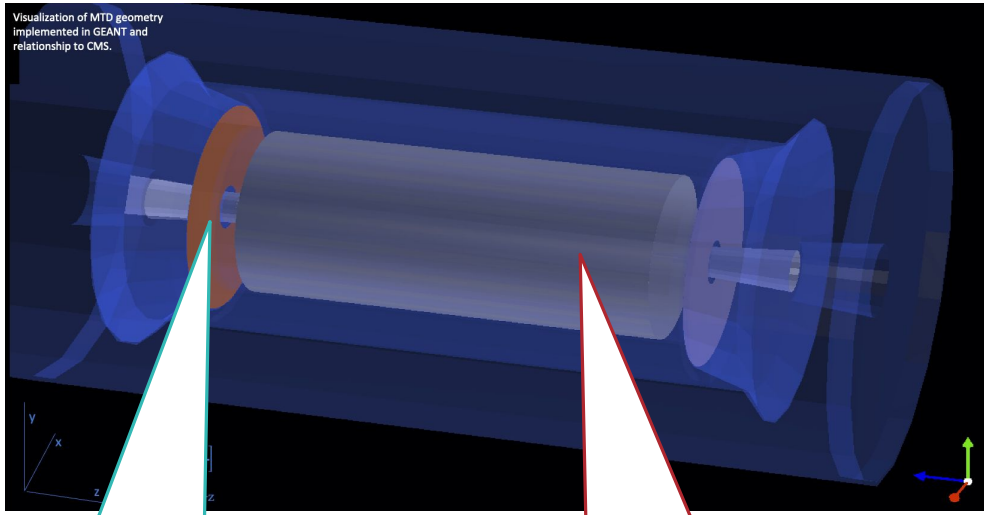
CMS Minimum Ionizing Particle Timing Detector (MTD)





The MTD will exploit timing information to reduce pile-up to current LHC level in both the forward and barrel regions.

CMS-TDR-020



Endcap Timing Layer (ETL)

Si with internal gain (LGAD):

- On the CE nose: 1.6 < $|\eta|$<3.0
- Fluence: max **2E15 n_{eq}/cm^2**
- Time resolution requirement: <50ps per hit (<35ps per track)

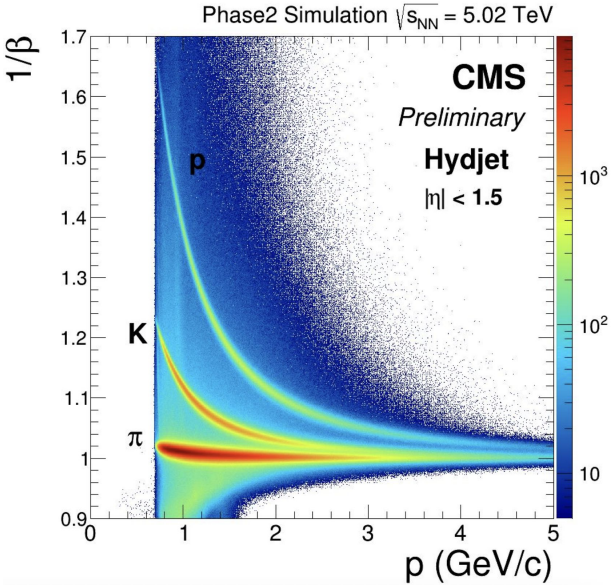
Barrel Timing Layer (BTL)

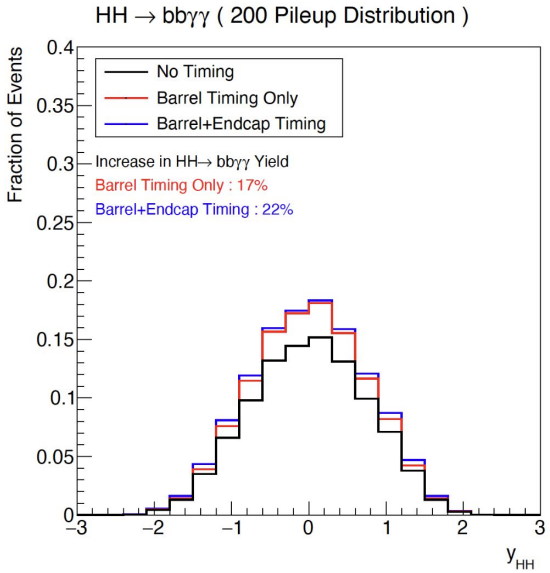
LYSO:Ce bars + SiPM readout:

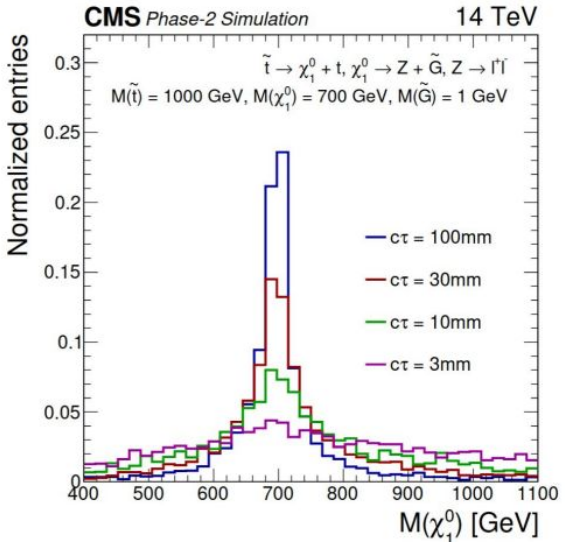
- TK/ECAL interface: $|\eta|$ < 1.45
- Fluence: max **2E14 n_{eq}/cm^2**

Physics Gain from MTD

CMS-TDR-020
CMS-DP-2022-025







Particle ID

- Infer mass from TOF, path length, and momentum

Reconstruction & Tagging

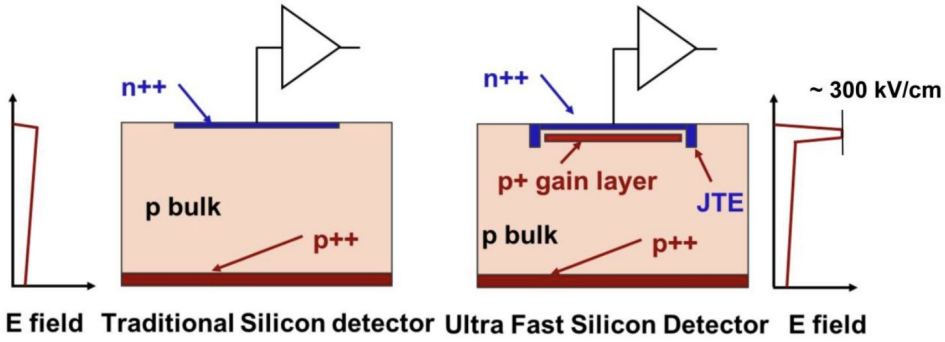
- Improve vertex reconstruction
- Better signal tagging with timing information

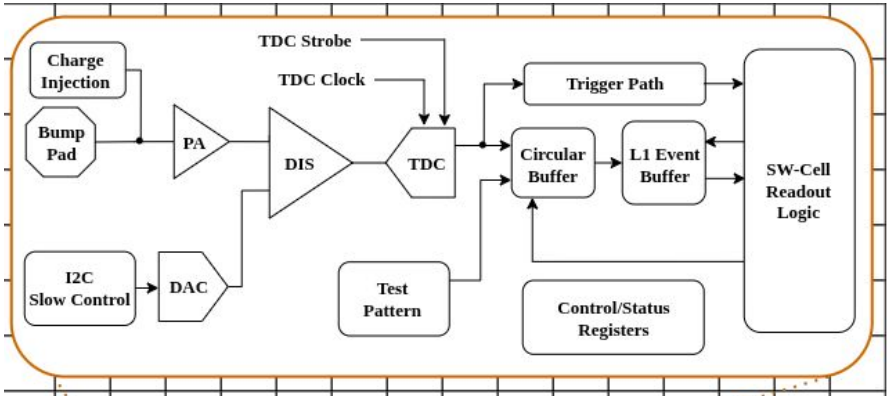
Long-Lived Particle

- Reconstruct LLP mass via kinematic constraints

Sensor and ASIC - Heart of ETL

V. Sola et al 2017 JINST 12 C02072

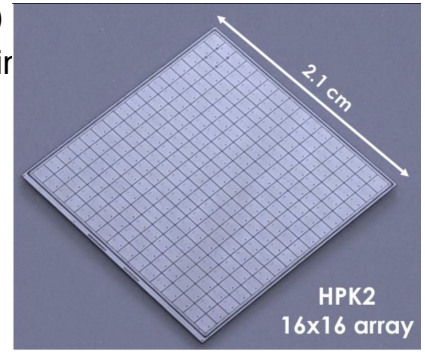


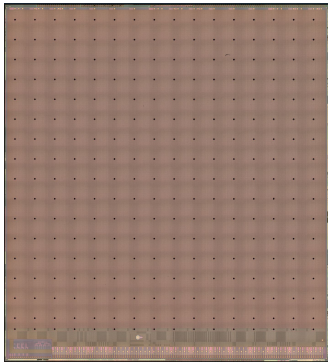


Low Gain Avalanche Diode (LGAD)

- n on p sensor with p-type gain layer
- Low gain (G~10): improve signal slope

15 year development cycle from idea to production in first-gen detectors





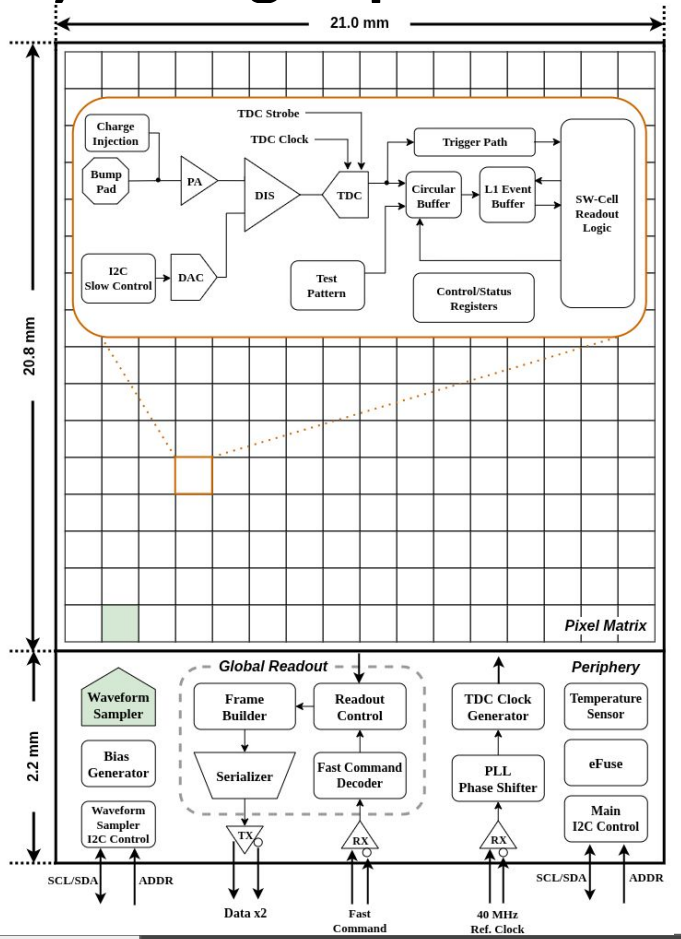
Custom ASIC design in 65nm CMOS for the ETL LGAD readout (ETROC)

- Low noise, low power
- Spec 100 MRad
- Time-Of-Arrival (TOA), Time-Over-Threshold (TOT), Calibration code (CAL)

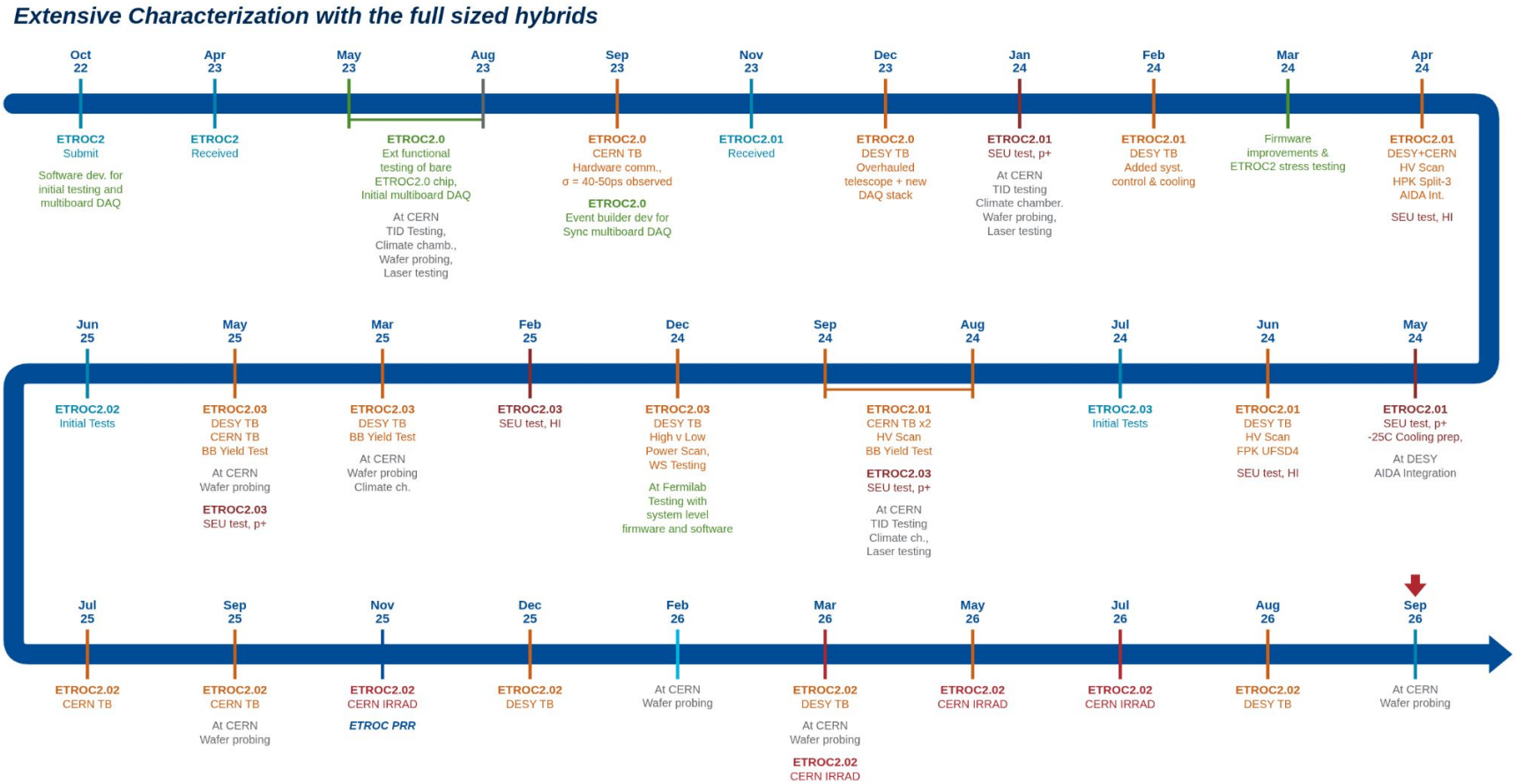
~8 year development cycle so far from the start of the ETROC project

Endcap Timing ReadOut Chip (ETROC) - Design Spec

- **Low Noise**: 30 ps intrinsic (Landau) resolution of a 50 μm LGAD limits ASIC contribution < 40 ps
- **Low Power**: Cooling capacity limits power consumption to < 1W per chip, 4 mW per pixel, 240 mW/cm^2
- **Radiation Hardness**: Must withstand 100 MRad over the 3 ab^{-1} of HL-LHC
- Sensitive to small LGAD signals: Around 10 fC per MIP towards end of lifetime of LGADs in ETL
- Some Key Features
  - Delay line based TDC with double-strobe calibration
  - Shielded H-tree Clock Distribution
  - Identical pixel layouts
  - 2.56 GS/s Waveform Sampler



History of ETROC2 Validation - Timeline



ETROC2 Validation Campaign - What We Tested

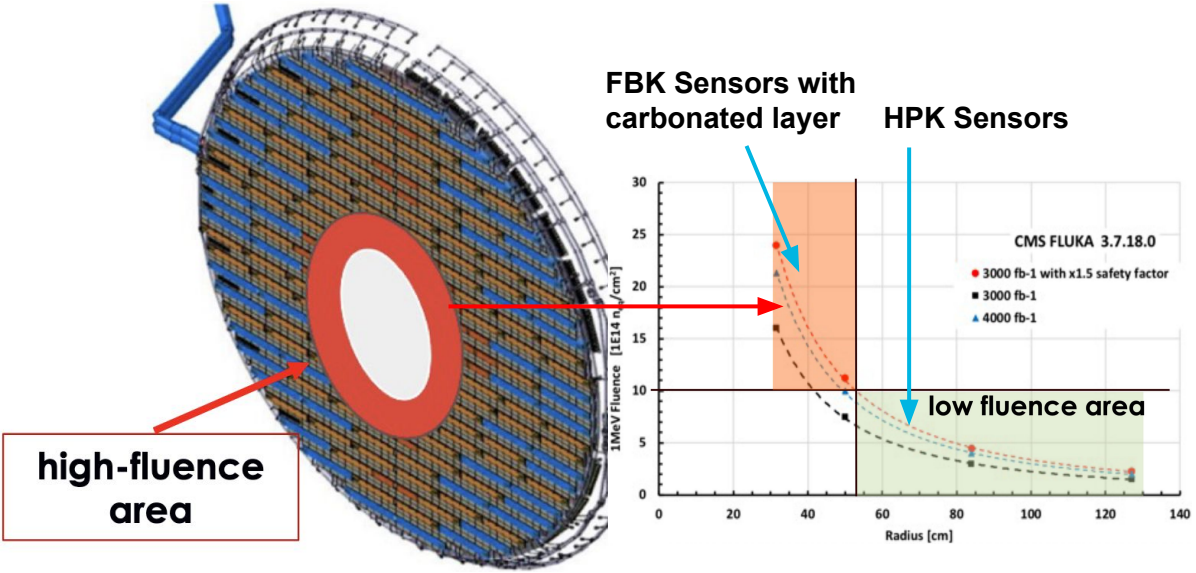
From *2023 Apr* to *2026 Sep*

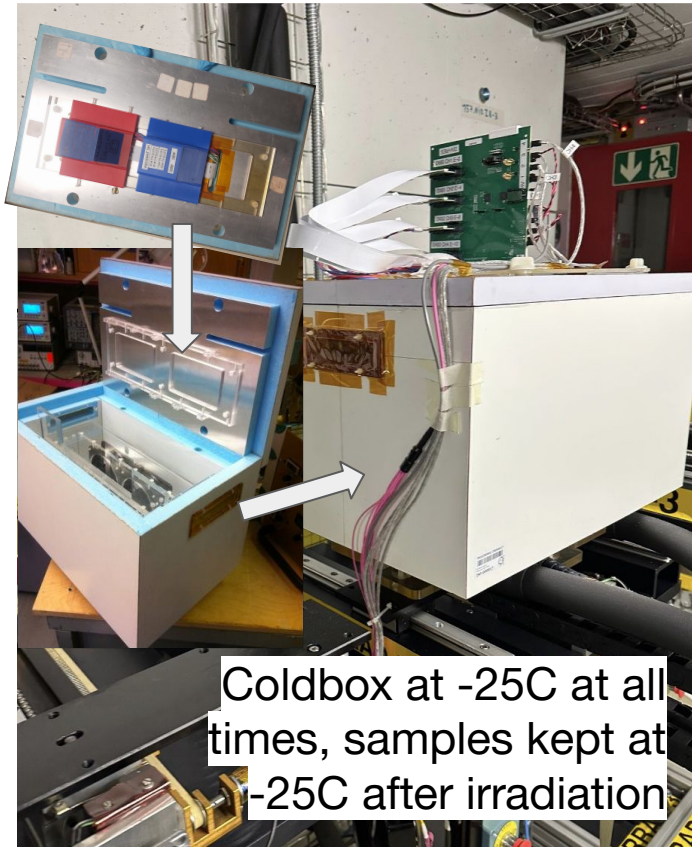
- Intensive test campaign to verify the performance of ETROC2 chips and hybrids bump-bonded with LGAD
- **16 Test beams** at CERN/DESY
  - Time resolution vs. HV, temperature, angle
- **3 irradiation testings** at cern IRRAD for etroc/sensor hybrids
  - Time resolution vs. Irradiation
- **6 SEU testings** with proton beam at Northwestern Medicine Proton Center & Heavy Ion beam at UC Louvain
  - Radiation protection & recovery
- TID testing with X ray at CERN
- Wafer probe testing

Focus this year: Irradiation tests, resolution vs. incidence angle, ETROC2 yields at wafer and QA/QC procedure

Irradiation Testing of LGAD/ETROC2 Hybrids

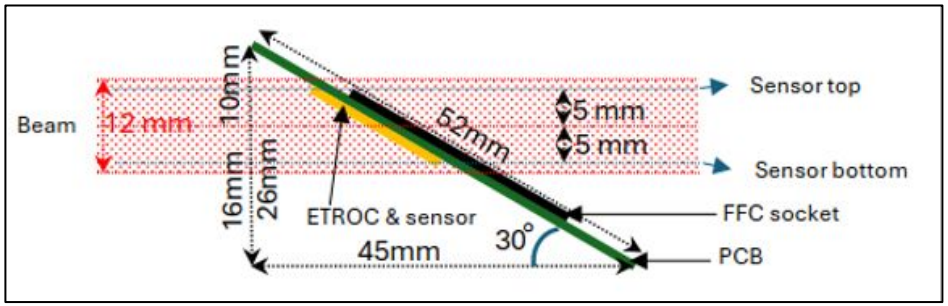
Photo by Murtaza Safdari





- LGAD/ETROC2 hybrids needs to withstand 2 x 10^{15} neq/cm^2 in the innermost region over 3 ab^{-1}, still deliver 8-10 fC for readout at the end of life
- FBK LGADs incorporate a carbonated layer for high-fluence tolerance, unlike HPK LGADs

Testing Setup at CERN IRRAD



- Telescope designed to have an angle that hybrids are fully covered with the beam
- Two different types of hybrids are installed together
  - HPK & FBK-LF Telescope
  - Allowed comparison of the two sensors in the same conditions at the same fluence
- These are final ETL vendors for LGADs



CERN IRRAD Beam Profile: Challenge and Solution

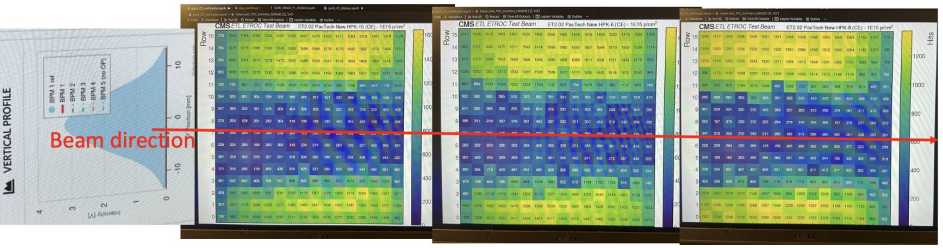
Lesson learned from first IRRAD test in Oct 2025

T1 (4 ETROC2.02/HPKs) telescope occupancy after 1E15/cm^2 proton fluence

The irradiation is rather non-uniform,

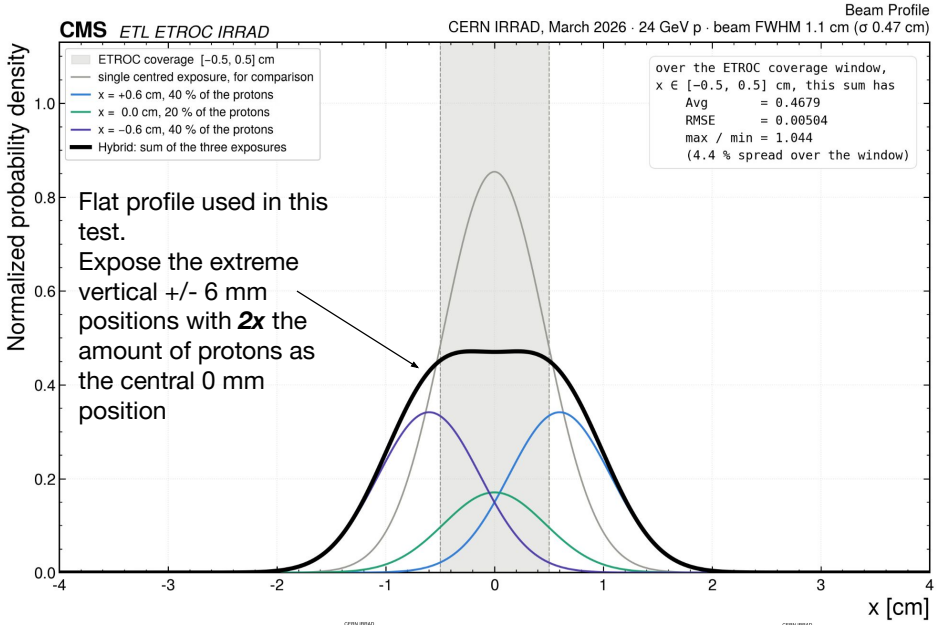
We cannot bias the more irradiated middle section with high enough HV without causing the top/bottom sections into breakdown.

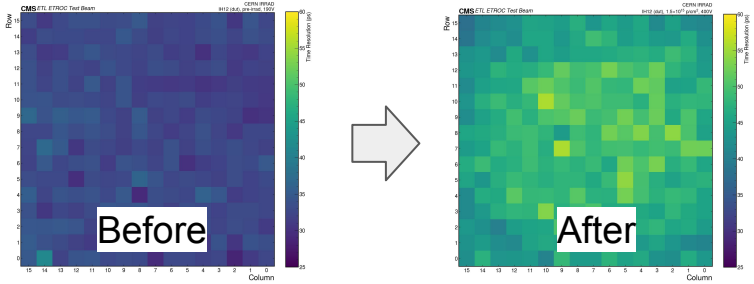
Discussing with IRRAD experts how to have more uniform irradiation vertically next time (***this is feasible***)



Hit occupancy plots

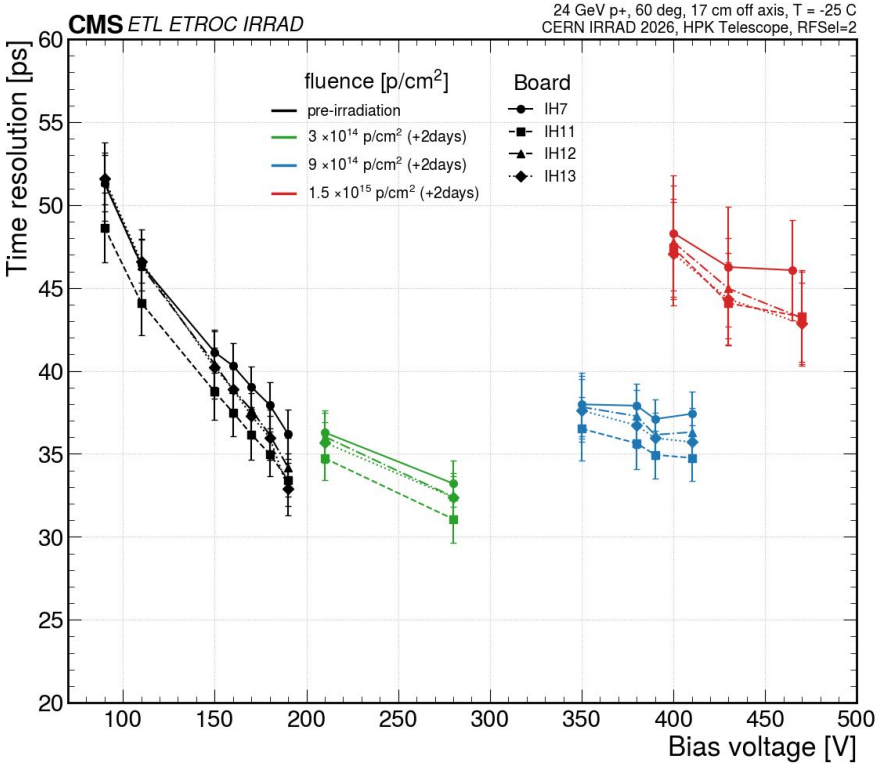
We have irradiated to 1.7E15/cm^2 proton fluence for ETROC2/HPK hybrids, and 2.82 E15/cm^2 for ETROC2/FBK-LF hybrids.
However, the non-uniform irradiation preventing us to properly study the performance due to HV limitation

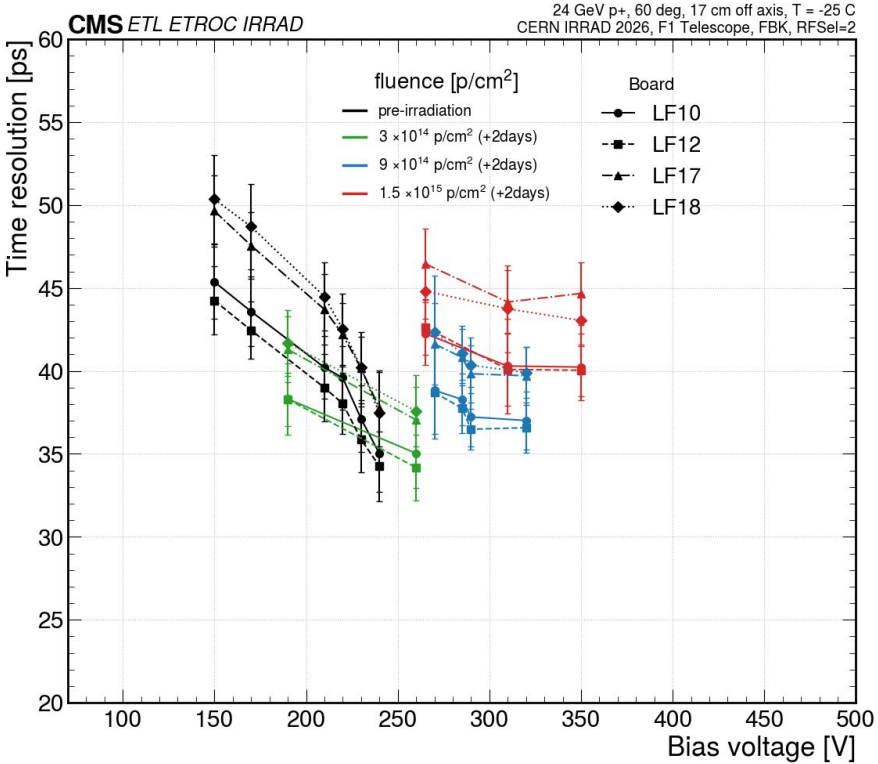




11/21/2025 ETROC2 PRR, Ted Liu 73

Time Resolution vs. Fluence After Irradiation

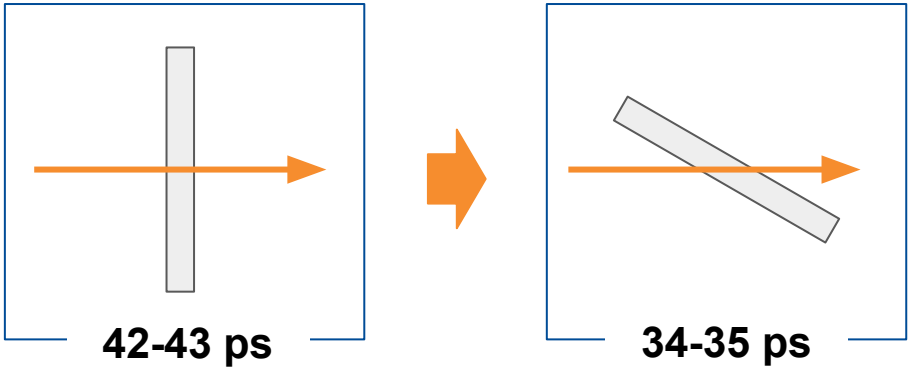




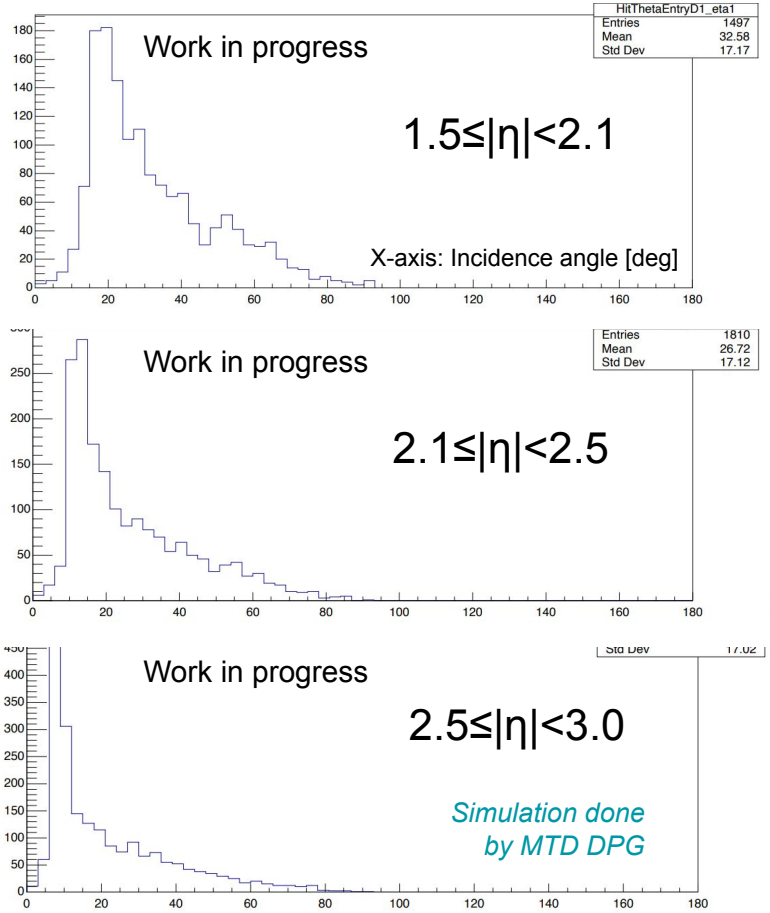
Time resolution below 50 ps at 1.5×10¹⁵ p/cm² for both HPK and FBK (60°)

(Recent testing pushed the fluence up to 2.6E15 on target, more results are coming)

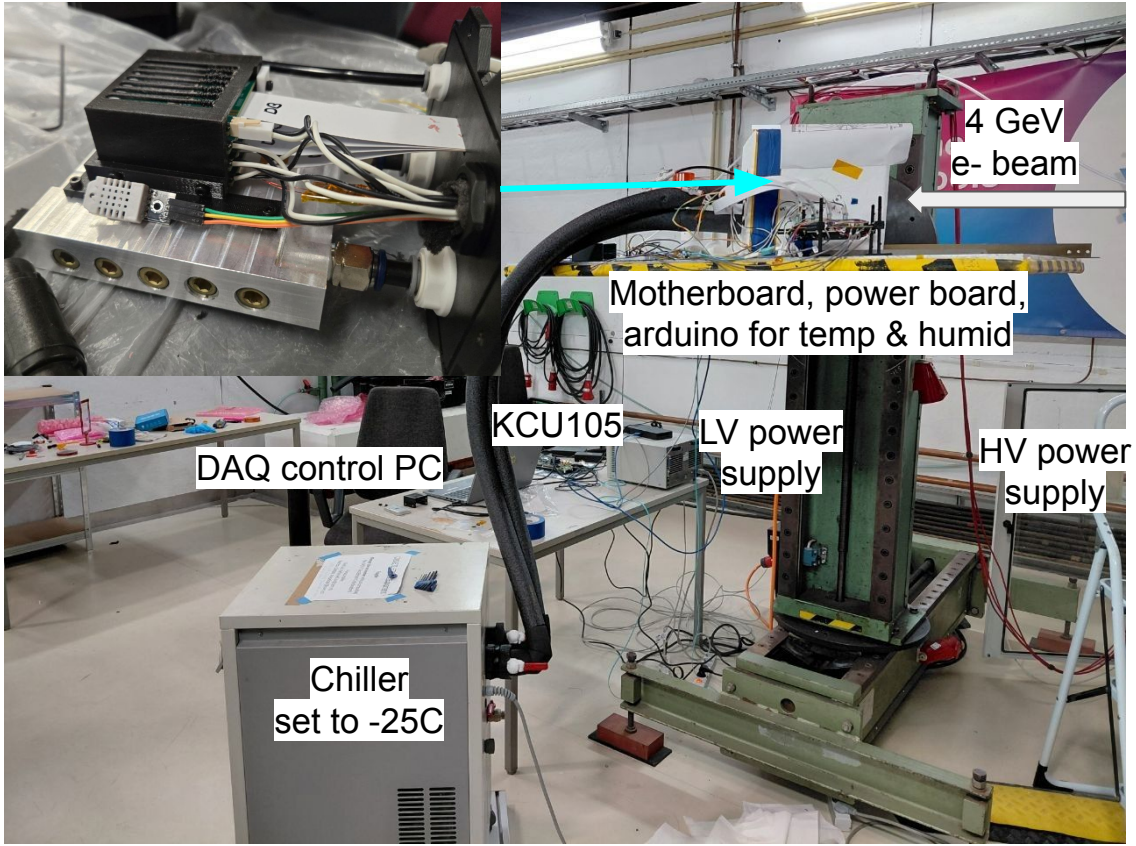
Why Test with an Angle?

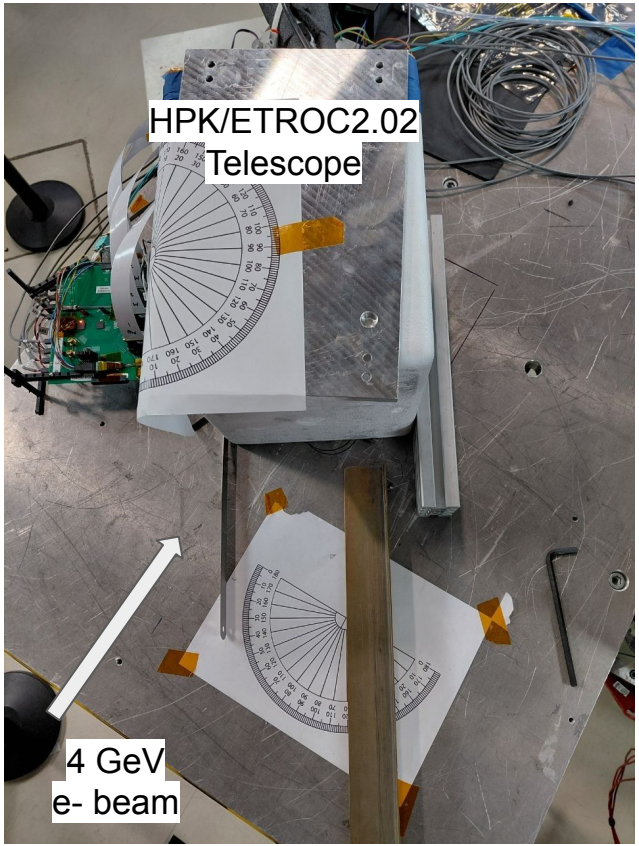


- Hybrids tilted to 60° reach 34–35 ps, against 42–43 ps when perpendicular to the beam
- Simulation: particles reach the detector at an angle
- IRRAD data are all taken at 60° incidence
- Goal: verify the angle dependence in a DESY test beam scan (0–60°)

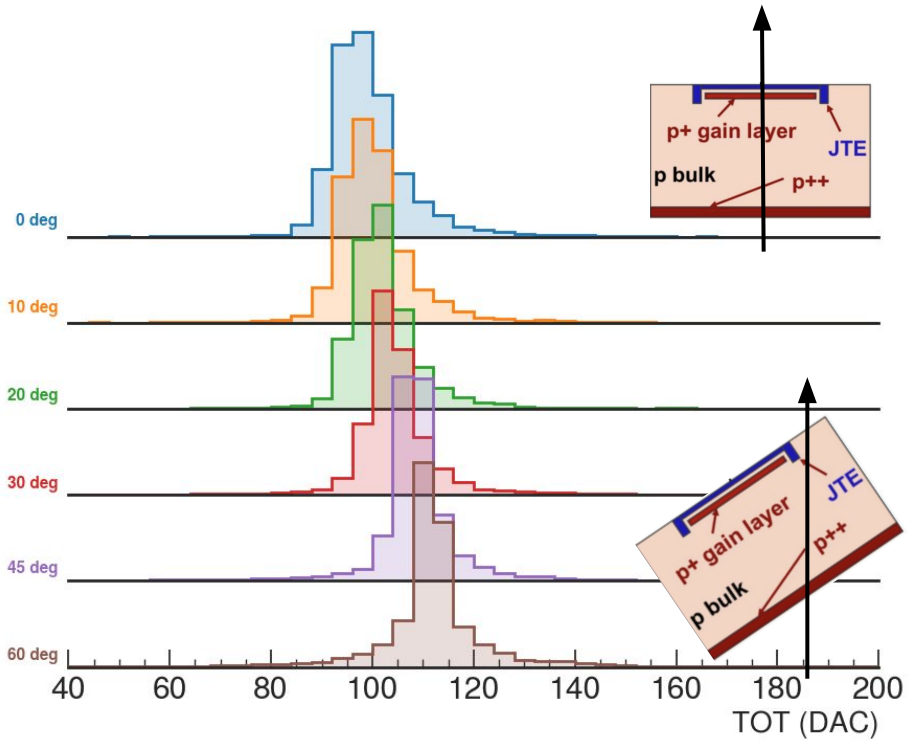


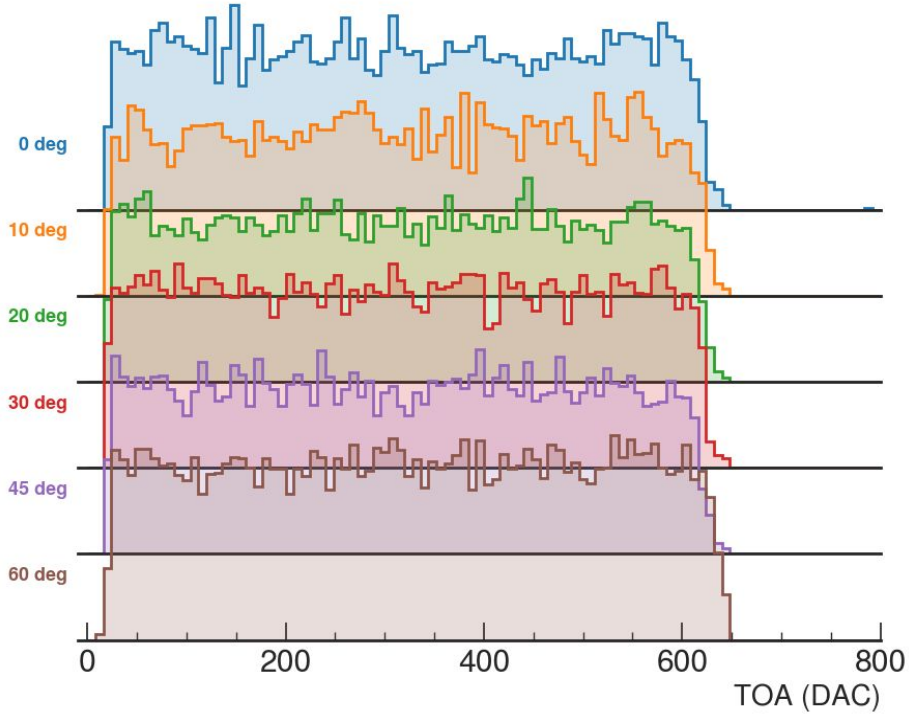
ETROC2 Test Beam Setup at DESY





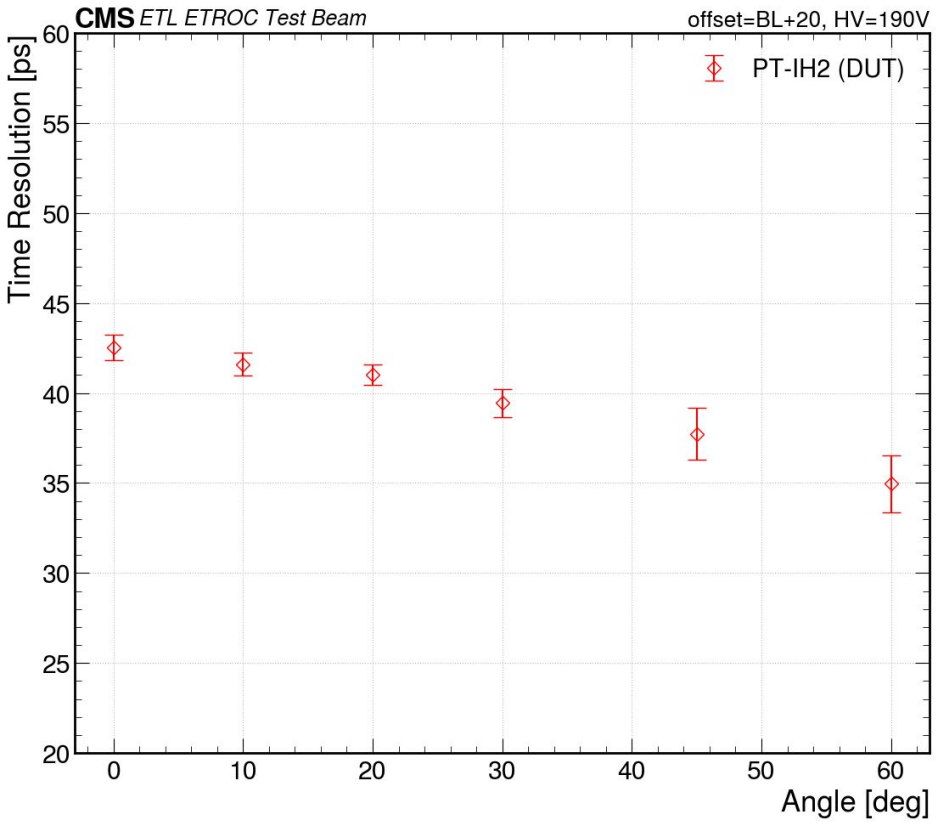
TOT and TOA vs. Incidence Angle (Single Pixel, DUT)





Larger angle → Longer path in the sensor → More charge → Larger TOT

Time Resolution vs. Incidence Angle



Board	Time resolution at 60 degree (ps)
PT-IH2 (DUT)	34.97 ± 1.58
PT-IH7 (Pre-irrad)	36.20 ± 1.49
PT-IH11 (Pre-irrad)	33.42 ± 1.58
PT-IH12 (Pre-irrad)	34.18 ± 1.76
PT-IH13 (Pre-irrad)	32.88 ± 1.58

- Time resolution improves from ~43 ps (0°) to ~35 ps (60°)
- The DUT agrees with the four pre-irradiation IRRAD hybrids at 60° (33–36 ps)

Wafer Probe: Qualifying Every ETROC2 Before Assembly



Why test at wafer level?

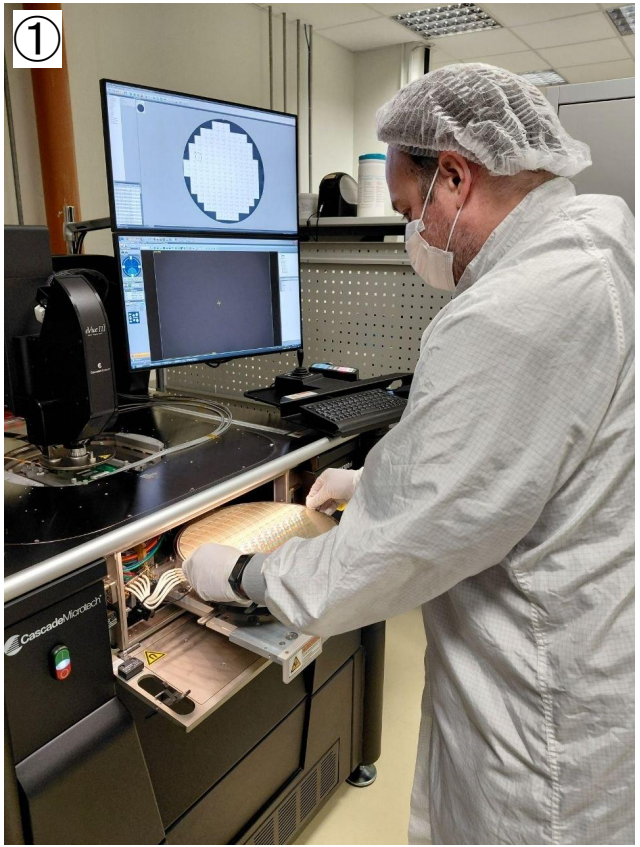
- Select only good ASICs for hybrid assembly, so bad chips are never bump-bonded
- Measure ASIC yield at the lowest level, per die and before assembly

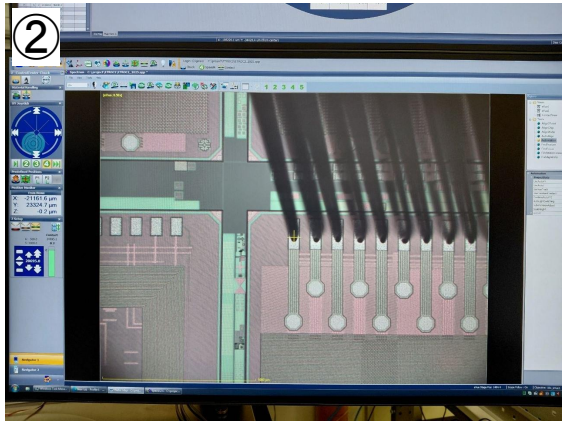
What we test on every die

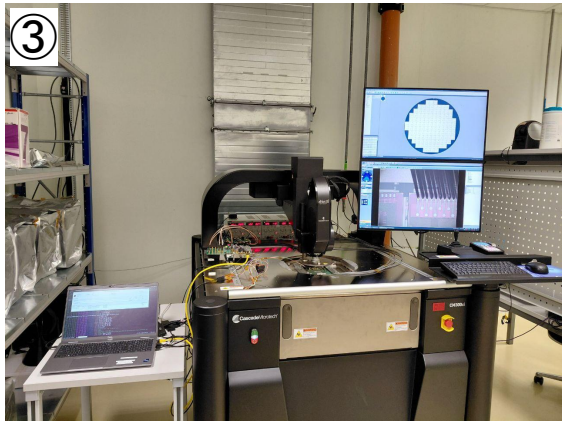
- Power: shorts and consumption in operation mode
- I2C functionality
- DAQ chain via charge injection

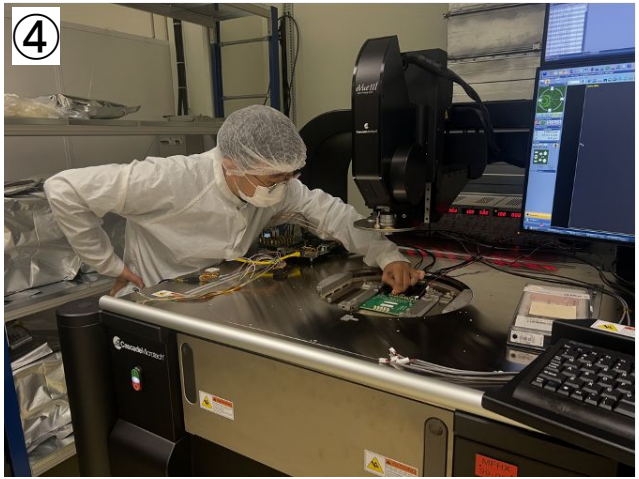
30+ pre-production wafers × 114 dies = more than 3k dies tested

Wafer Probe Station Setup



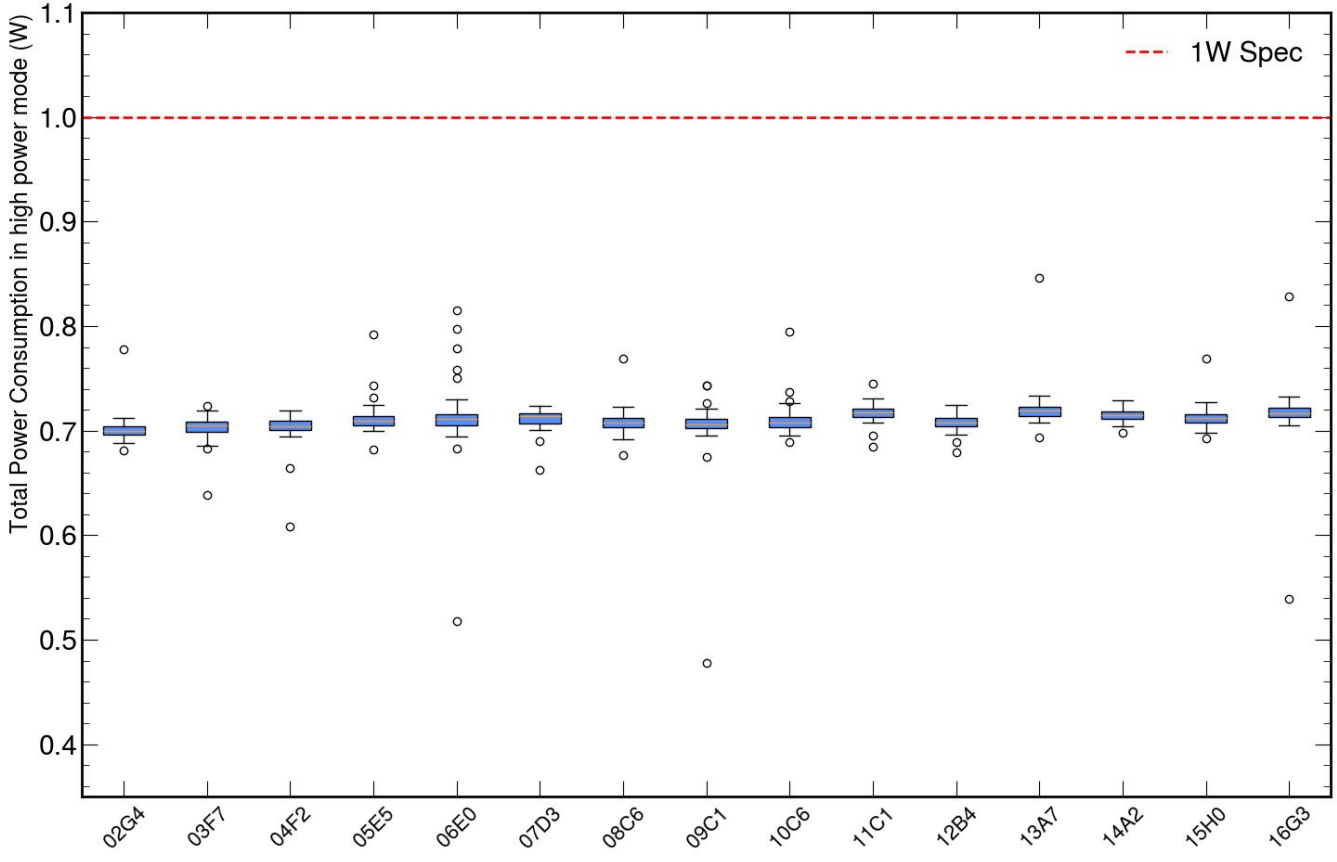






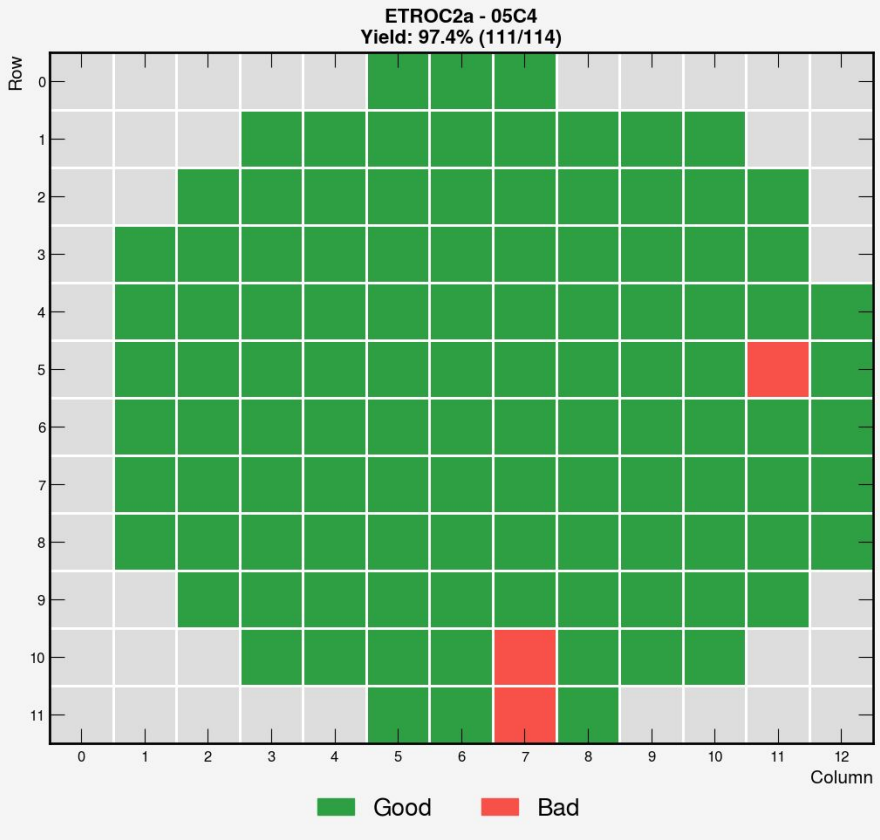
① Probe card & Wafer installed by Jerome
② Verifying probe contact and alignment
③ Wafer probe station setup
④ Cable installation by Jongho

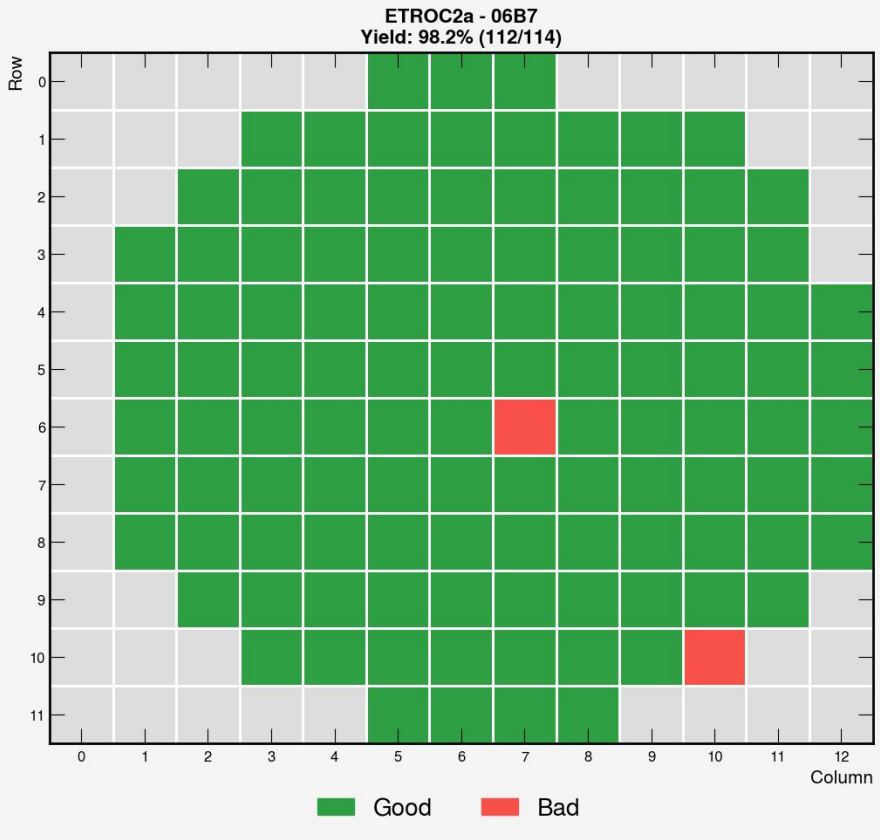
Wafer Probe Results - Power Consumption



- ETROC power consumption stays below 1 W when running in operation mode
- Operation mode refers to the preamplifier highest-current setting

Wafer Probe Results - Yield Examples





Summary

- ETROC2 is the first full-size, full-functionality ASIC for the ETL
  - With minor metal-level fixes it is the final design, with wafers on hold at TSMC
- Hybrid validation vs. fluence and incidence angle:
  - Time resolution is below 50 ps up to 1.5×10^{15} peq/cm² at 60° incidence
  - 35 ps at 60° against a 30 ps from the LGAD alone, so ETROC + system add ~18 ps (budget: <40 ps)
- Wafer-level QA/QC on more than 30 pre-production wafers (more than 3k dies)
  - Power consumption is below the 1 W spec (about 0.7 W in operation mode)
  - Yield is more than 96% across the wafers
- Production of ETROC will start soon

Acknowledgments

- This work was produced by FermiForward Discovery Group, LLC under Contract No. 89243024CSC000002 with the U.S. Department of Energy, Office of Science, Office of High Energy Physics. Publisher acknowledges the U.S. Government license to provide public access under the DOE Public Access Plan
- The research leading to these results has received funding from the European Union's Horizon Europe research and innovation programme under grant agreement no. 101057511
- The measurements leading to these results have been performed at the Test Beam Facility at DESY Hamburg (Germany), a member of the Helmholtz Association (HGF)

Backup

HL-LHC - CMS Phase 2 Upgrade

Image
F. Hartmann, UC Plenary at CMS week

L1-Trigger
- Tracks in L1-Trigger at 40 MHz
- Particle Flow selection
- 750 kHz L1 output
- 40 MHz data scouting

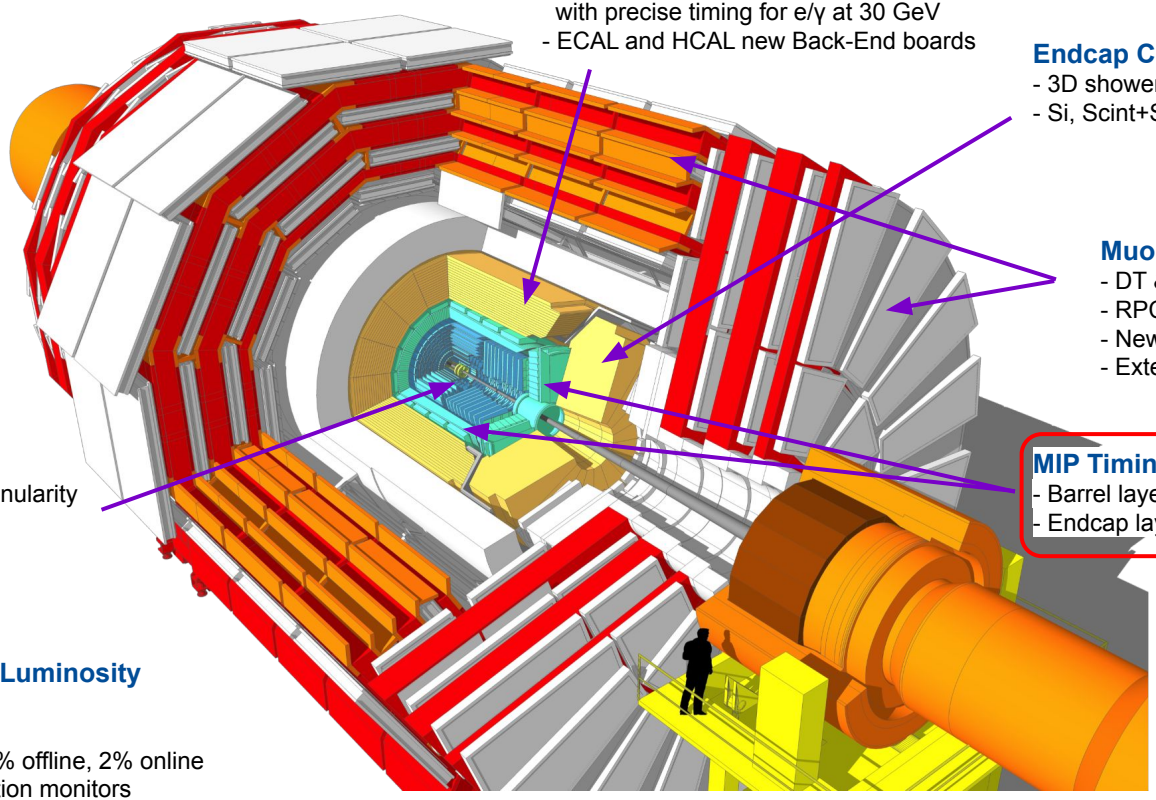
DAQ & High-Level Trigger
- Full optical readout
- Heterogenous architecture
- 60 TB/s event network
- 7.5 kHz HLT output

Tracker
- Si-Strip and Pixels increased granularity
- Design for tracking in L1-Trigger
- Extended coverage to $\eta \simeq 3.8$

Beam Radiation Instr. and Luminosity
- Beam abort & timing
- Beam-induced background
- Bunch-by-bunch luminosity: 1% offline, 2% online
- Neutron and mixed-field radiation monitors

Barrel Calorimeters
- ECAL single crystal granularity at L1 trigger with precise timing for e/γ at 30 GeV
- ECAL and HCAL new Back-End boards

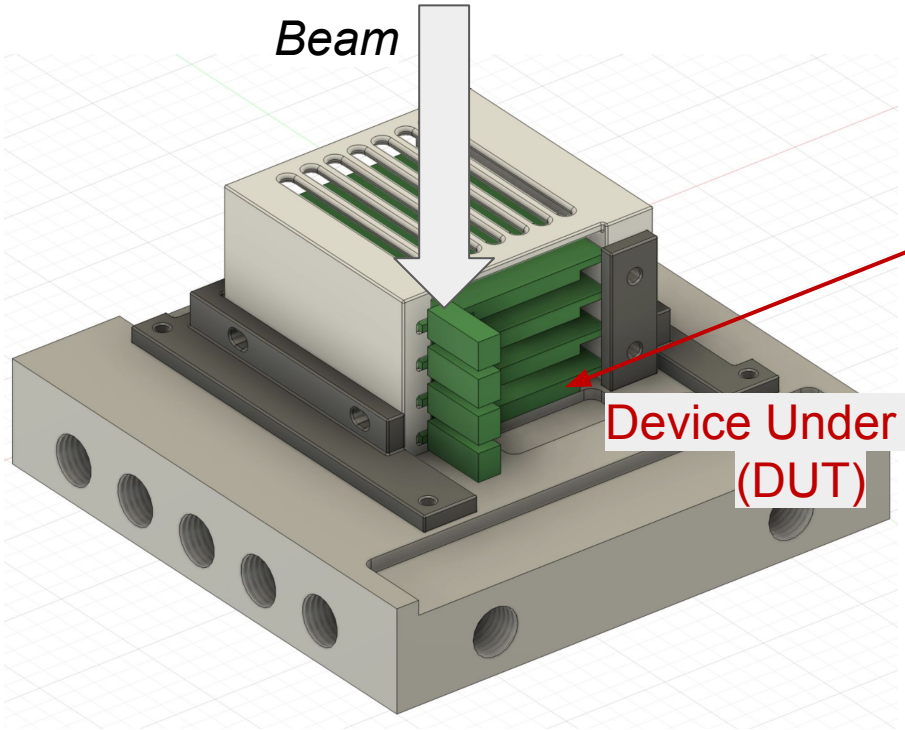
Endcap Calorimeter (HGCAL)
- 3D showers and precise timing
- Si, Scint+SiPM in Pb/W-SS

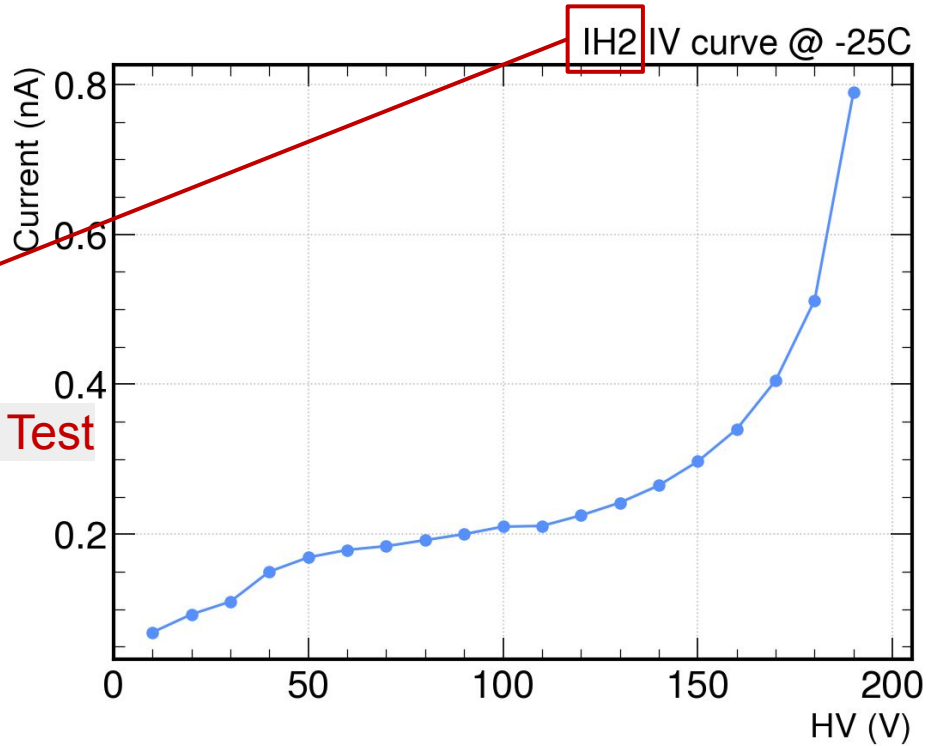


Muon systems
- DT & CSC new FE/BE readout
- RPC back-end electronics
- New GEM/RPC $1.6 < \eta < 2.4$
- Extended coverage to $\eta \simeq 3$

MIP Timing Detector
- Barrel layer: Crystals + SiPMs
- Endcap layer: Low Gain Avalanche Diodes

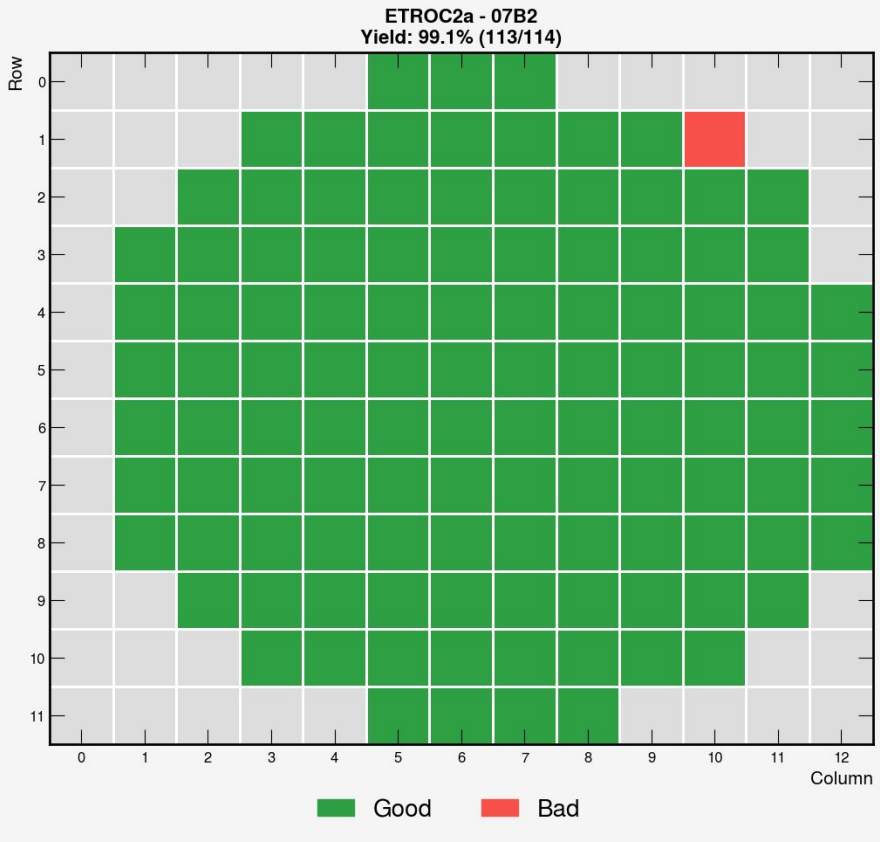
Test Beam Preparation

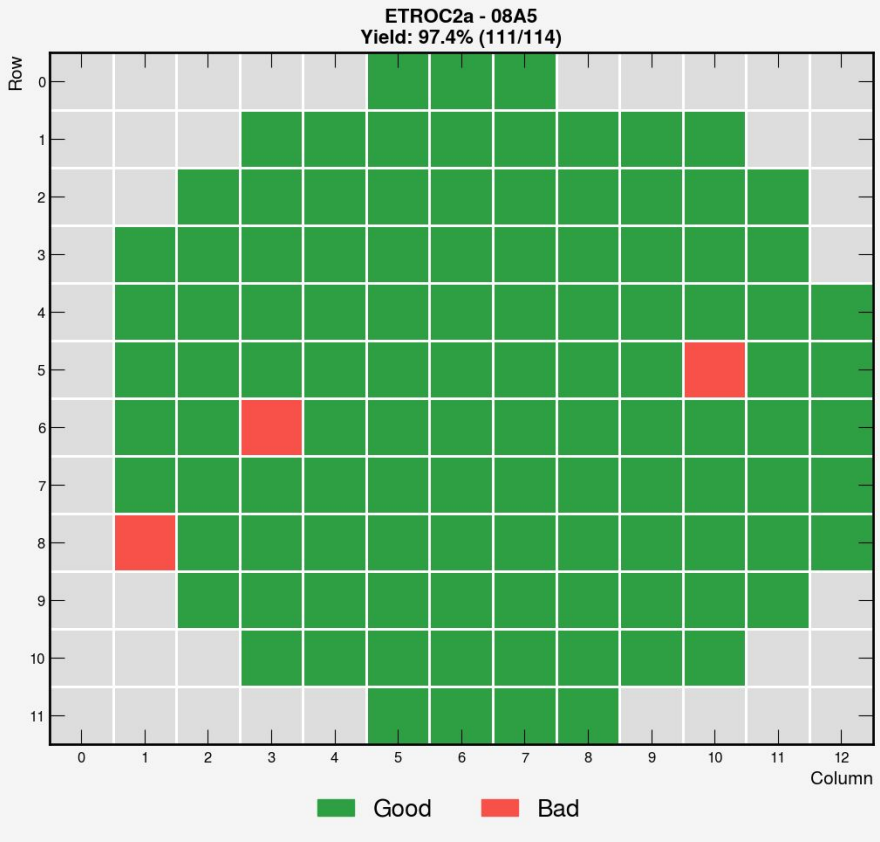




Telescope of HPK/ETROC2.02 hybrids

Wafer maps


ETROC2a - 07B2
Yield: 99.1% (113/114)
Row
Column
Good
Bad


ETROC2a - 08A5
Yield: 97.4% (111/114)
Row
Column
Good
Bad