

The Analog Photon Processor ASIC: Design Updates

Coordinating Panel for Advanced Detectors Workshop

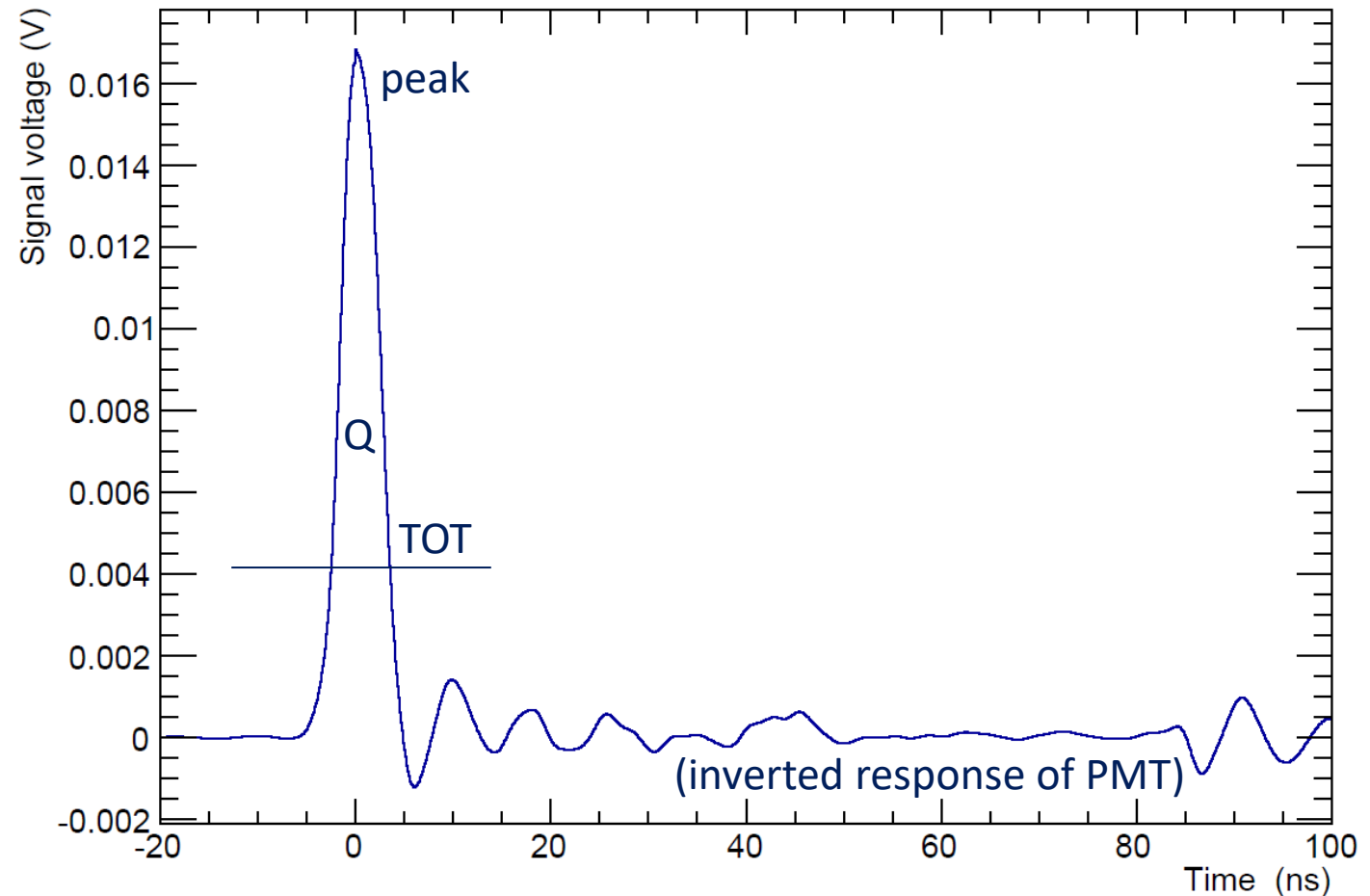
Adrian Nikolica, for the UPenn Instrumentation Group

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University of Washington, 22 October 2026

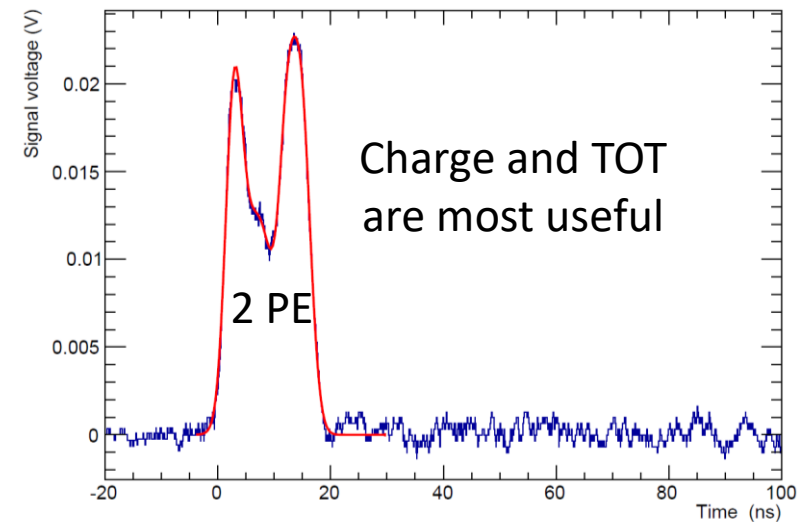
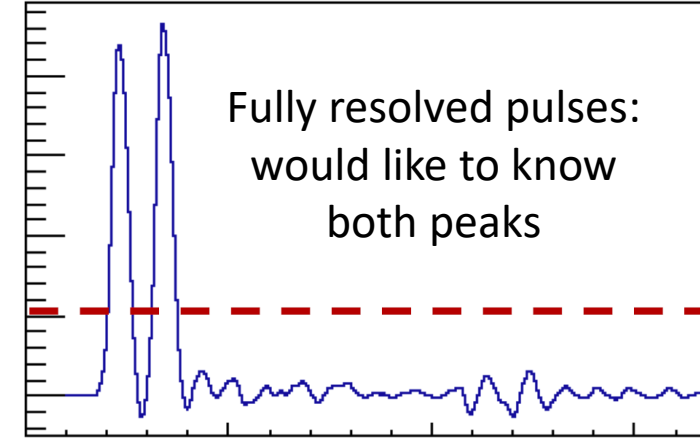
APP concept

- Motivation:
 - Cherenkov, scintillation, or hybrid neutrino detectors
 - Fast, large area photomultiplier tubes (PMTs)
 - Moderate rate, infrequent, but important data
 - We are interested in the number of photoelectrons (PE), and their arrival times
- Can we do better than full digitization?
 - Petabytes – exabytes per year in 10^4 channel systems
 - High cost, relatively power hungry
 - Resolution and dead time limitations (for closely spaced pulses)
- Need these parameters to characterize an arbitrary PMT pulse:
 - Leading and trailing edge times – get time over threshold (TOT) from edge times
 - Peak amplitude
 - Peak time
 - Total charge (Q)

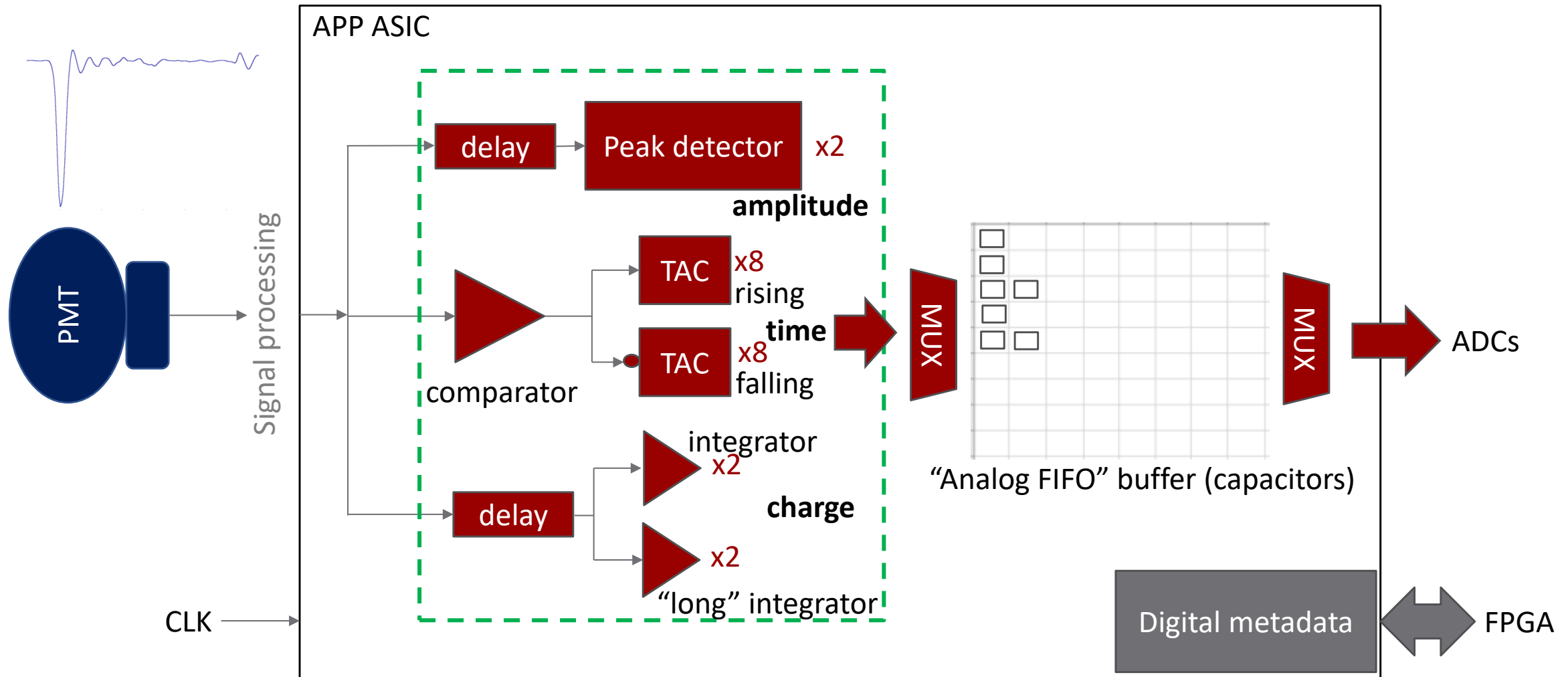


PE measurement and counting

- How can we determine #PEs ?
- Maximum likelihood estimation
 - Calculate 3-D probability density functions using TOT, Q, peak
 - Obtain good estimate of number of PE in a pulse for 1—8 PE
 - (PE PMT responses obey the laws of linear superposition)
- Frequency domain
 - Matched filter e.g. convolve filter response of ideal log-normal pulse with input signal
 - Sensitive to filter kernel, aliasing problems
- Many approaches work best offline
- Analog circuit blocks:
 - Time to amplitude converter (TAC)
 - Peak detector
 - Integrator
- Use an ASIC, with local analog memory, read out with low cost ADCs
 - SNO did this to some extent with TAC, charge (fixed windows), no timing information on second hit
 - Some “photon counting” ASICs exist
 - Some older work in 0.35 μ m process – not good for modern tubes with sub-ns TTS



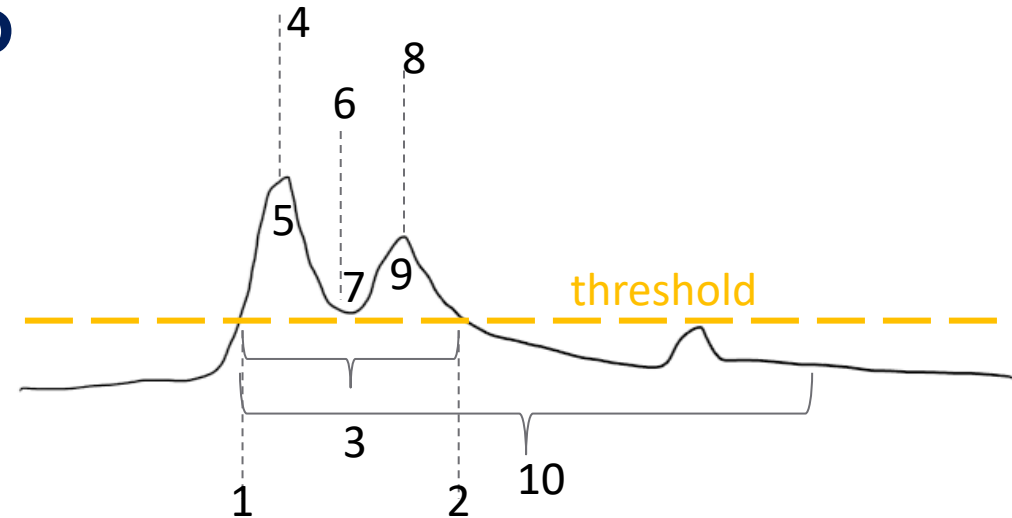
Block diagram (very simplified)



Lots of detail not shown: internal connections, digital logic, etc.

Basic requirements of APP

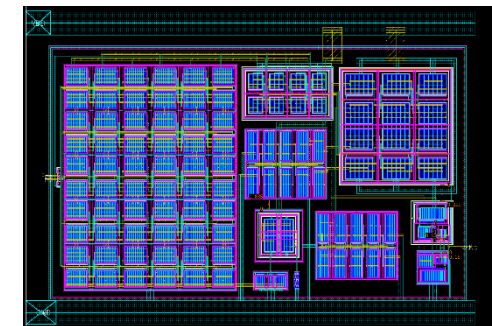
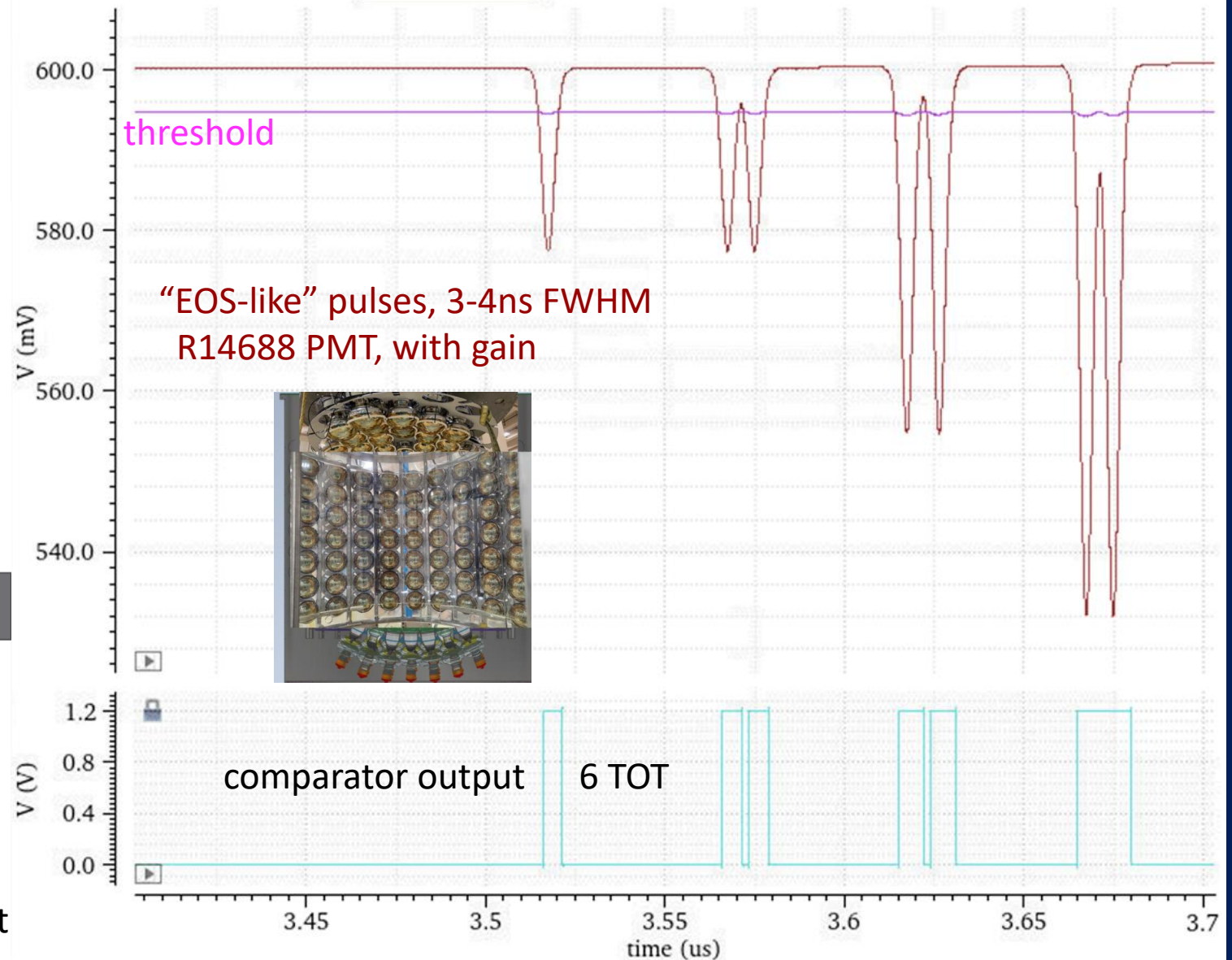
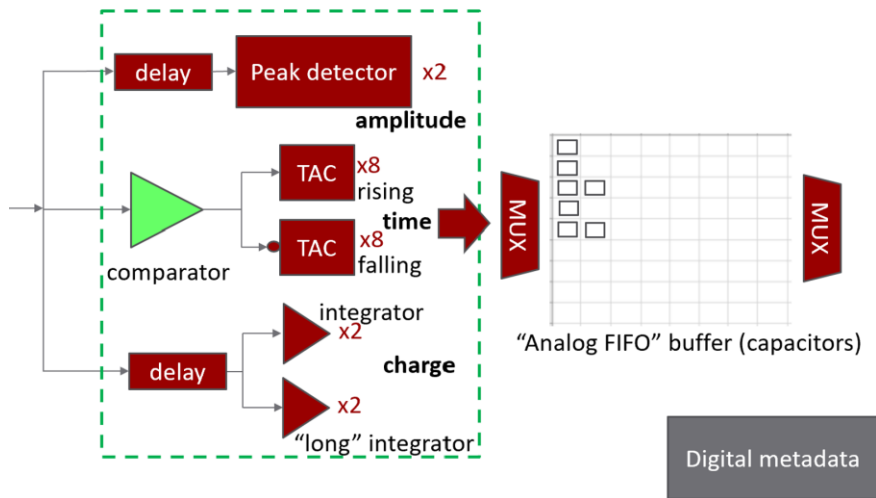
- We'd like to capture PMT pulses with:
 - FWHM $\sim 5\text{ns}$ or less, risetimes $\sim 1\text{ns}$ or less
 - Better than 100ps **timing** resolution (much better than PMT transit time spread, or TTS) on peak time and edges
 - $\sim 5\text{--}500\text{mV}$ peak **amplitude** (up to 100 PE)
- **Charge** integral (Q) – within window of a few hundreds of ns (single peak), up to μs (“long” charge)
 - Programmable window for “late” scintillation light
- We want to **re-trigger with minimal deadtime**
 - To catch closely spaced resolved PE
 - Motivates “analog FIFO”
- Key measurements at right:
 - Not every measurement needed for every application
 - Some measurements are cross-checks on others (e.g. “long charge”)
 - After a few unresolved PE, most information also in Q
- Low #ch / chip – channel density probably limited by cables in a PMT system (not true for pixelated detectors!)



1. Leading edge of TOT "event"
2. Trailing edge of TOT event
3. Integral of TOT event (charge)
4. Time of 1st peak in the event
5. Amplitude of 1st peak in the event
6. Time of 1st valley in the event
7. Amplitude of 2nd valley in the event
8. Time of 2nd peak in the event
9. Amplitude of 2nd peak in the event
10. Integral of total charge over a programmable time starting with the 1st event

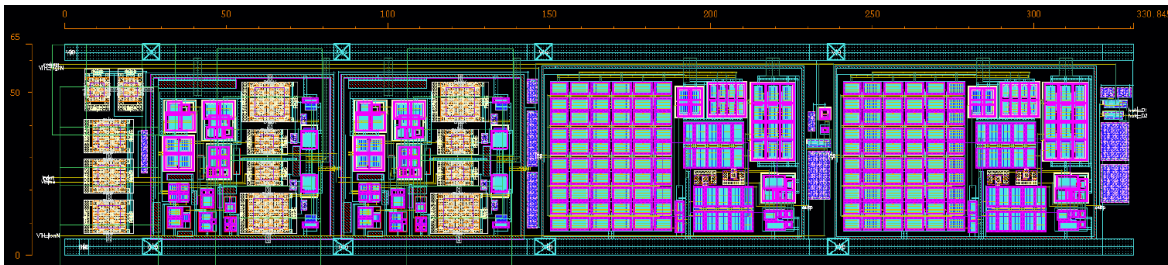
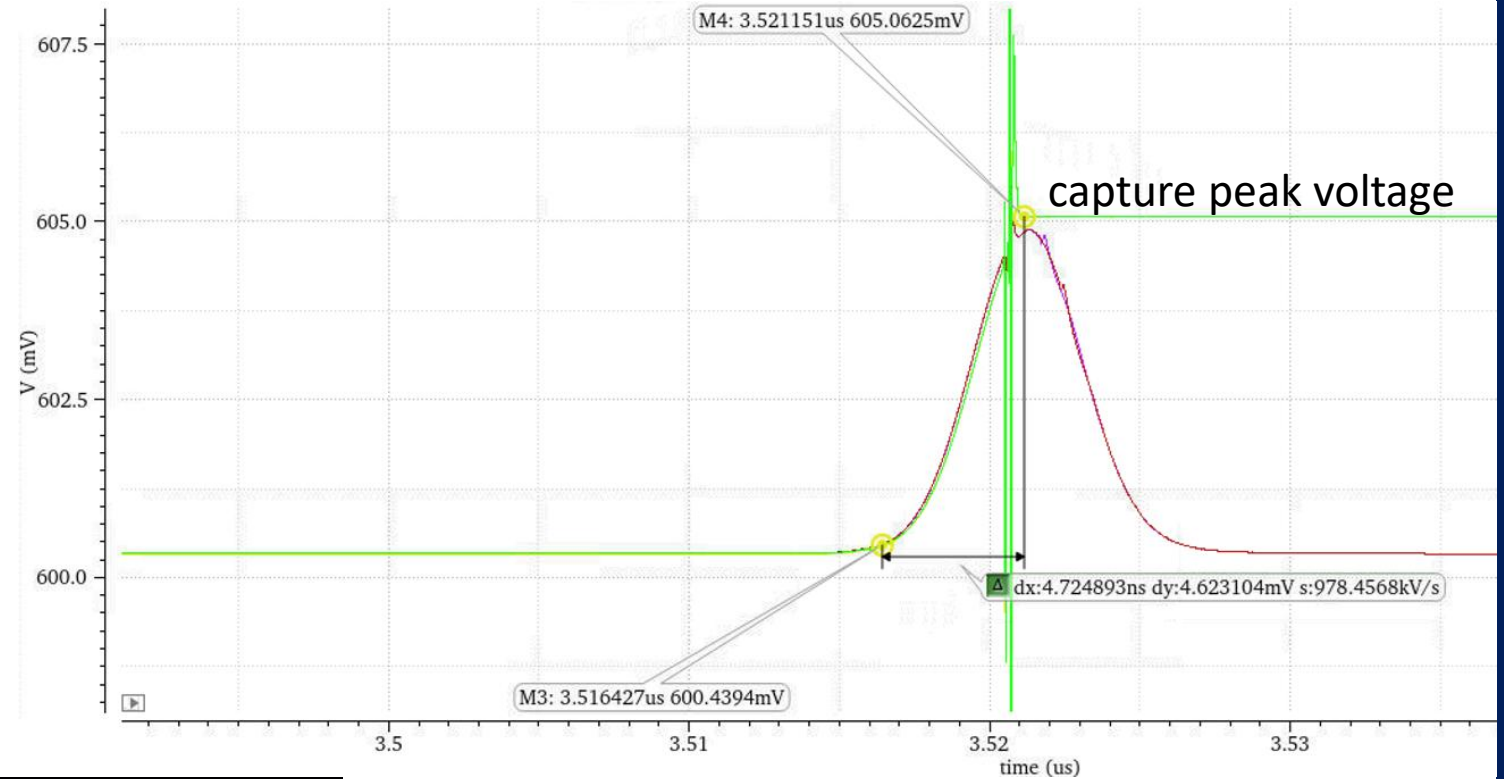
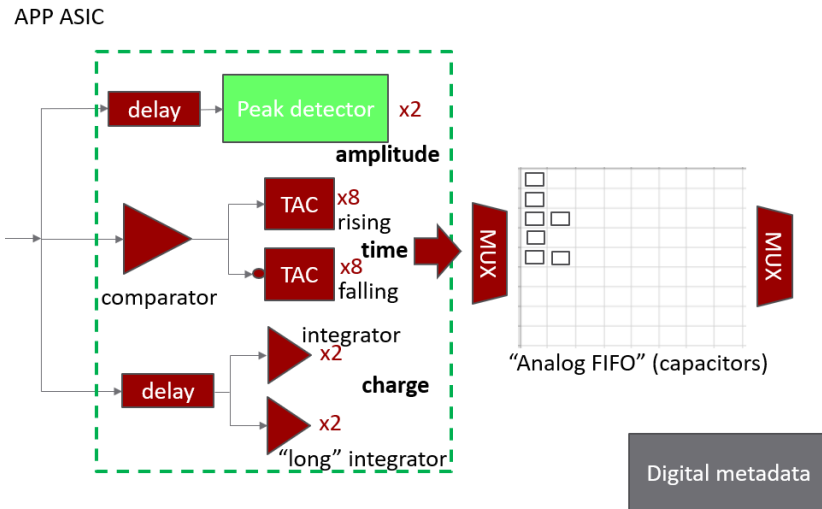
Some circuit simulations: comparator

APP ASIC



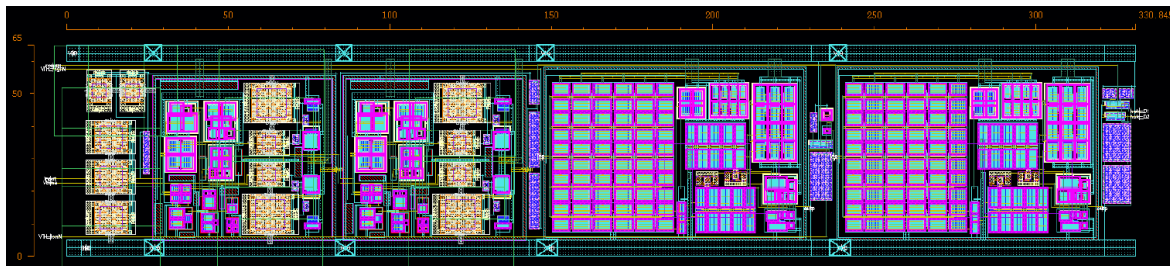
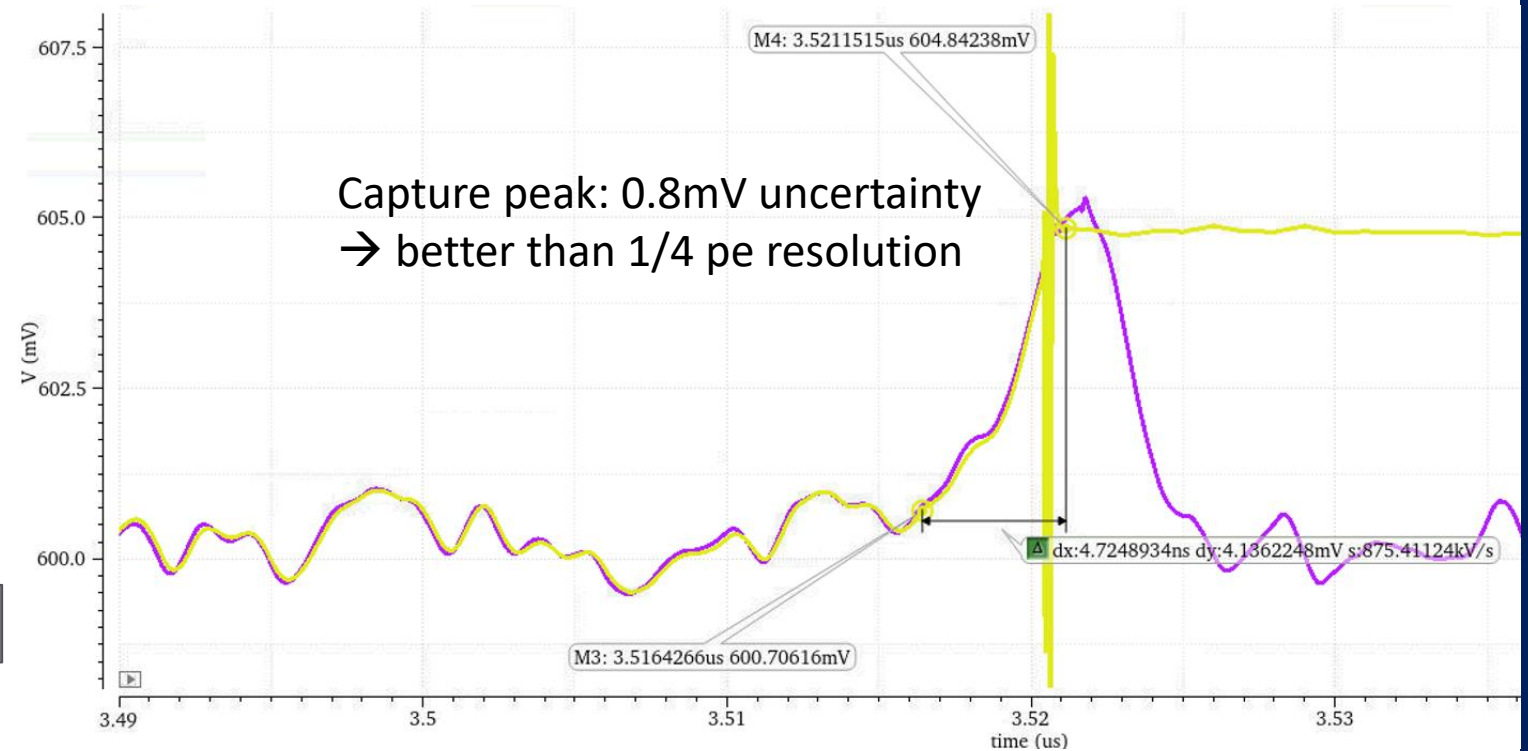
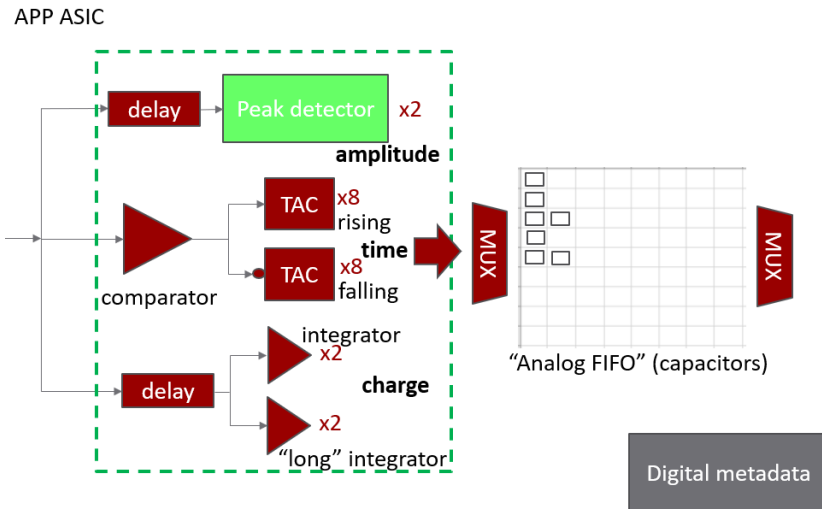
Comparator layout

Peak detector



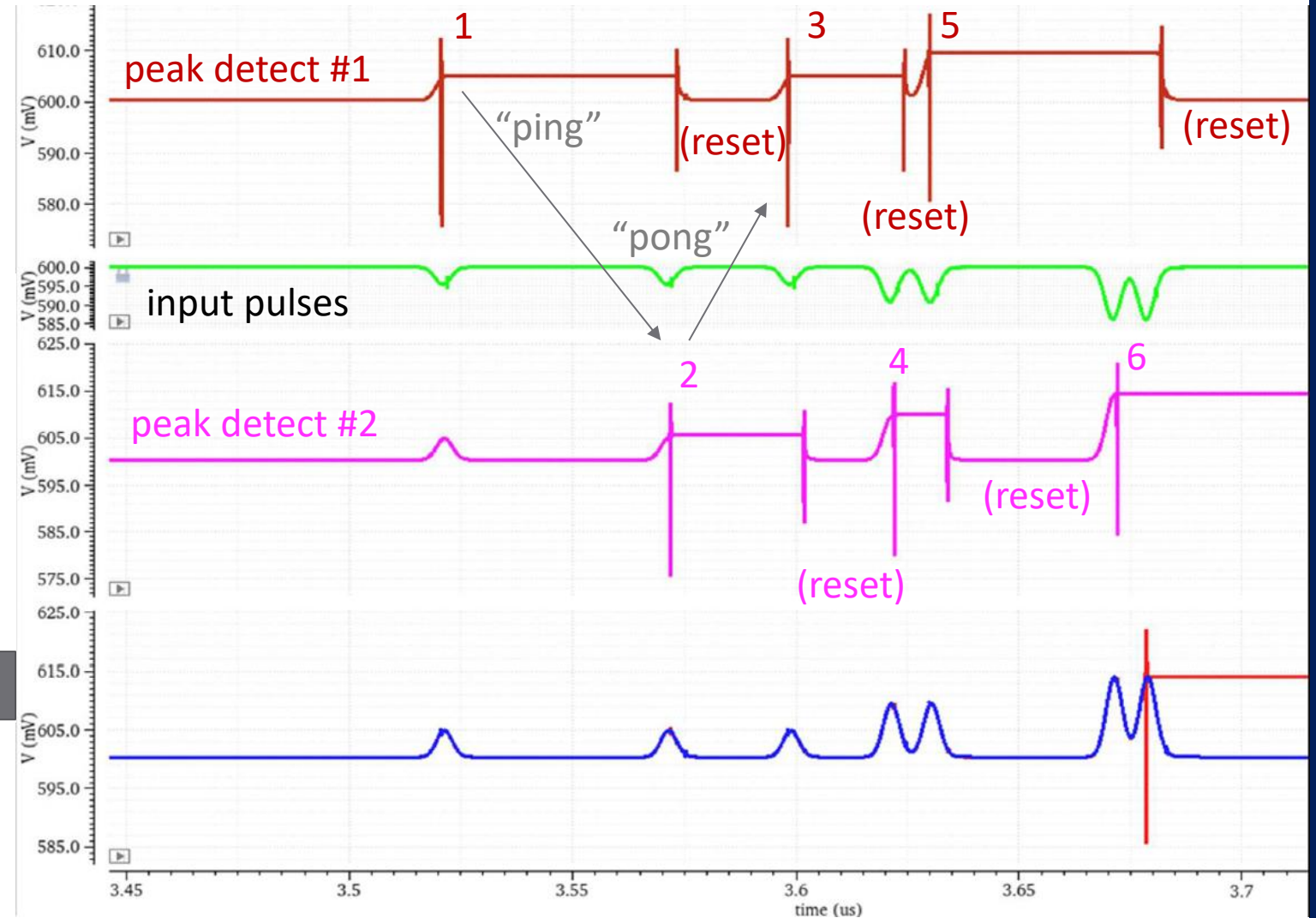
Peak detector layout

Peak detector (with intrinsic transient noise)

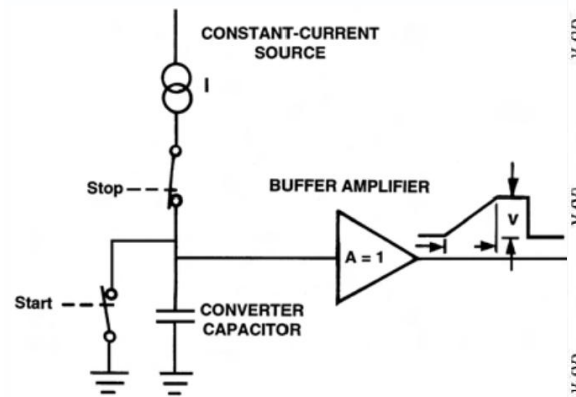


Peak detector layout

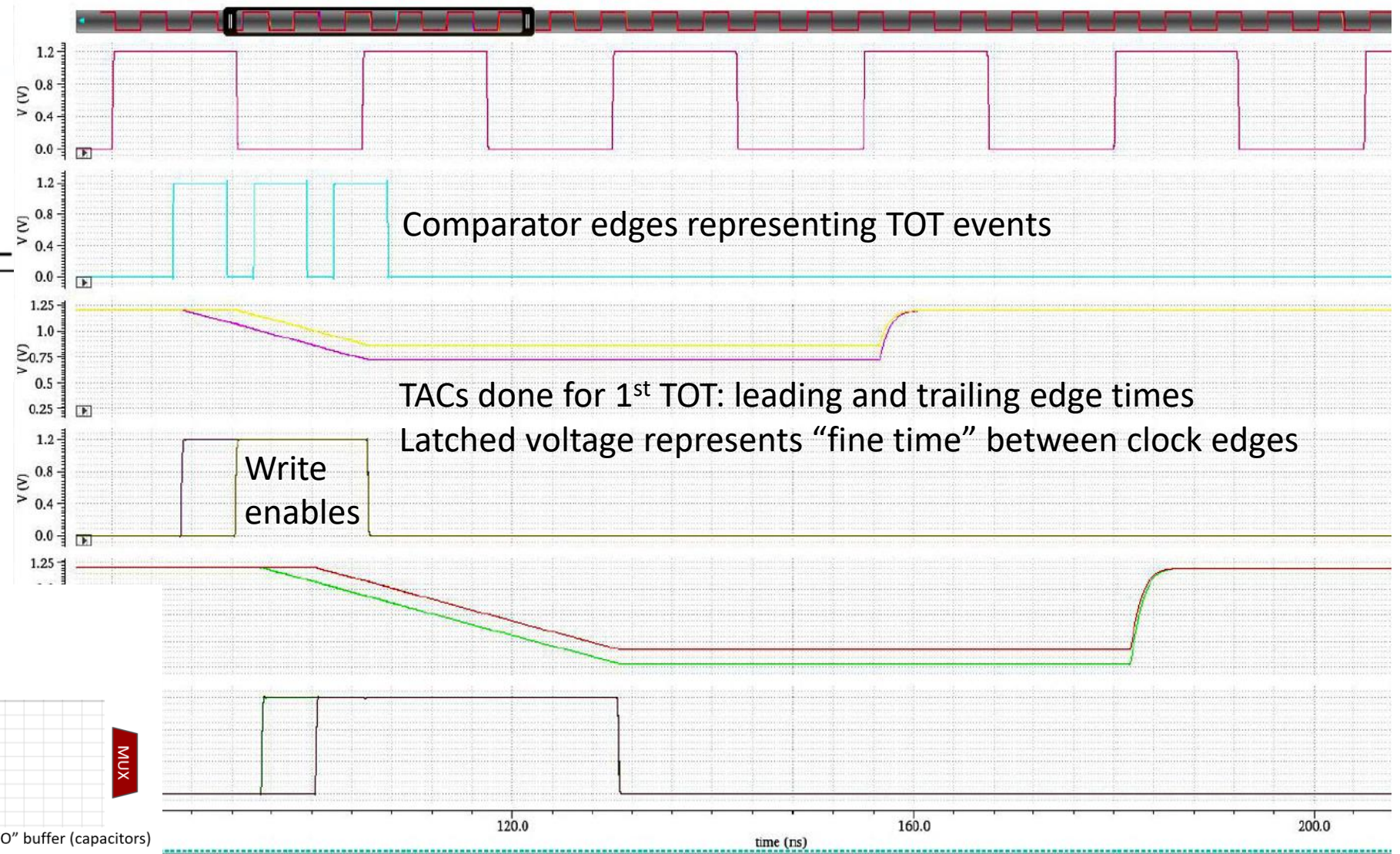
- APP ASIC



Timing measurement



Simplified TAC*

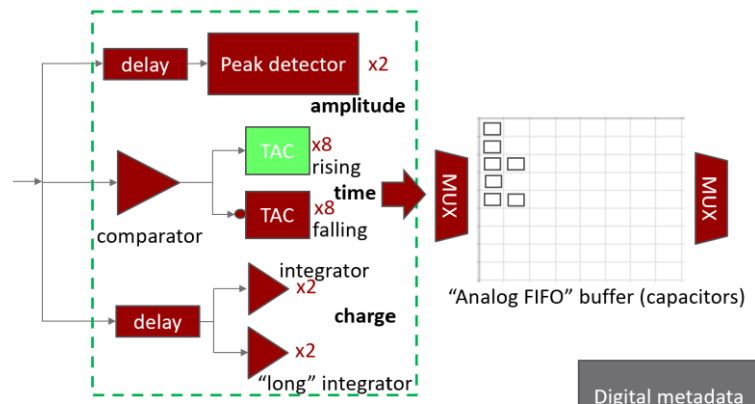


Comparator edges representing TOT events

TACs done for 1st TOT: leading and trailing edge times
Latched voltage represents "fine time" between clock edges

Write enables

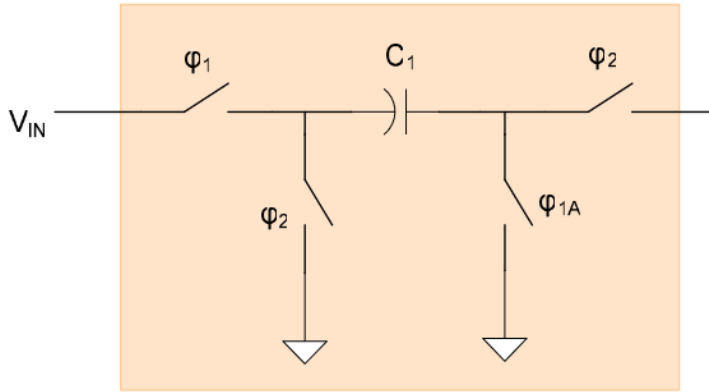
APP ASIC



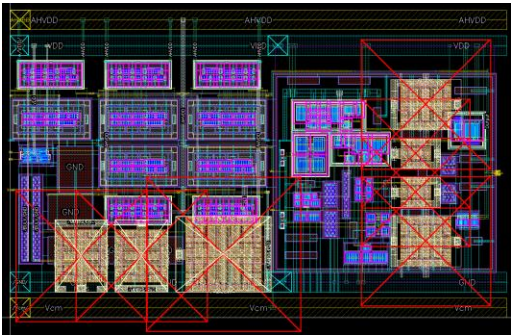
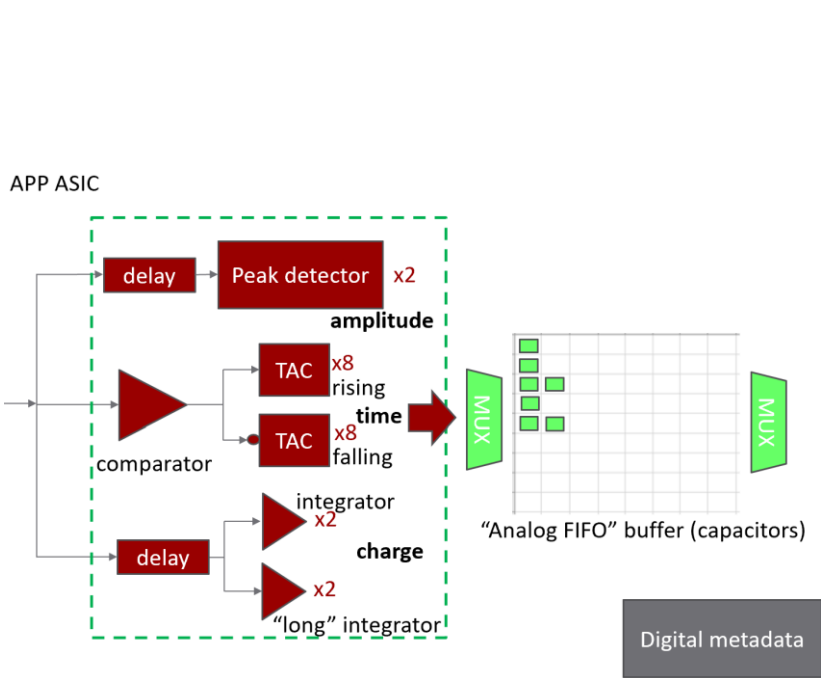
Digital metadata

*Image credit: <https://www.ortec-online.com/-/media/ametektortec/other/tac-time-calibrator.pdf>

Analog memory write



Simplified bottom plate sampling*



Memory cell layout

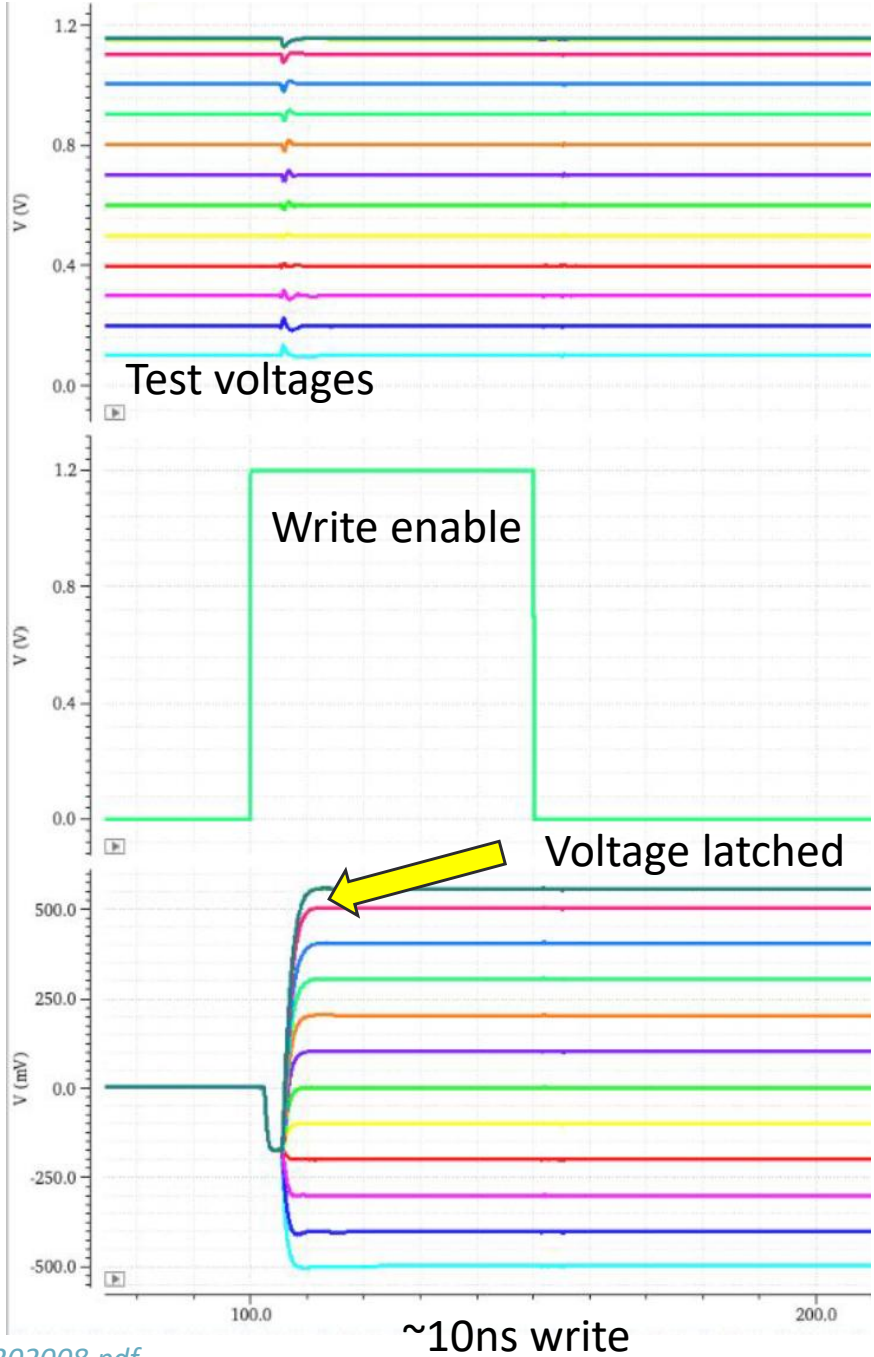
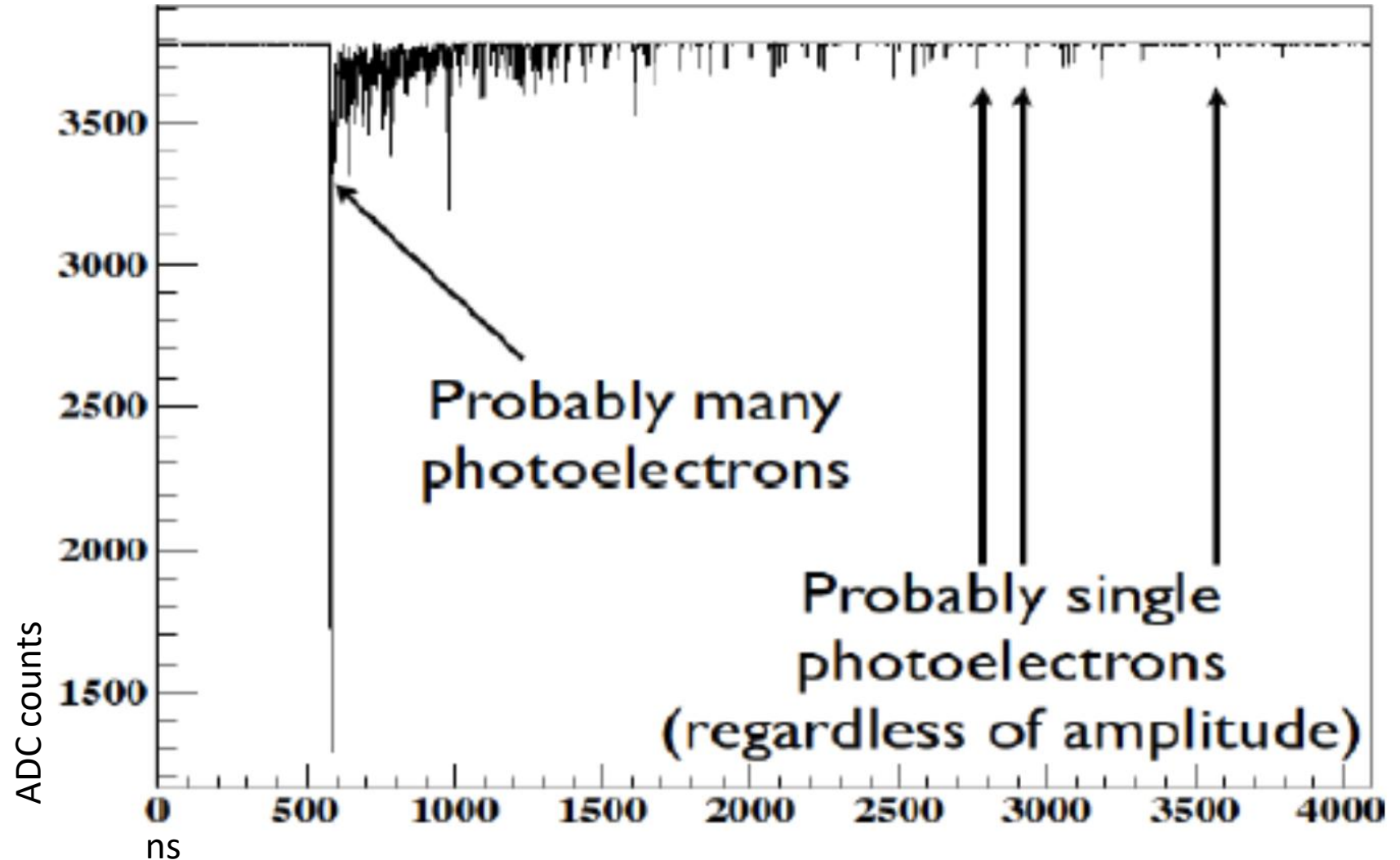


*Image credit: <https://class.ece.iastate.edu/ee435/lectures/EE%20435%20Lect%2044%20Spring%202008.pdf>



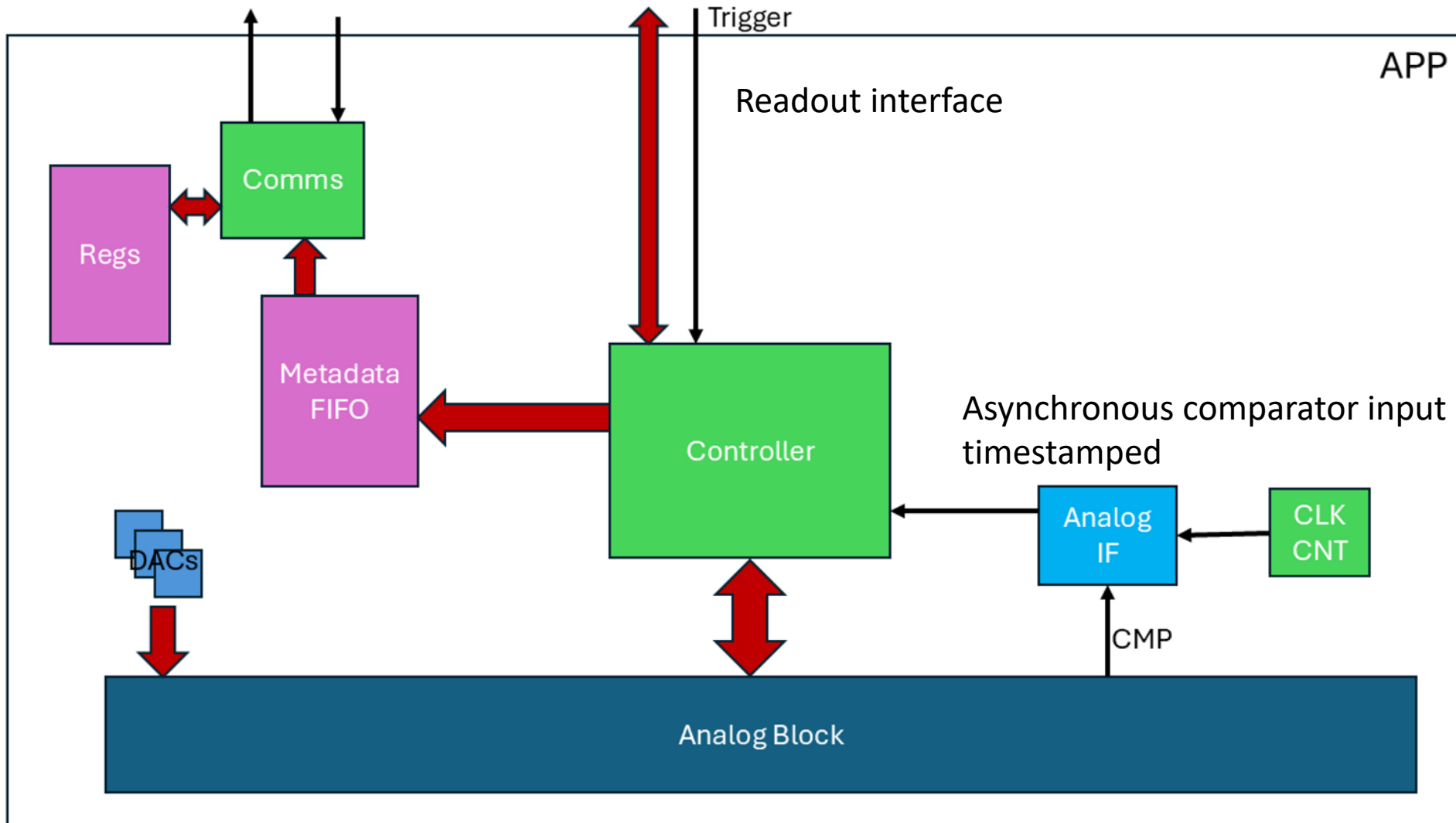
What happens in this case?

- Prompt region: Q gives good estimate of PE
 - Fast timing for Cherenkov light
- Tail region: PE counting more relevant
 - Multi-PE resolution and large dynamic range for scintillation light

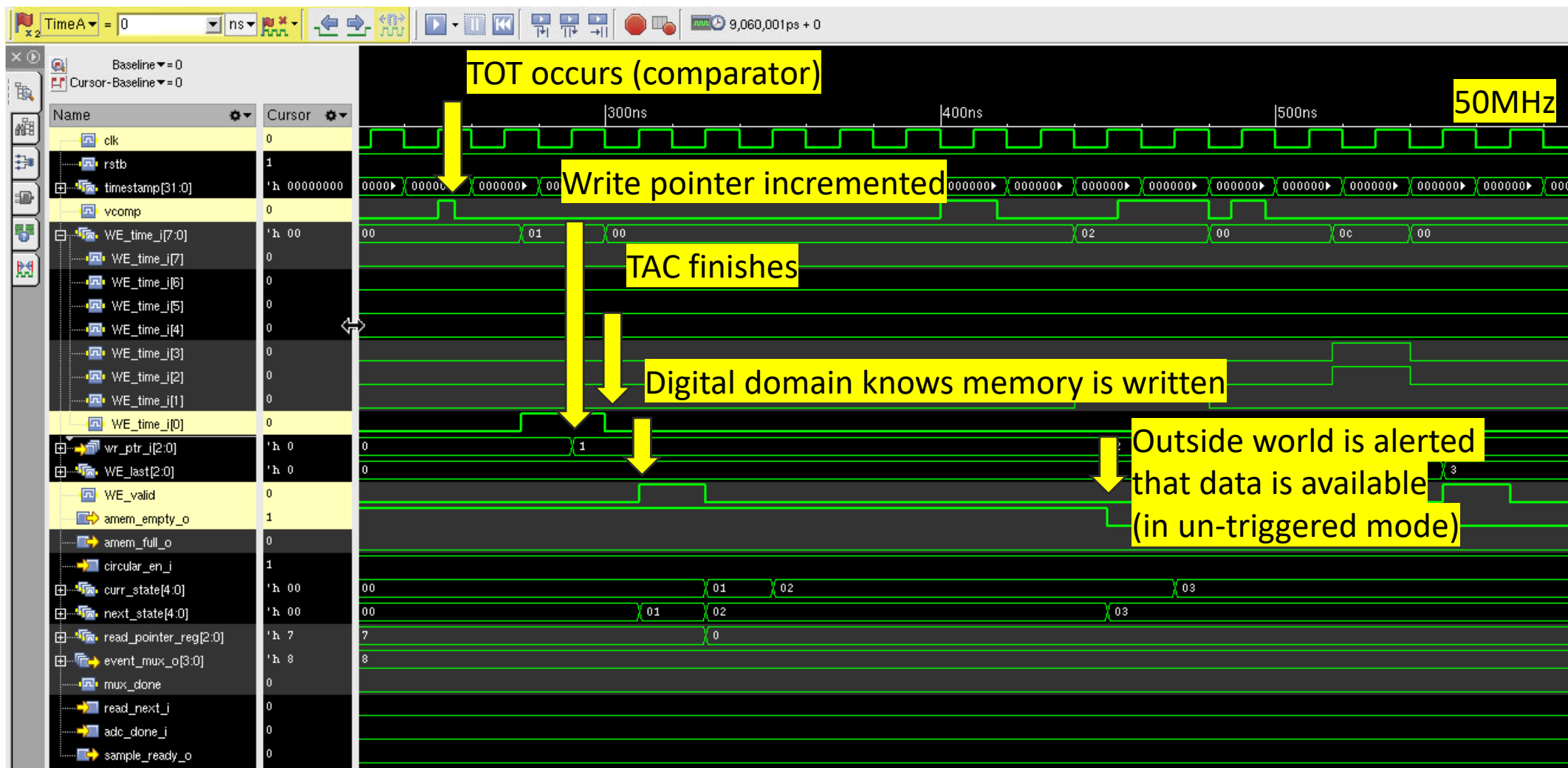


LAr waveform

Digital architecture



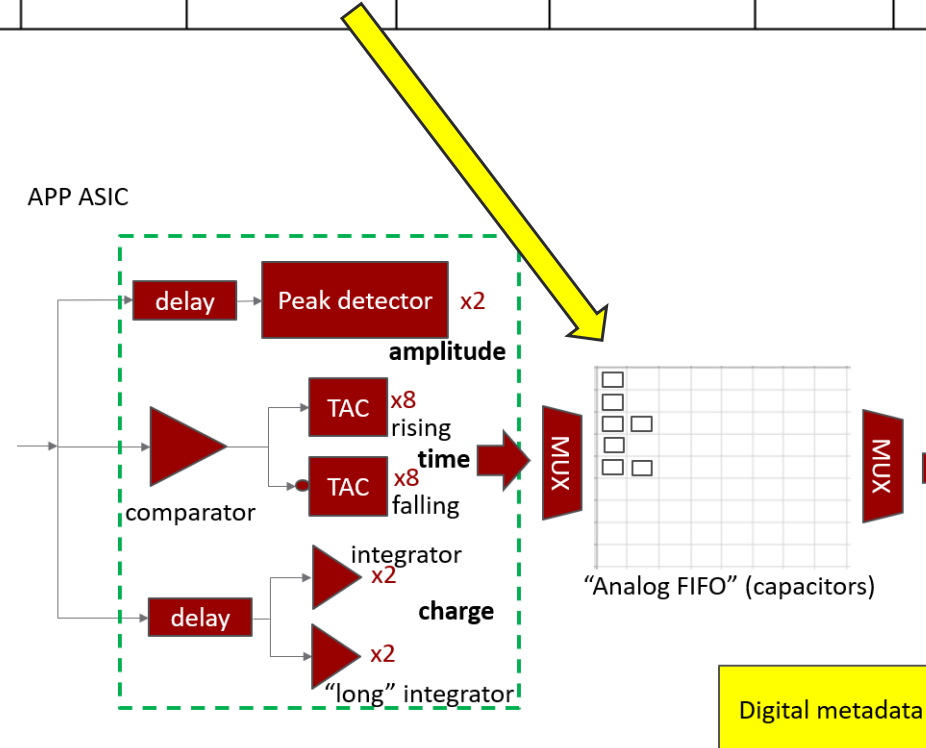
Digital memory write → alert outside world



Metadata

- TOT trailing edge less than 1 clock tick
 - All timing info in TAC value
- Memory “column” 0
- Untriggered mode
- Single peak event
- 11 ToTs occurred since reset
- No trigger ID associated with this
- APP did not flag any internal errors
- Packet type (TOT, register read, etc.)

Leading timestamp (32-bit)	Trailing timestamp (8-bit)	Memory column (3-bit)	Triggered (1-bit)	Single / double peak? (1-bit)	Global counter (5-bit)	GTID (5-bit)	Error (1-bit)	Packet type (4-bit)
0x0002fc98	0x98	3b000	1b0	1b0	5b01011	5b00000	1b0	4b0001

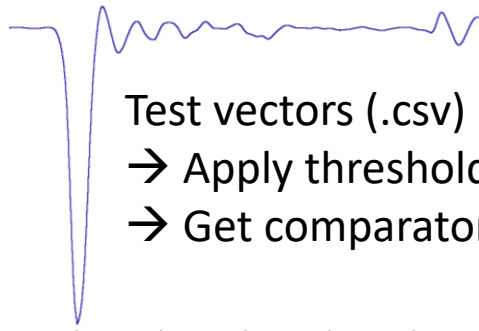




Simulation structure

APP

ANALOG domain

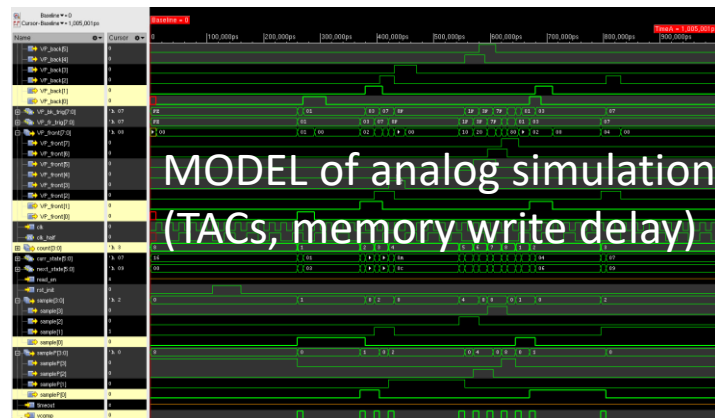
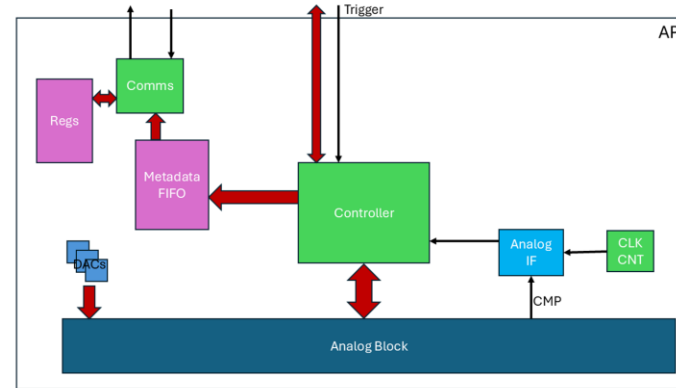


Test vectors (.csv)

→ Apply threshold

→ Get comparator “input”

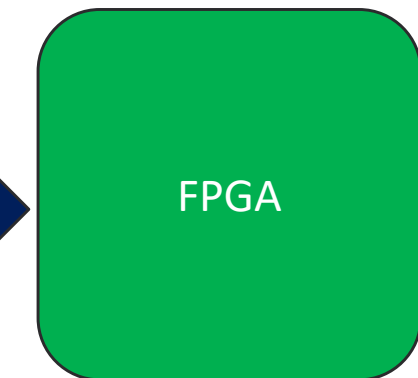
DIGITAL domain



MODEL of analog simulation
(TACs, memory write delay)

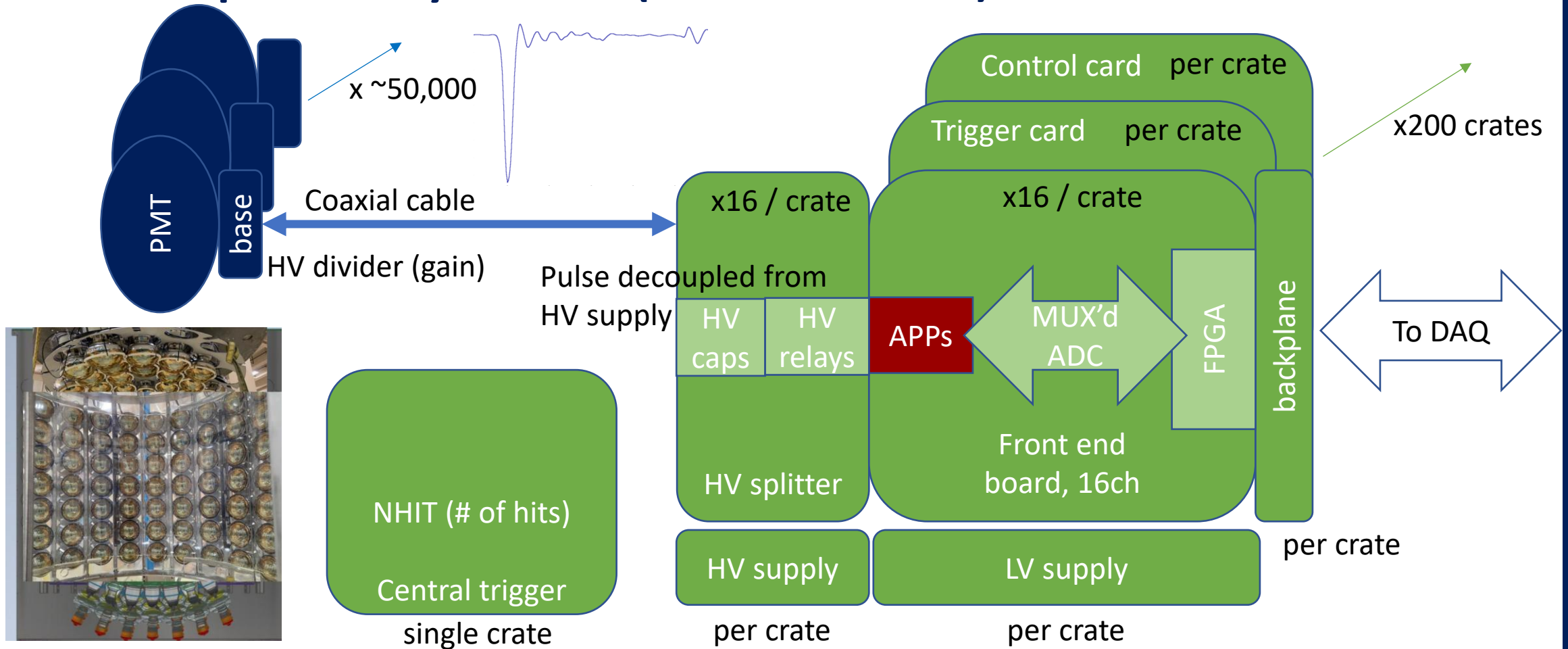
```
21 module amem_core #(parameter DEPTH=8)(
22   // Intra-chip signals (controller, register map, trigger)
23   input wire [2:0] wr_ptr_i, // from controller.sv
24   input wire [(DEPTH-1):0] valid_cells_i, // analog mem locations to read,
25   // from trigger
26   input wire circular_en_i, // chip reg setting to "cycle", 1 -> continuous
27   input wire LI_valid_i, // asserted at start of LI and deasserted at end
28   input wire triggered_mode_i, // 1 -> triggered, 0 -> untriggered
29   input wire [(DEPTH-1):0] WE_time_i, // TACs done on falling edge
30   output wire read_en_o, // goes to RE in analog memory
31   output wire [3:0] event_mux_o, // to sel_TOT event[3:1], and outside world
32   // XXX - sel_TOT_event needs a "Z" state !!
33
34   // Signals to/from outside world
35   input wire clk,
36   input wire rstb,
37   input wire trigger_i, // Valid trigger signal from outside world
38   input wire adc_done_i, // FPGA done taking a sample
39   input wire read_next_i, // FPGA asking to advance to next location
40   output wire sample_ready_o, // APP indicating MUX is set
41   output wire amem_empty_o, // wr_ptr = rd_ptr + 1
42   output wire amem_full_o, // asserted if circular_en = 0 and 8 locations full,
43   // or if rd_ptr = wr_ptr.
44   // Also wired to stopB internally to pause storage
45 );
```

- cocotb is a simulation framework that allows one to use Python to write testbenches
- Used successfully in the design and verification of ITk ASICs
- See talk by Paul Keener and Ben Rosser: <https://indico.global/event/14966/contributions/133732/>



OUTSIDE world

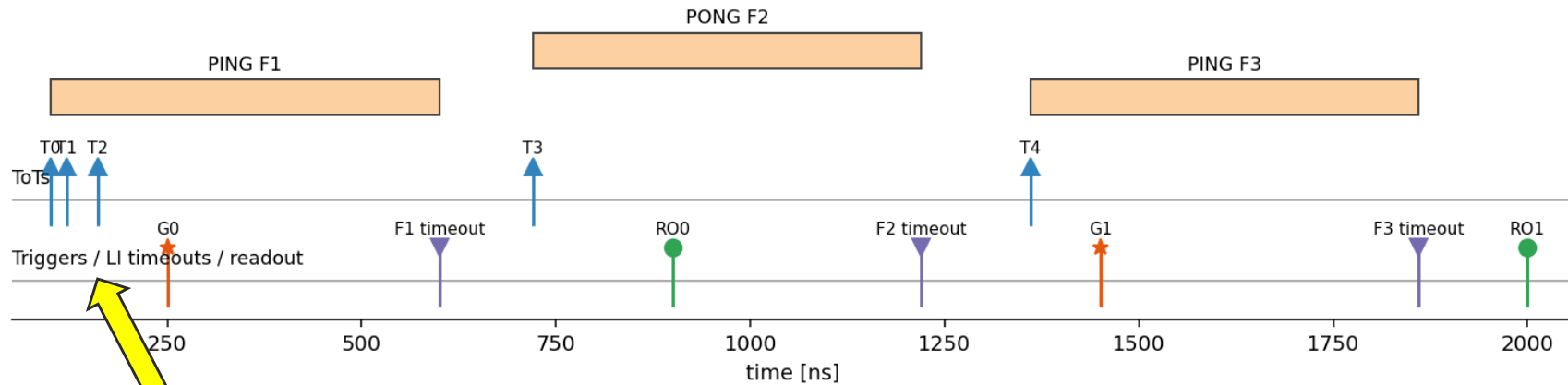
Conceptual system (a detector)



- Example: data rates for a large system $O(50k \text{ PMT})$
 - Untriggered WFD v. untriggered feature extraction: 7.5 EB v. 44 PB / year
 - Triggered WFD v. triggered feature extraction: 4 PB v. 160 TB / year
 - Best case: order(s) of magnitude reduction in data volume

Triggering logic

Specified ToT / trigger / readout times



3 TOT, then trigger

ToT written at 120.0 ns



ToT written at 160.0 ns



Trigger at 250.0 ns



F1: LI timeout, descriptor written

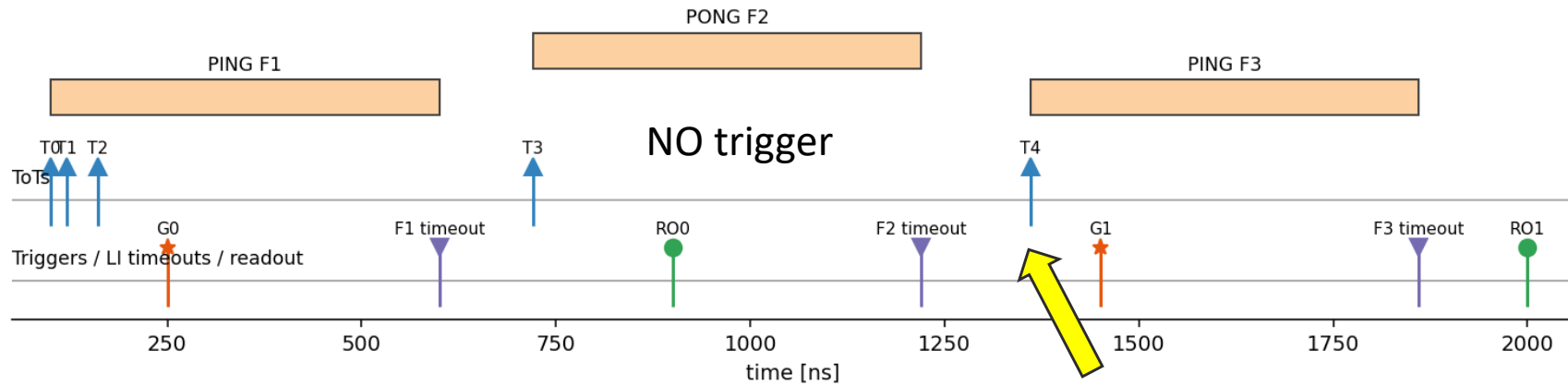


write pointer rolls over

trigger marks data to be read

Triggering logic

Specified ToT / trigger / readout times



F3: LI starts at 1360.0 ns



ToT written at 1360.0 ns



Trigger at 1450.0 ns



F3: LI timeout, descriptor written

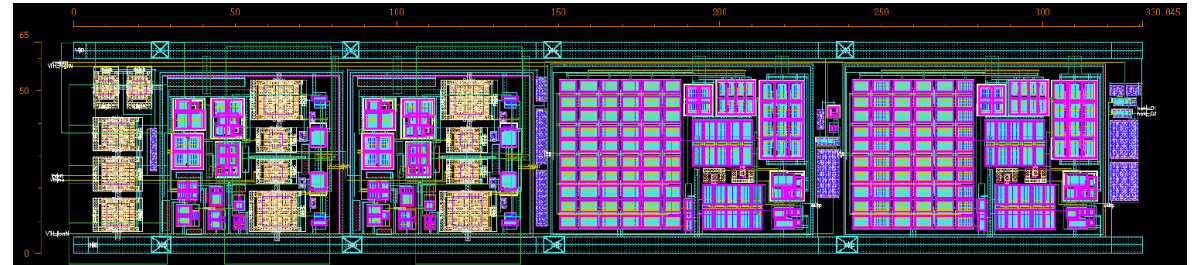


stale data; no trigger

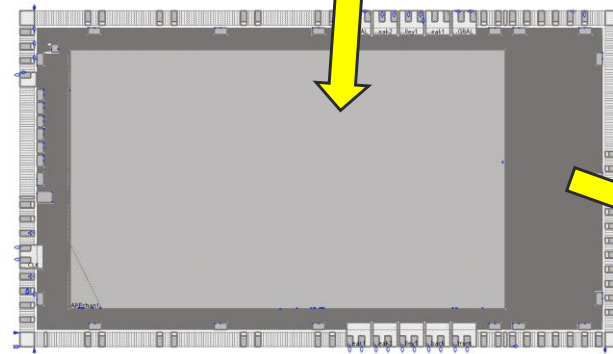
new data at T4

Summary

- The Analog Photon Processor is an analog feature extraction chip for future, moderate rate detectors
- Novel features of APP:
 - Nearly deadtime-less re-triggering
 - Peak amplitude and time measurements
 - Low cost per channel
- Many APP analog blocks have been extensively simulated:
 - Functionally
 - And over process
 - With real, representative data
- We are now assembling the chip, including digital metadata logic and triggering logic
- We are designing a test structure/demonstrator for APP

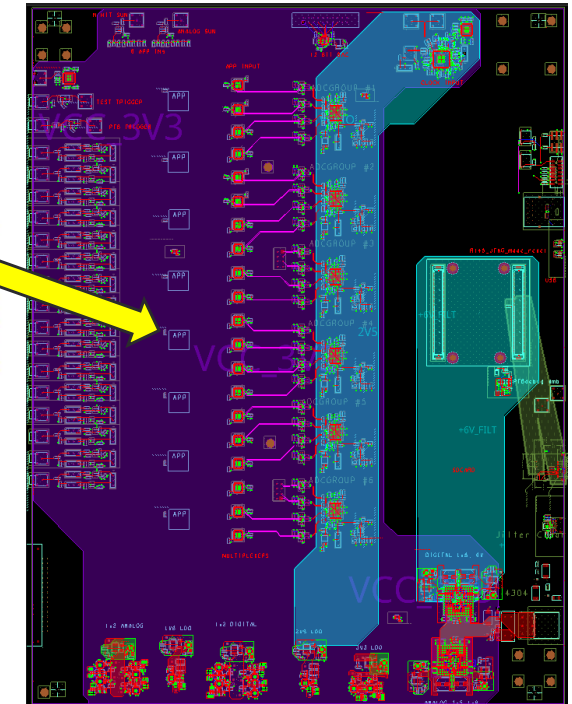


Peak detector layout



Chip floorplan: 3x5 mm
TSMC 65nm

Test PCB layout



Thank you!

- Current APP team: David Drobner³, Carl Grace⁸, Paul Keener², Josh Klein¹, Godwin Mayers², Mitch Newcomer², Adrian Nikolica², Ravi Pitelka³, Rick Van Berg², Jihao Yang²
- Past contributors: Nandor Dressnandt², Yiming He⁴, Bill Heintzelman⁷, Ben Land⁶, Chengjun Li⁴, Ke Liu⁴, Xiaokai Ma⁴, Max Malakhovets⁵, Meijun Tian⁴, Hao Yan⁴

¹Principal investigator

²Instrumentation group

Physics ⁶postdocs, ³PhD students, ⁷visiting scholars

Electrical Engineering ⁴Master's students, ⁵undergraduate students

⁸Collaborators



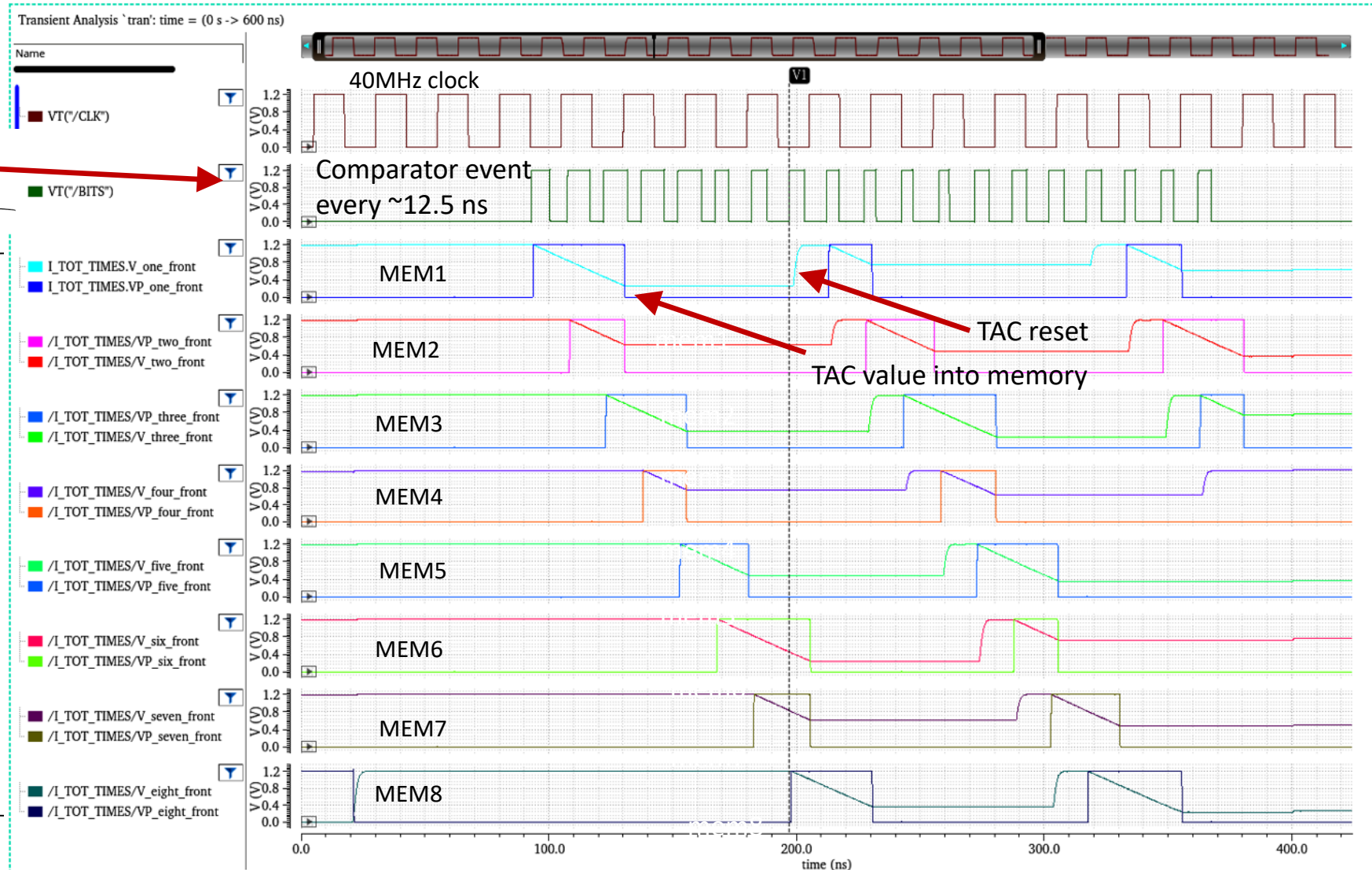


Backup

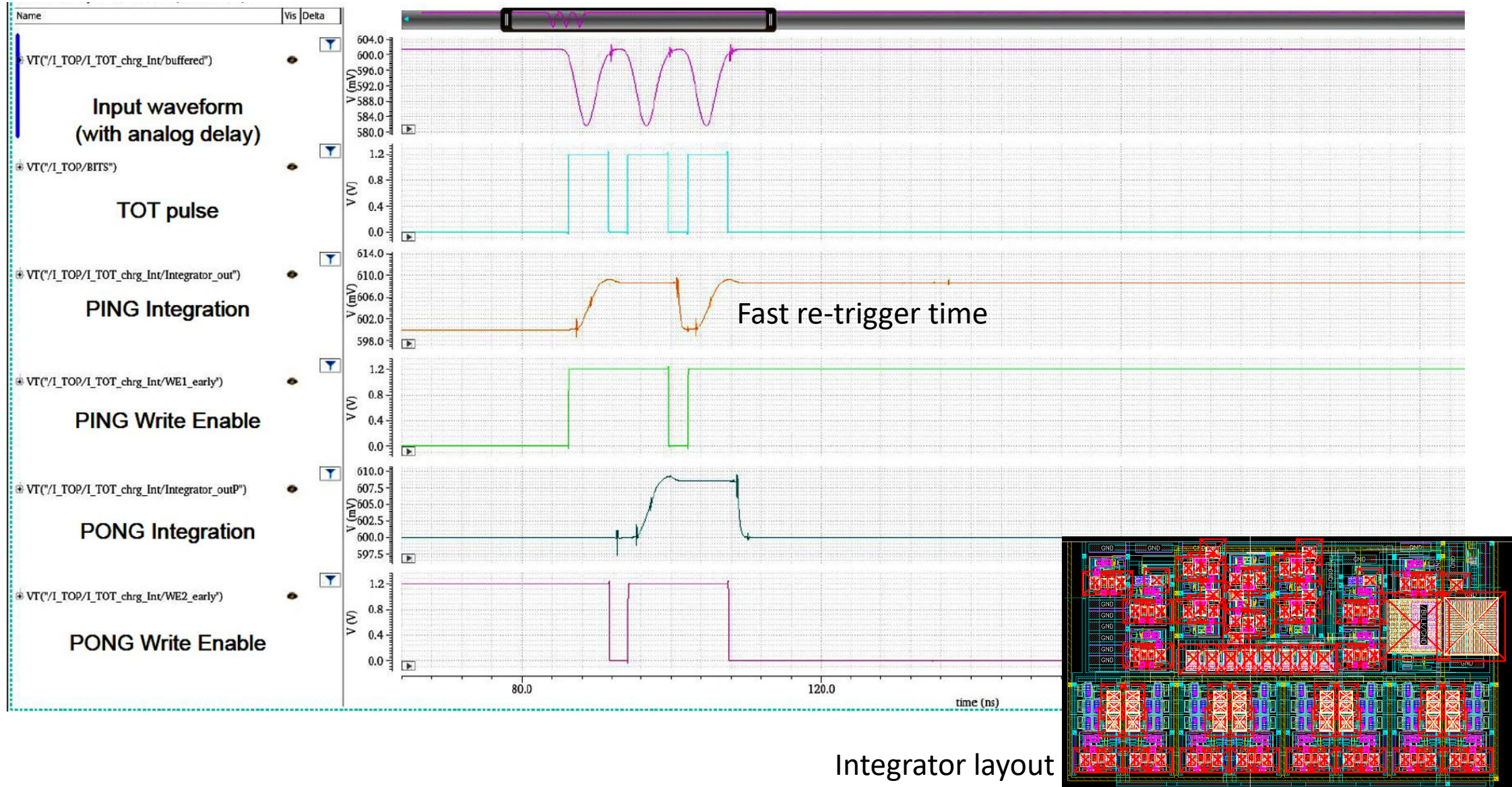
Simulated performance to date

Quantity	Design specification	Comment
Pulse-pulse deadtime	sub ns	“ping-pong-ping” re-trigger @ 1pe
Leading edge time precision	25ps	@ 10-bit ENOB (~12-bit ADC)
TOT precision	35ps	2 edges, in quadrature
Single TOT integral dynamic range	1/4 – up to 200 PE (@ 5mV / pe)	1/5 PE intrinsic noise
Single TOT integral resolution	1/5 PE	
Long integral dynamic range	1 – up to 1000 PE (@ 0.5mV / pe)	1 PE intrinsic noise
Long integral resolution	~1 PE	
Peak height dynamic range	1 – 60 PE	Typical 10 mV / PE @ 10^7 PMT gain
Peak height resolution	1/4 PE	
Peak time precision	1ns	
TOT FIFO depth	8	
Long integral FIFO depth	4	
FIFO write time	~10ns	
FIFO read time	~50ns	

Full channel analog simulation

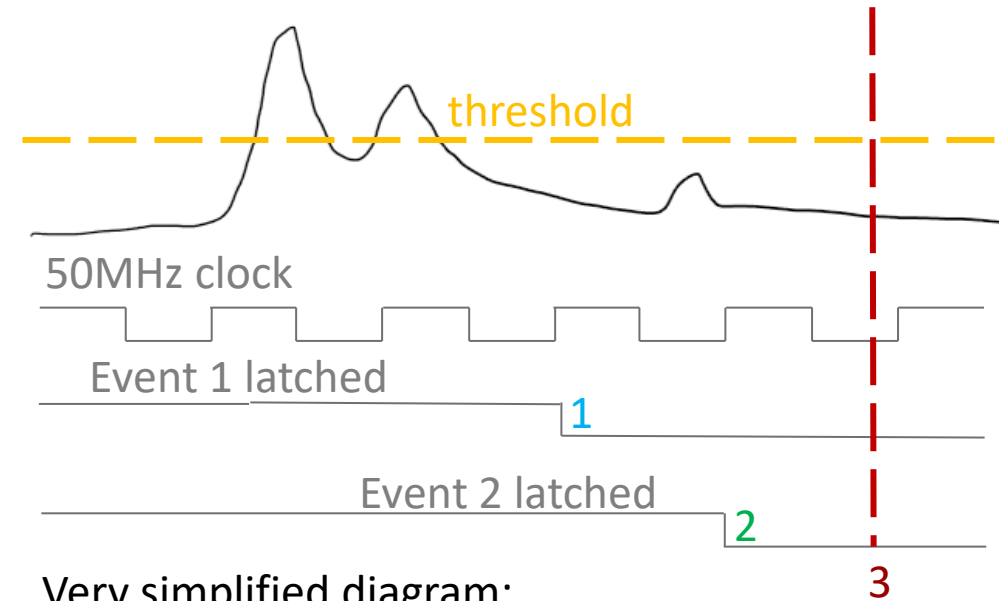


Simulation: integration, 8ns pulse separation



Example #1

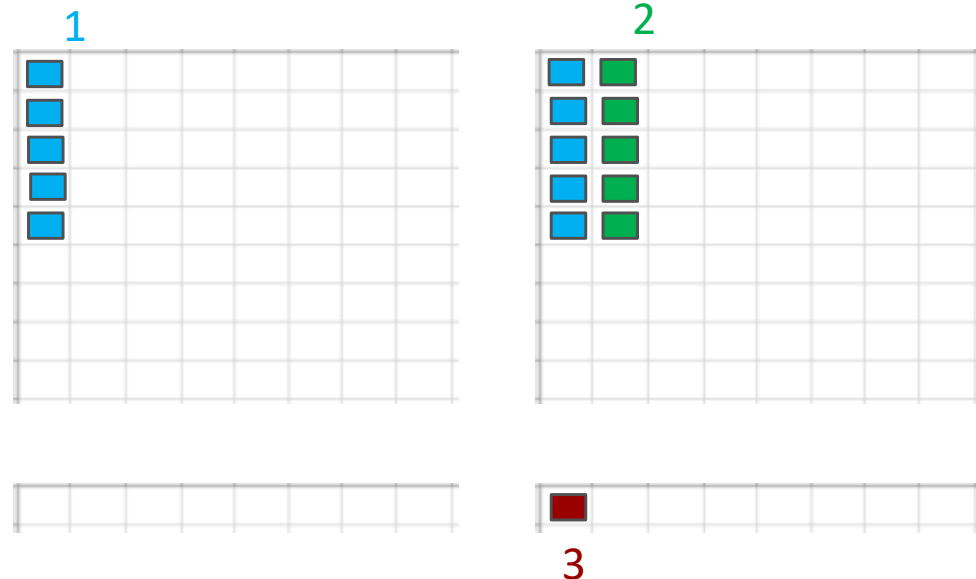
- Ping-pong architecture can store 2 closely spaced peaks
- ➔
- Second peak is counted as a separate event, and measurements #6—9 are not stored
 - The “long charge” measurement #10 is always a separate analog memory



Very simplified diagram:

2 sample snapshots of analog memory shown
(not all digital signals shown)

1. Leading edge time
2. Trailing edge time
3. Integral (Q)
4. Time of 1st peak
5. Amplitude of 1st peak
6. Time of 2nd peak
7. Amplitude of 2nd peak
8. Time of 1st valley
9. Amplitude of 2nd valley



Key metadata at 2:

b0001 – packet type (data)

b0 – not a “long charge”

32-bit + 8 timestamps –
leading/trailing edges

b0 – single peak

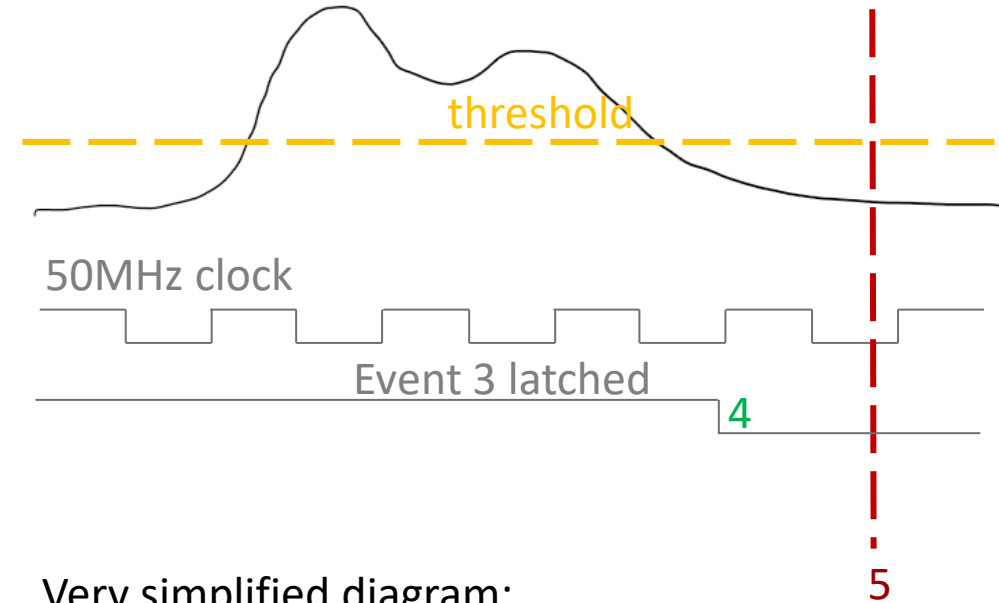
b001 – memory “column”

10. Integral of total charge over a
programmable time starting with the
1st event



Example #2

- Ping-pong architecture can store 2 closely spaced peaks
 - Second peak is counted as a separate event, and measurements #6—9 are not stored
 - The “long charge” measurement #10 is always a separate analog memory
- ➔ • Entire TOT is a double peak event



Very simplified diagram:

1 sample snapshots of analog memory shown
(not all digital signals shown)

Key metadata at 4:

b0001 – packet type (data)

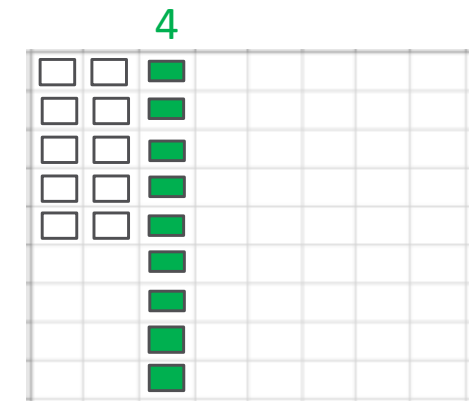
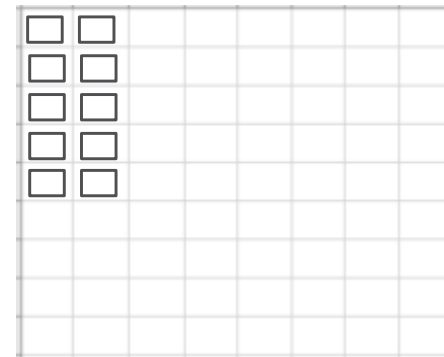
b0 – not a “long charge”

32-bit + 8 timestamps –
leading/trailing edges

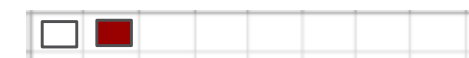
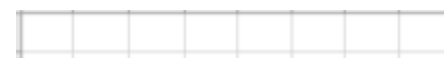
b1 – double peak

b010 – memory “column”

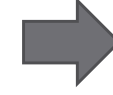
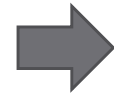
1. Leading edge time
2. Trailing edge time
3. Integral (Q)
4. Time of 1st peak
5. Amplitude of 1st peak
6. Time of 2nd peak
7. Amplitude of 2nd peak
8. Time of 1st valley
9. Amplitude of 2nd valley



10. Integral of total charge over a programmable time starting with the 1st event



- PMT
inputs



Ethernet
readout