

KrIO

A REUSABLE DATA ACQUISITION MODULE FOR THE KRIA K26

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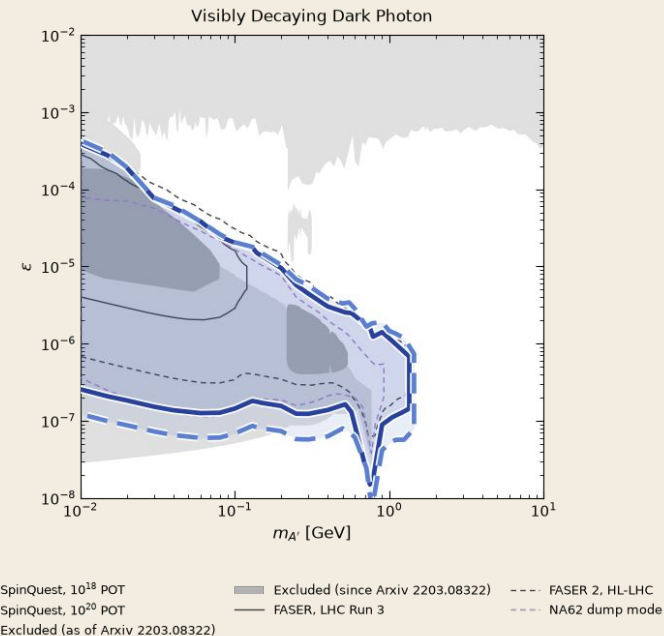
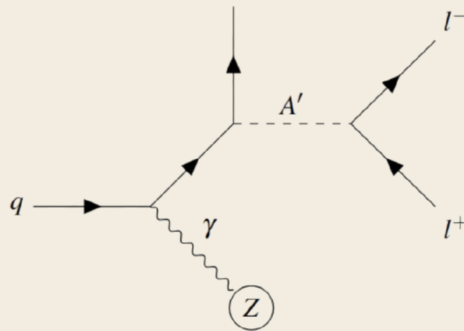
[www.noahpaladino.com/krio]

(¹MIT | ²JHU | SpinQuest)

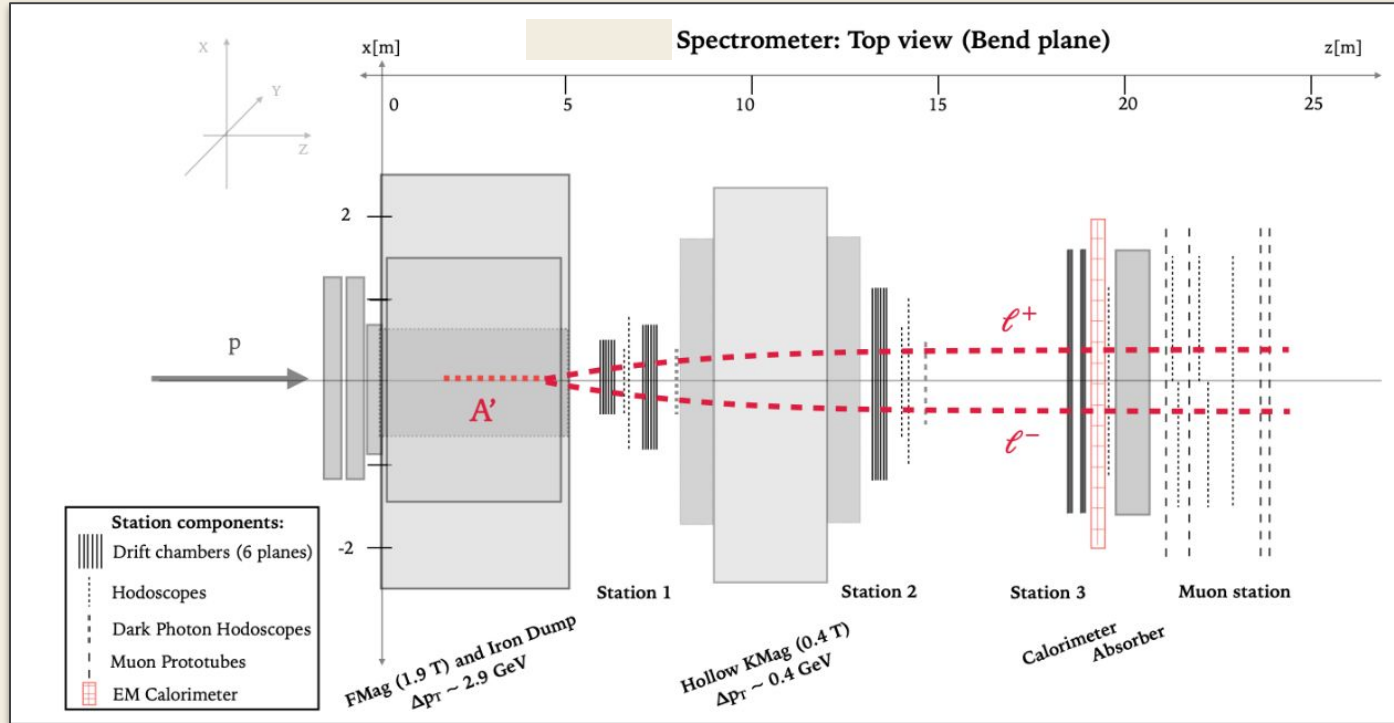
Background

The SpinQuest Experiment and Dark Photons

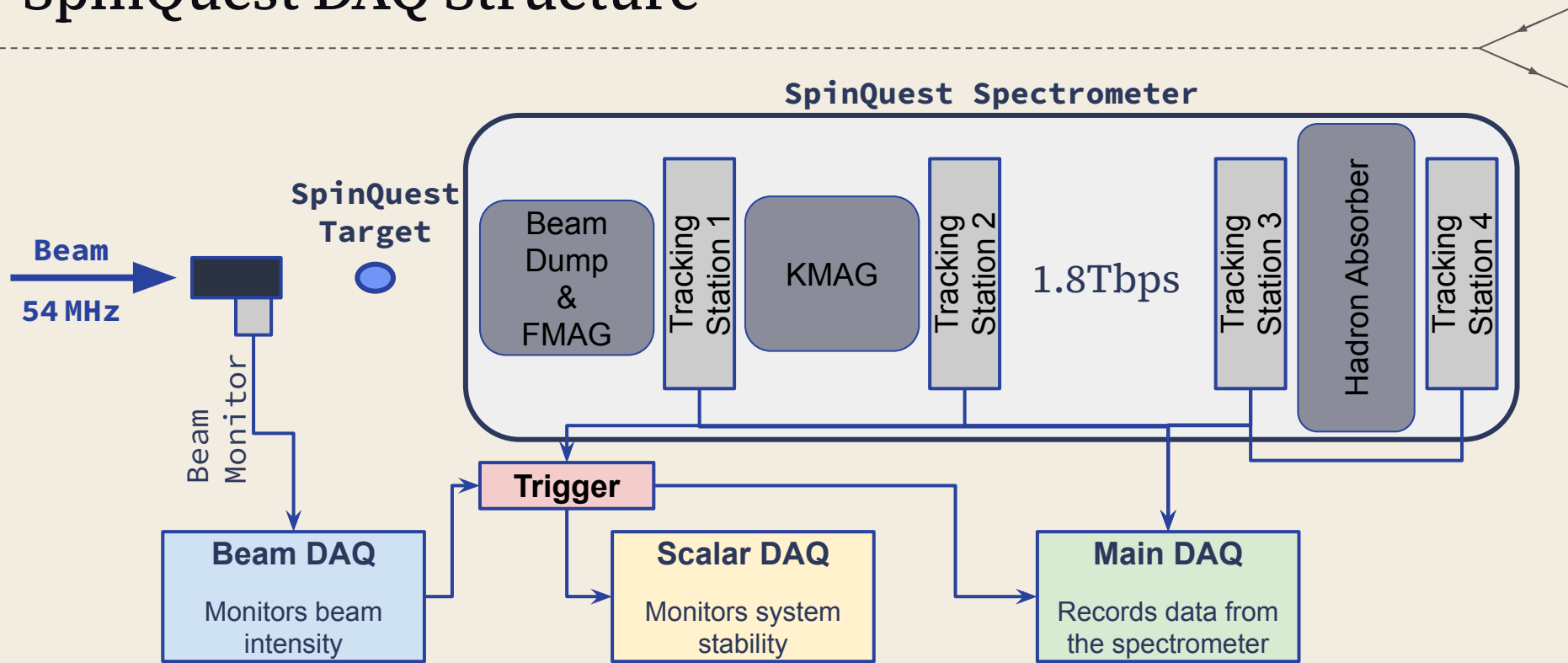
- Proton on spin-polarized target experiment
- Tracks dimuon pairs to make inferences about where the proton gets its spin
- **Dark photons** are like a photon we can't see
 - Potentially a form of dark matter
 - Can be produced in the same ways as the standard photon and can decay to electron/muon pairs



Dark Photon Searches at SpinQuest

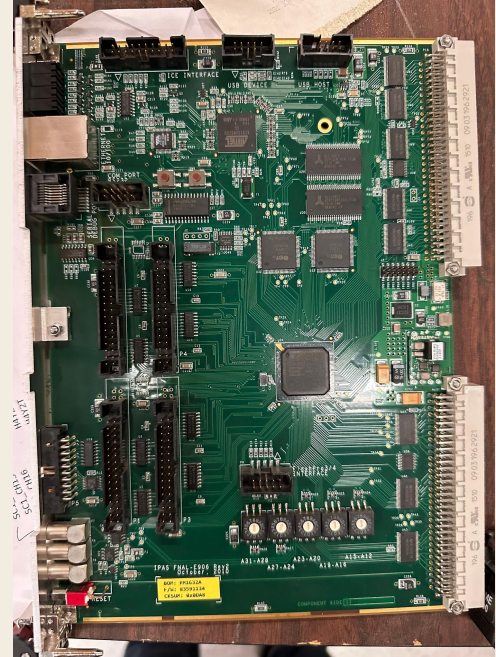


SpinQuest DAQ Structure



Current Time-to-Digital Converter Boards

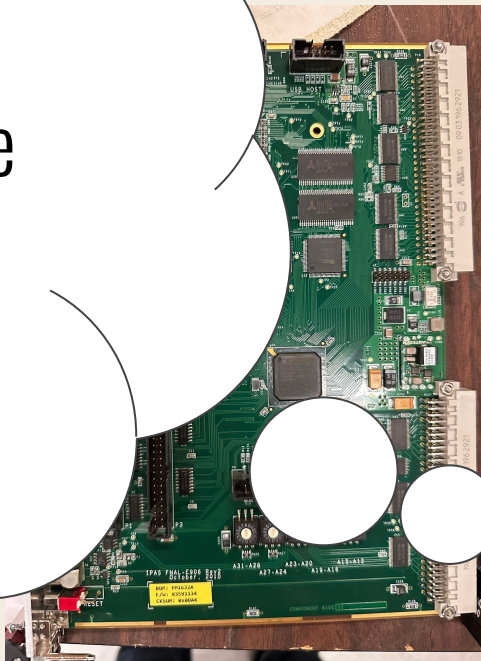
- Time-to-Digital Converter (TDC) boards are custom-designed and interface via VME backplane
- 1 (very, very old) ARM microcontroller and 1 FPGA, with shared memory
- Issues:
 - FPGA->MCU->Buffer->MCU->FPGA->VME backplane->CPU->network data flow introduces latency and overhead
 - Buffers are too small for trigger rates $>8\text{KHz}$, which is detrimental to dark photon search performance



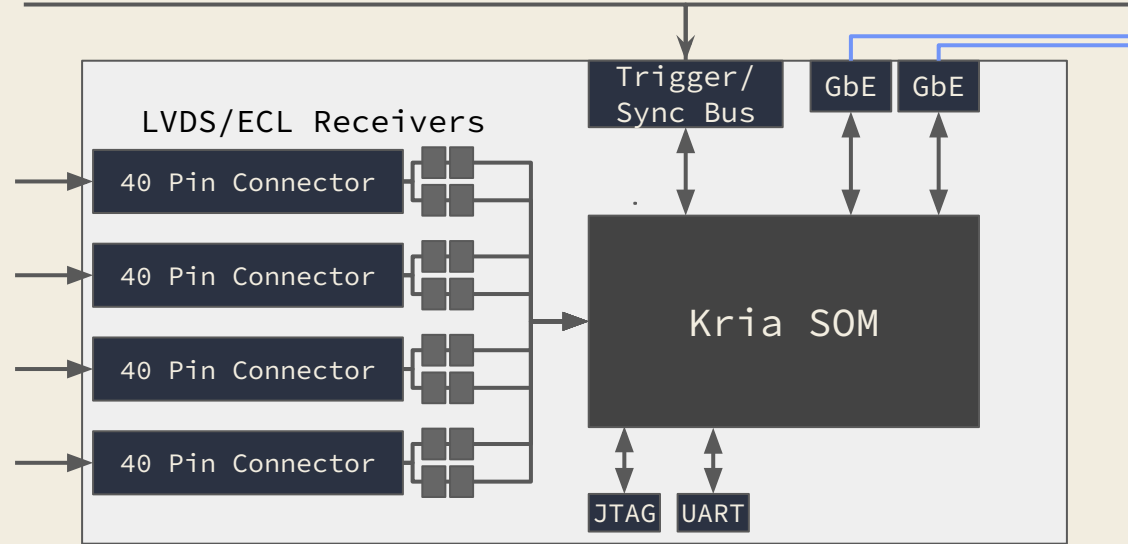
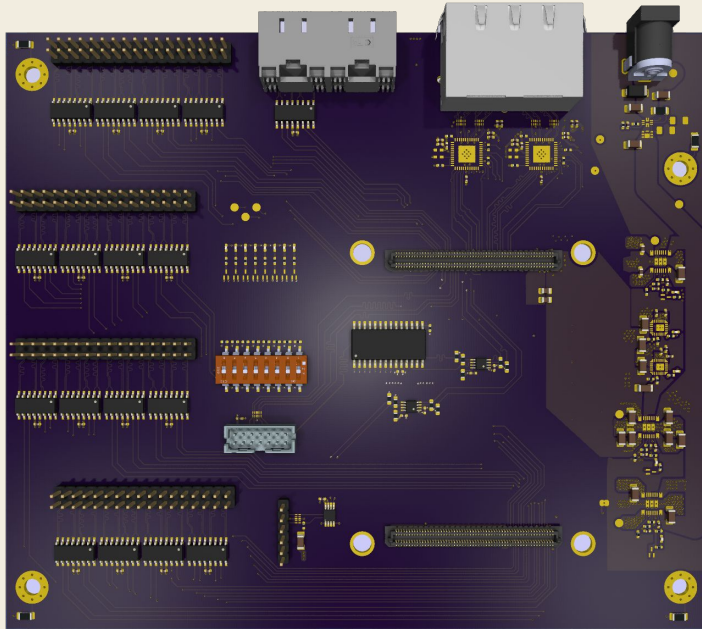
Current TDC Boards

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- 1 (very, very) 1 FPGA, w
- Issues:
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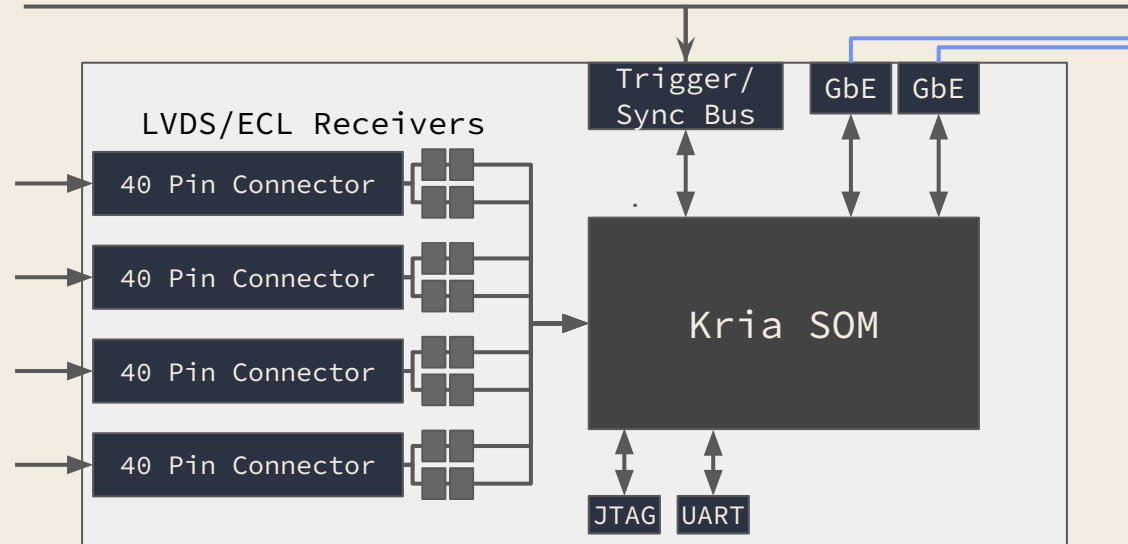
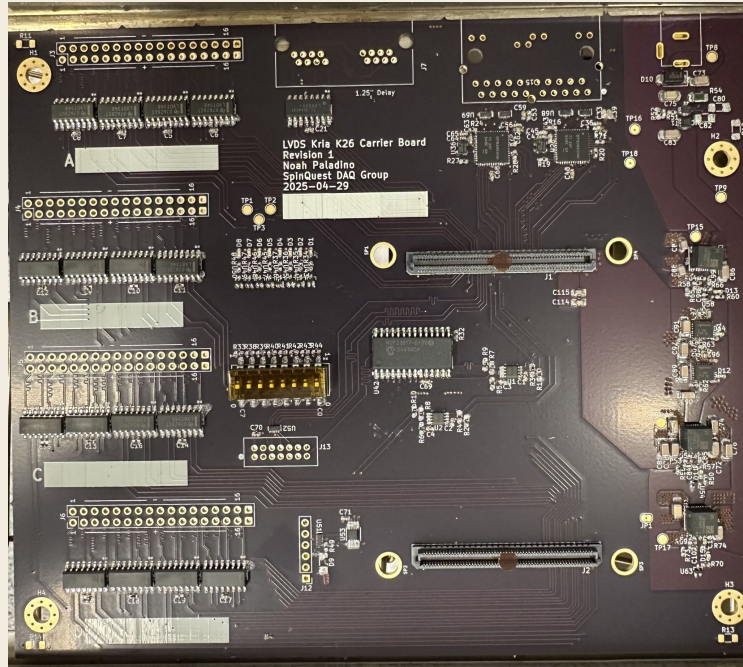
FPGA+ARM? Sounds like a System-on-Chip with extra steps...



TDC Update Proposal - Kria

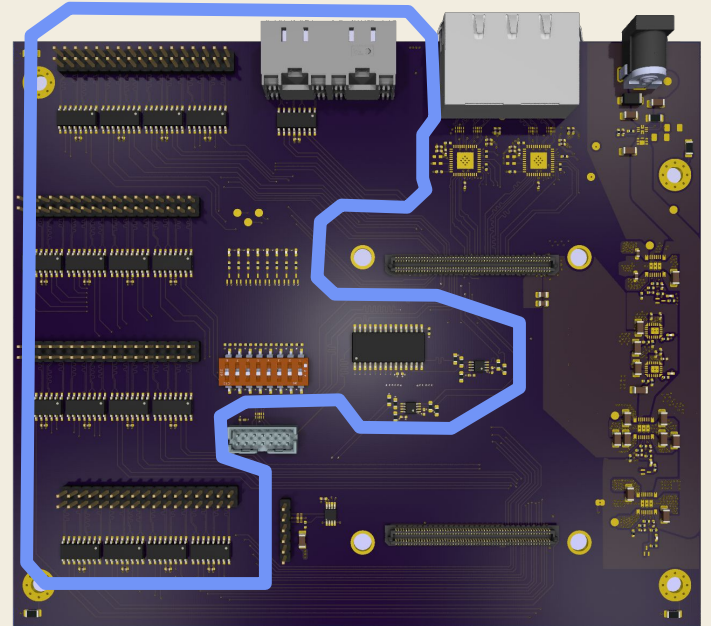


TDC Update Proposal - Kria



Carrier Board Simplification

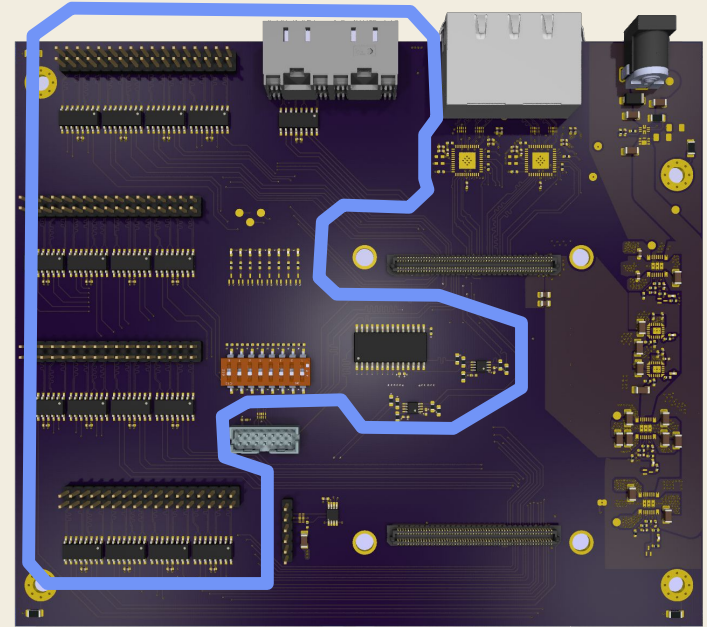
- About half the carrier board doesn't require multiple power planes and strict impedance control
- This region is also very particular to our use case, but the rest isn't...



Carrier Board Simplification

- About half the carrier board doesn't require multiple power planes and strict

Maybe we can
standardize this for use
with other experiments
now too...



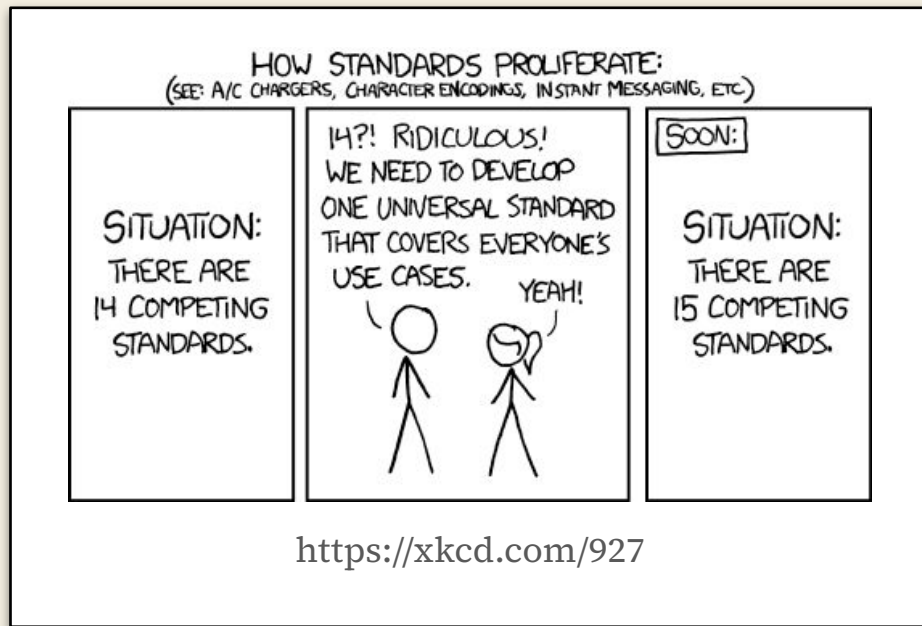


Introducing KrIO:

A Low-Cost, High-Throughput DAQ System

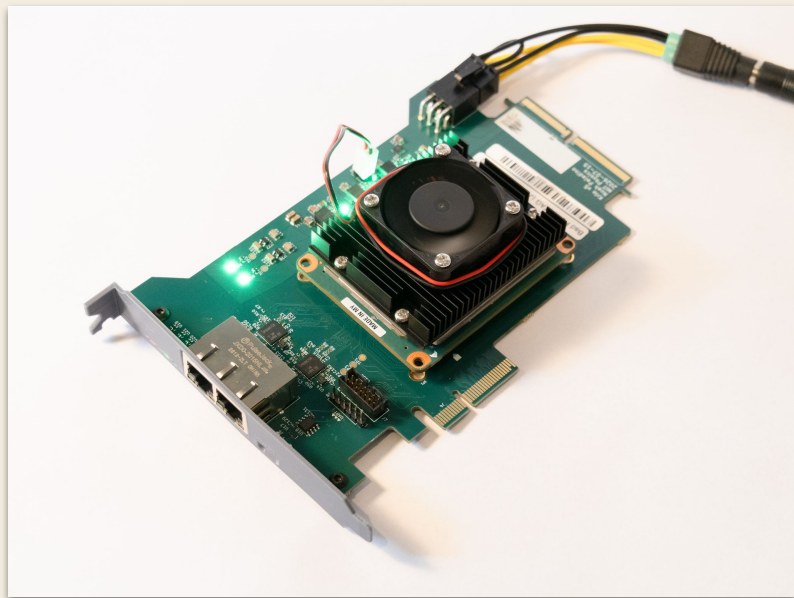
Why?

- Not every experiment needs a brand new, custom FPGA board
- Using development kits doesn't scale well
 - Power, order quantity restrictions
 - Too many unused interfaces
- Existing GPIO connector standards either lack density, speed, or ease-of-use

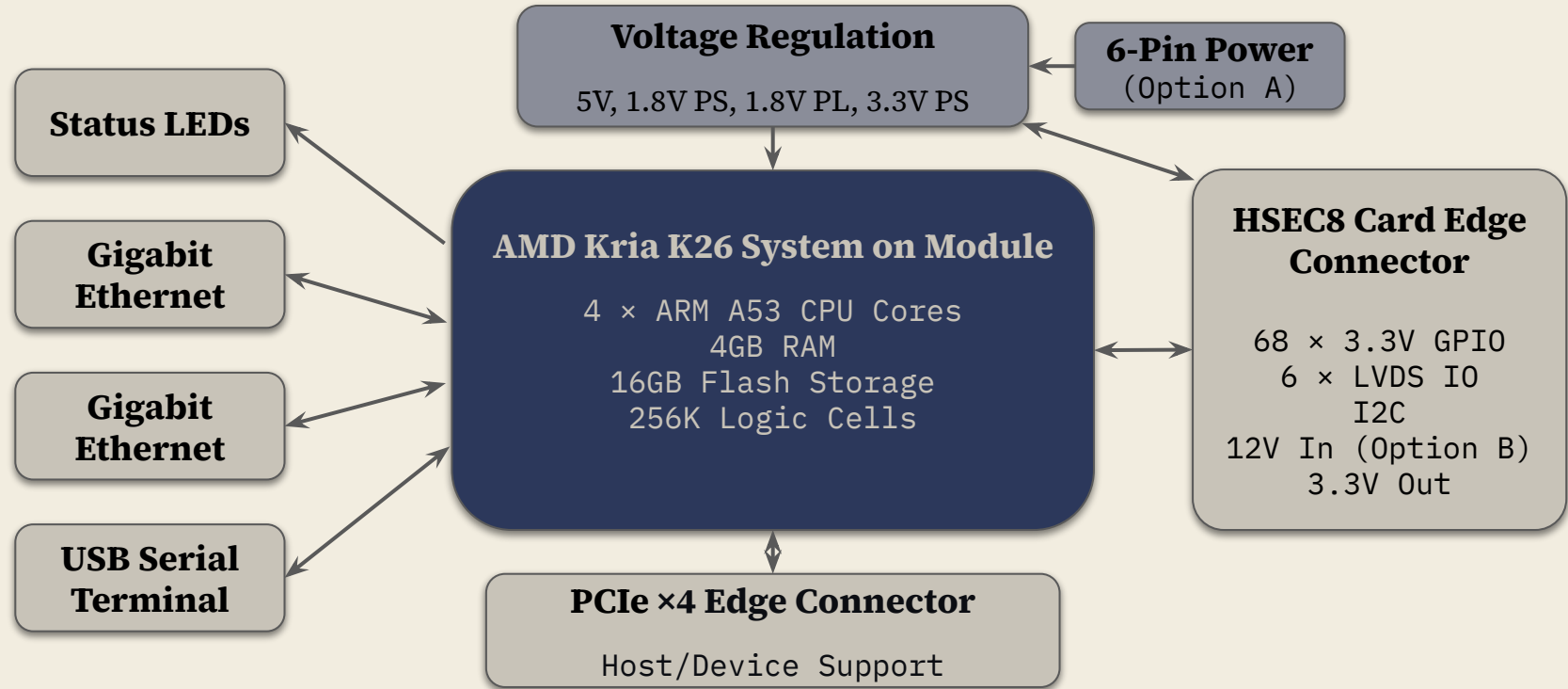


What KrIO IS:

- **High-throughput** data (pre)processing hardware
- Easy-to-integrate readout via two **gigabit Ethernet** ports
- A **PCI Express ×4** card form factor to fit in standard computer cases
- **Open Source** hardware design

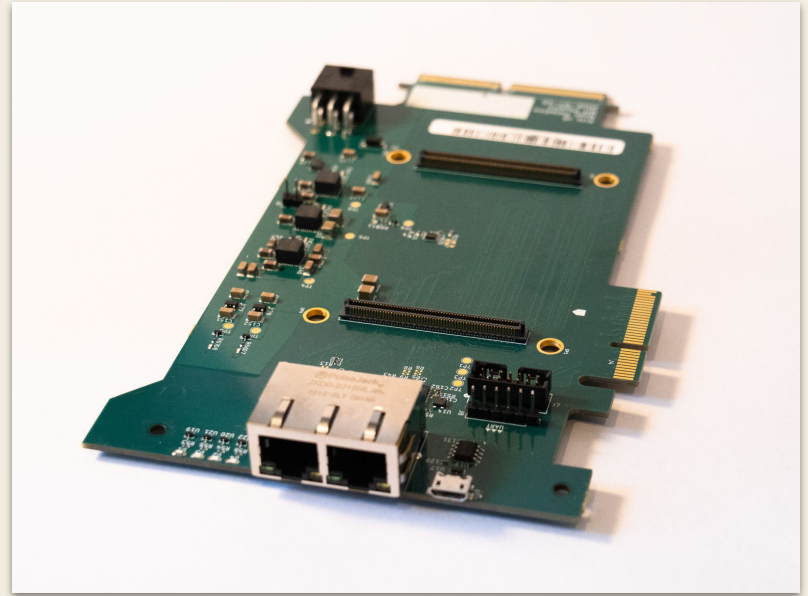


Block Diagram



What KrIO ISN'T:

- A **full replacement** for your front-end electronics
 - Digitization hardware is still required
- A **complete** Kria K26 SoM dev board
 - Not every feature is broken out (intentionally)
- The answer to life, the universe, and everything



Comparison

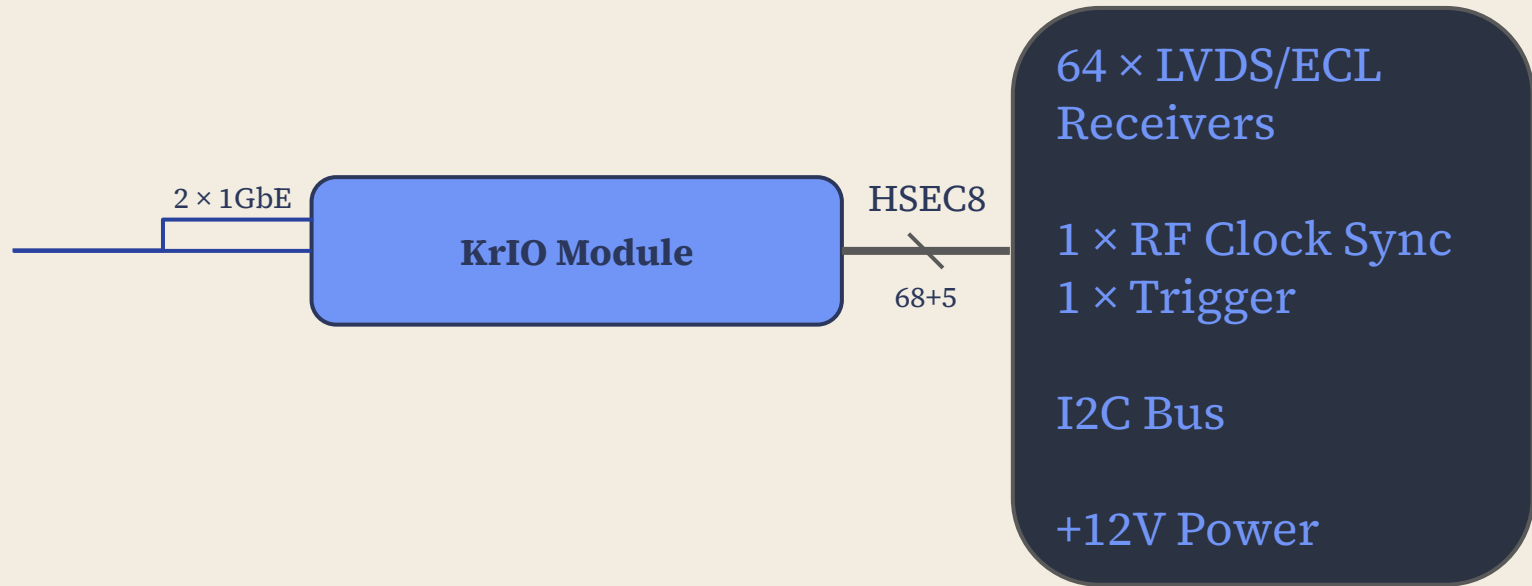
	KrIO	KR260	AUP-ZU ₃	Genesys ZU	PYNQ-Z1
CPU	4 × ARM A53	4 × ARM A53	4 × ARM A53	4 × ARM A53	2 × ARM A9
RAM	4GB	4GB	4GB	4GB	512MB
Storage	16GB Flash	MicroSD Card	MicroSD Card	MicroSD Card	MicroSD Card
Ethernet	2 × 1 Gigabit	2 × 1 Gigabit*	1 × 1 Gigabit	1 × 1 Gigabit	1 × 1 Gigabit
PCIe	×4 Host/Device	N/A	N/A	×1 Host	N/A
Exposed GPIO (S+D)	68+5	58+6**	54+2	66+33	65
Logic Cells	256k	256k	154k	154k	13k
Cost	~\$150+\$325 (K26)	\$349	\$274 (Academic)	\$1,312	\$314

* Additional 2 × 1G + 10G via (paid) soft IP

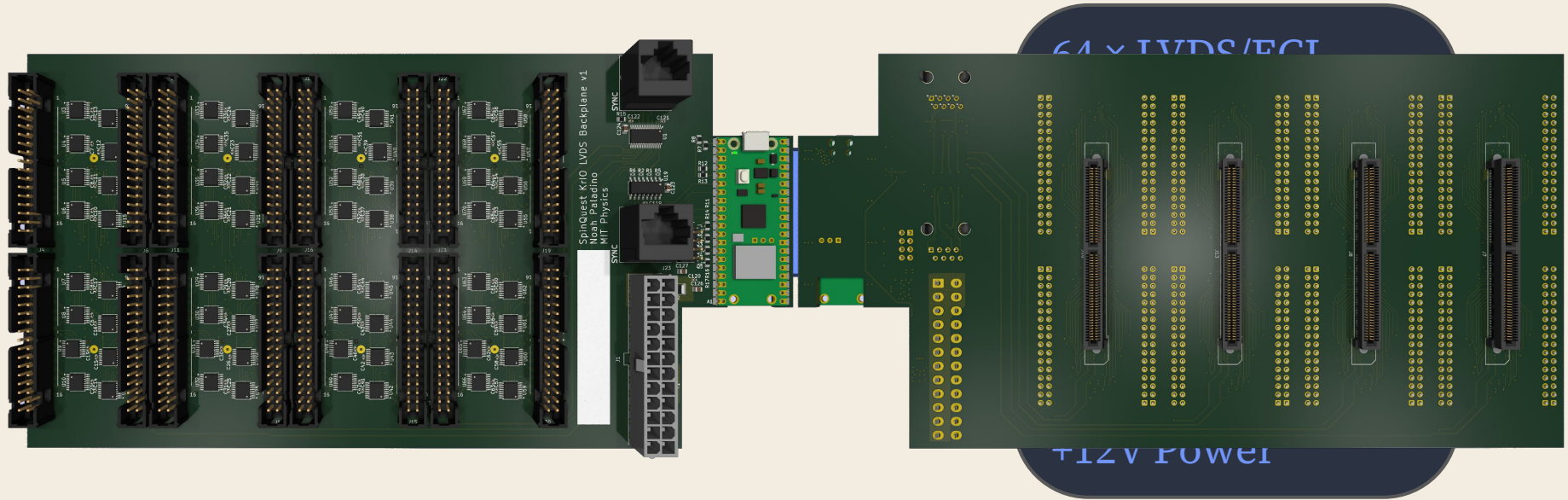
** Differential available via camera connector

KrIO Frontends

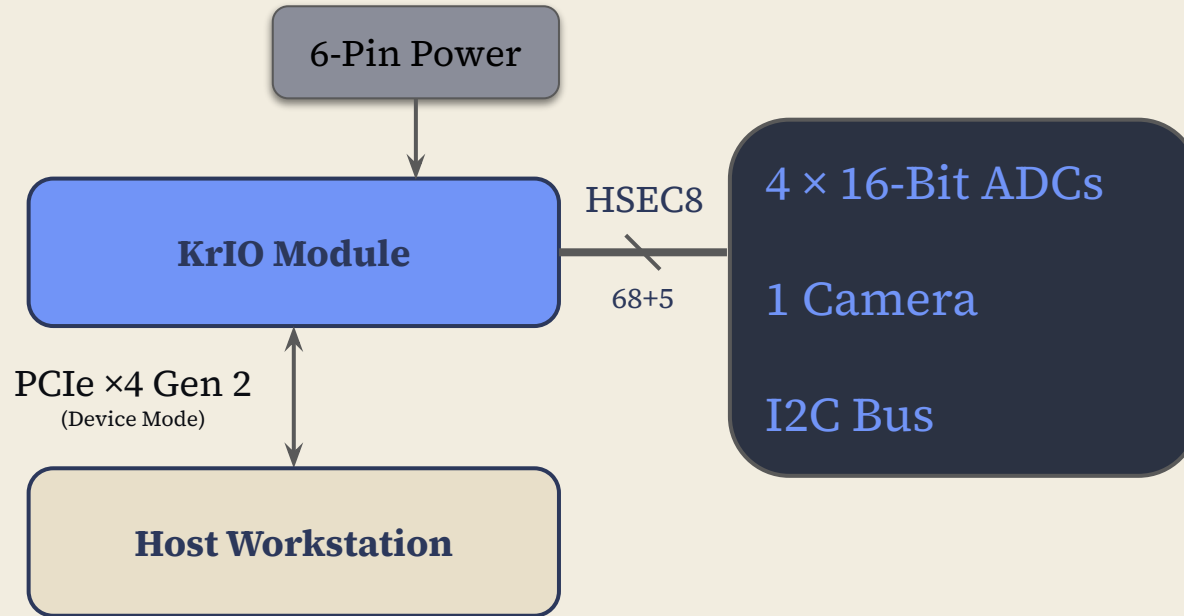
Example Frontend - LVDS/ECL TDC



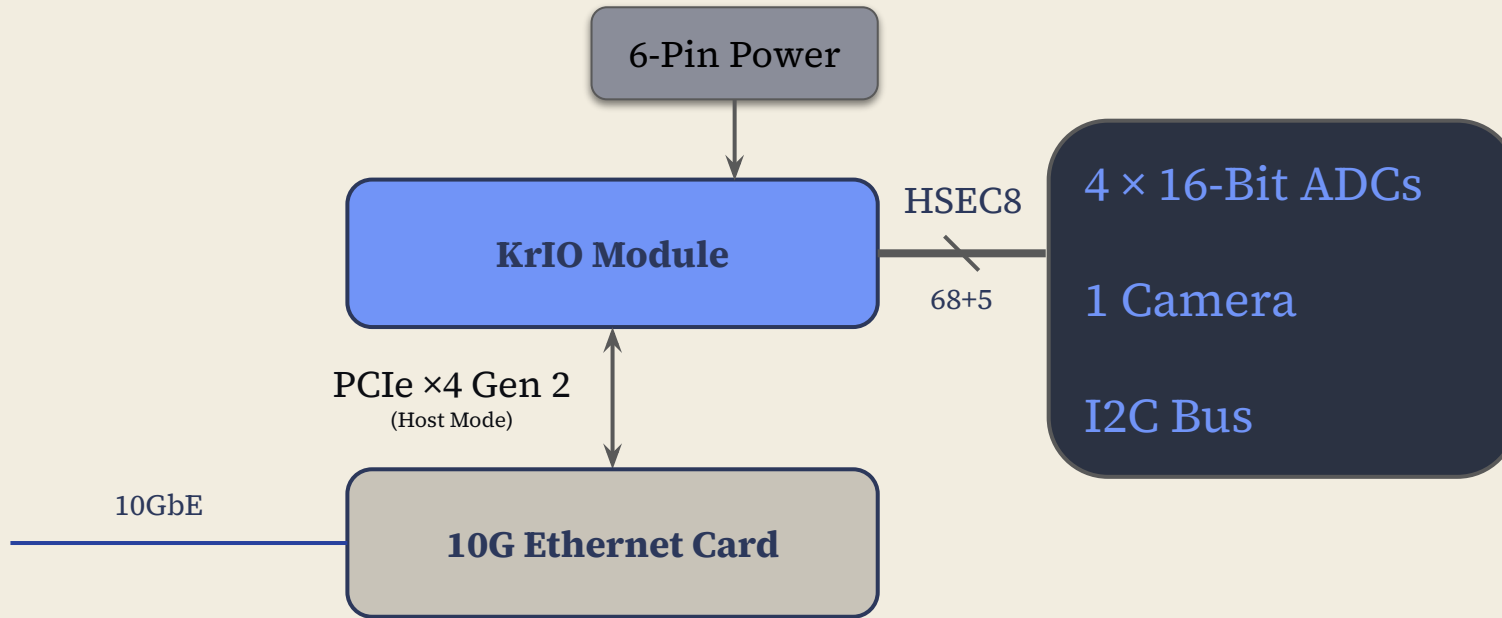
Example Frontend - LVDS/ECL TDC



Example Frontend - General Remote Experiment



Example Frontend - General Remote Experiment

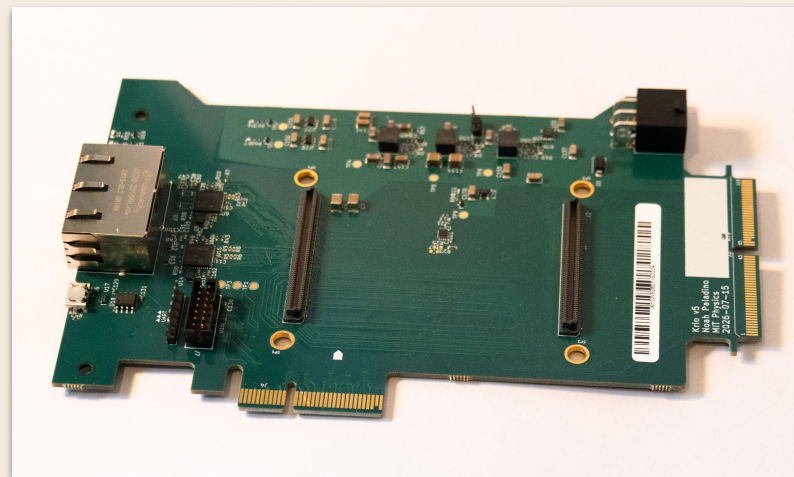




HLS4ML Support

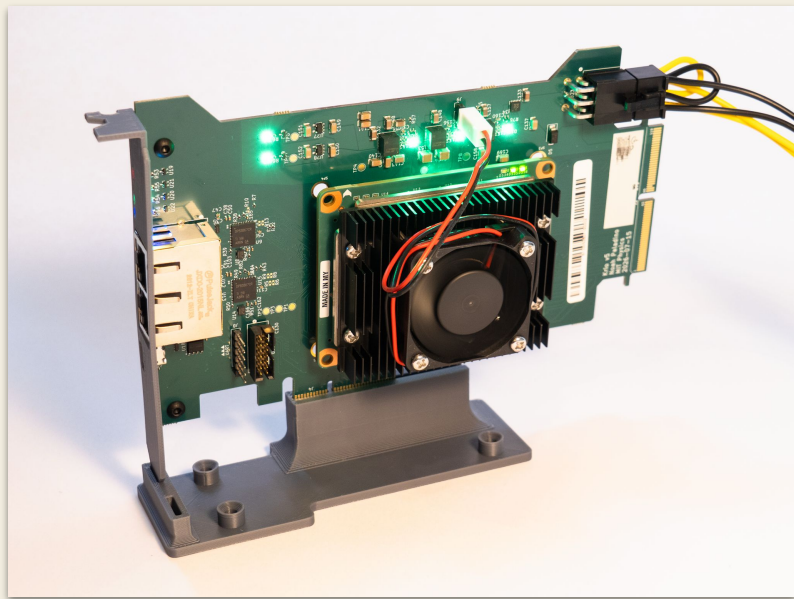
HLS4ML Support

- KrIO's flexibility offers an easy opportunity to integrate real-time ML
- Tested with a few sample models
 - Significantly accelerated deployment via Claude Code
 - ~1hr from model to running on hardware (including synthesis)



HLS4ML Benchmark Results

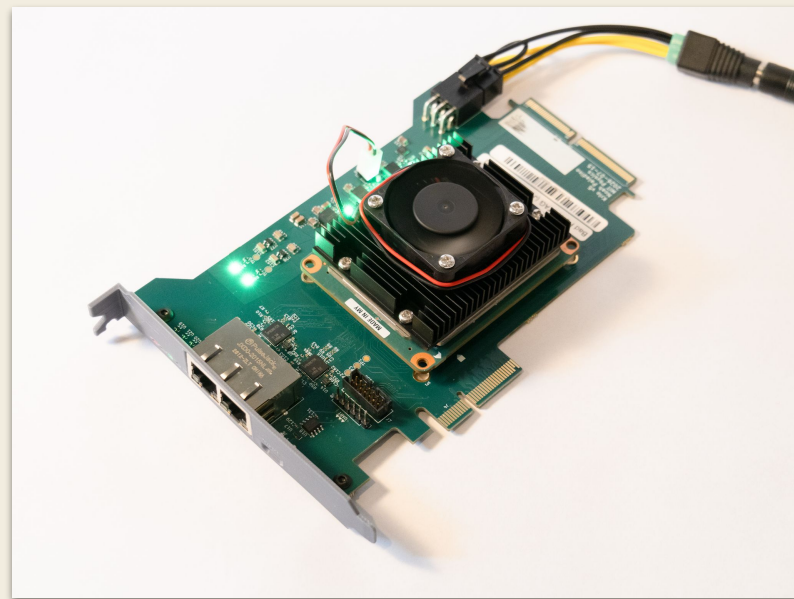
- 300k inferences/s in Jet-Tagging MLP over ethernet (AXI4-Lite, reuse factor 16)
 - With direct memory access and distributed arithmetic, we can achieve up to 42.6M (max ethernet capacity ~6M)
- 929 μ s / image MLPerf Tiny ResNet-8 classifying CIFAR-10 (AXI4-Lite, variable reuse factors)
 - Still room for optimization
- ~0.4s model swap time



Summary

Summary

- KrIO offers an open-source module for experiment data acquisition
- Gives scalable high-throughput data acquisition at a modest cost
- Provides a standardized platform for real-time AI in science via HLS4ML





Thank You!