



Simulation of 4D Fabric: a NIFTY-fied Pixel ROC

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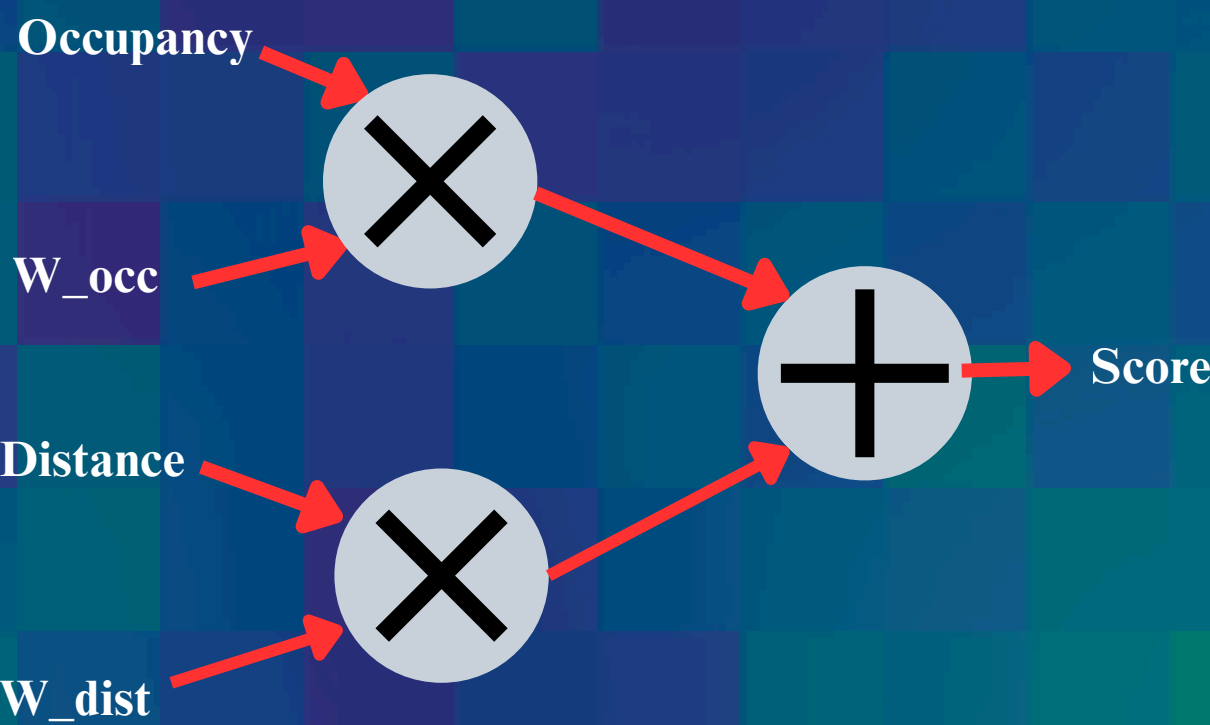


Motivation

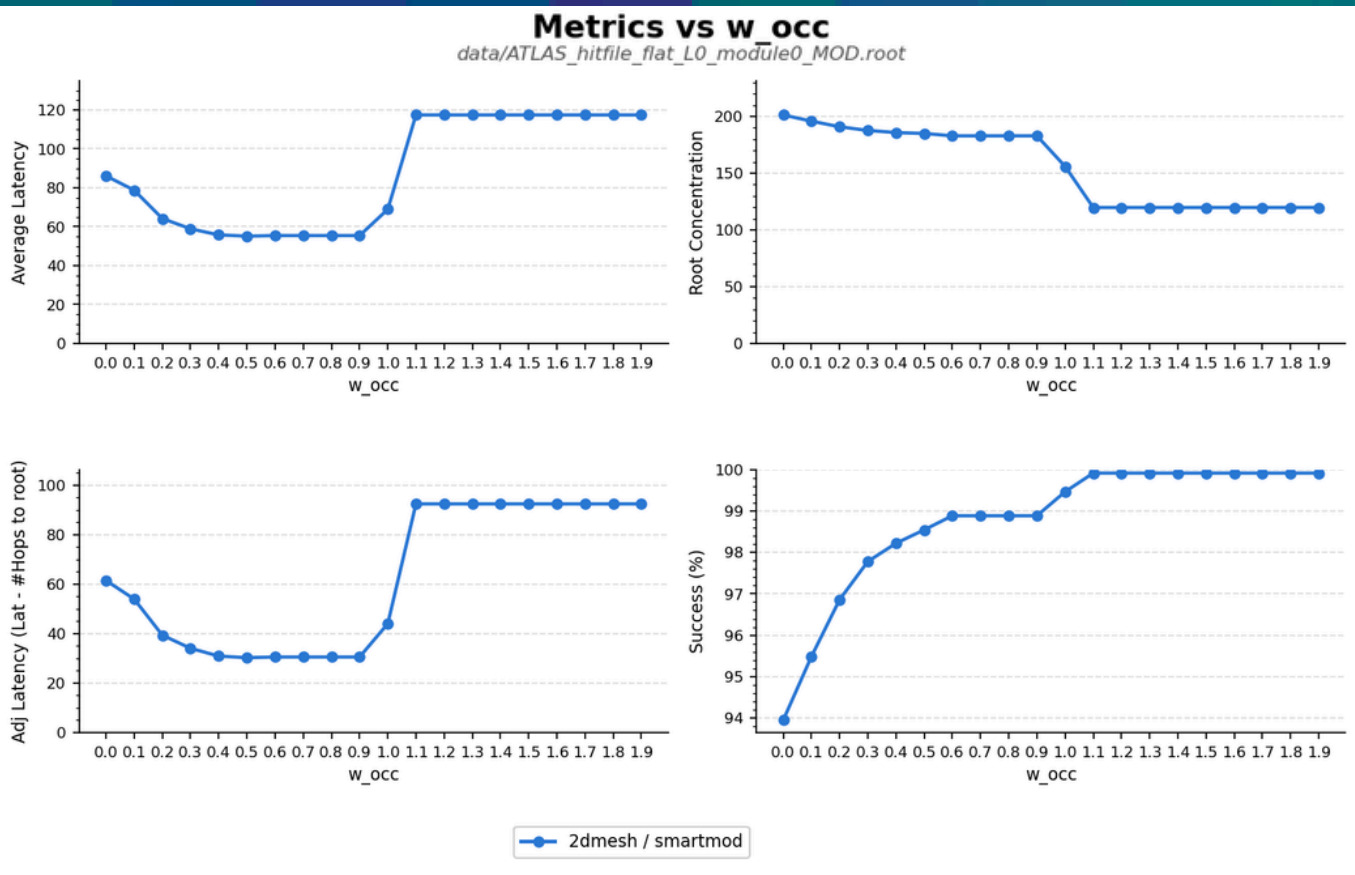
- Current readout chips (RD53) are prone to failures
- Single node failures or congestion can cause large quantities of data loss
- Next gen readout chips should allow for smarter routing of data and detection of issues

Routers

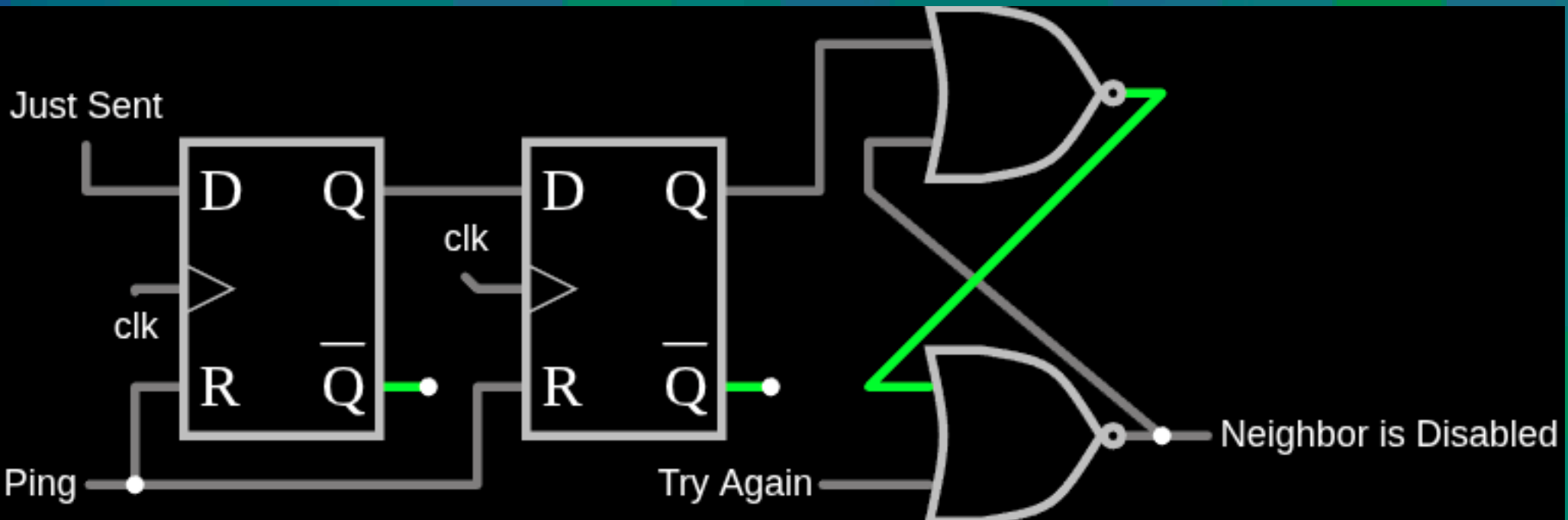
- Tested to find if weighting neighbor distance and occupancy help
- Found no significant change to stats showing that weights wouldn't be worth cost of silicon implementation



Router Results



Failure Detection



- We were able to test methods of failure detection in the sim
- We found a simplistic method that can catch failed nodes
- A node will count how long it takes for a neighbor to send data
- If neighbor hasn't sent the nodes data after N cycles, the node marks it as disabled

Simulator

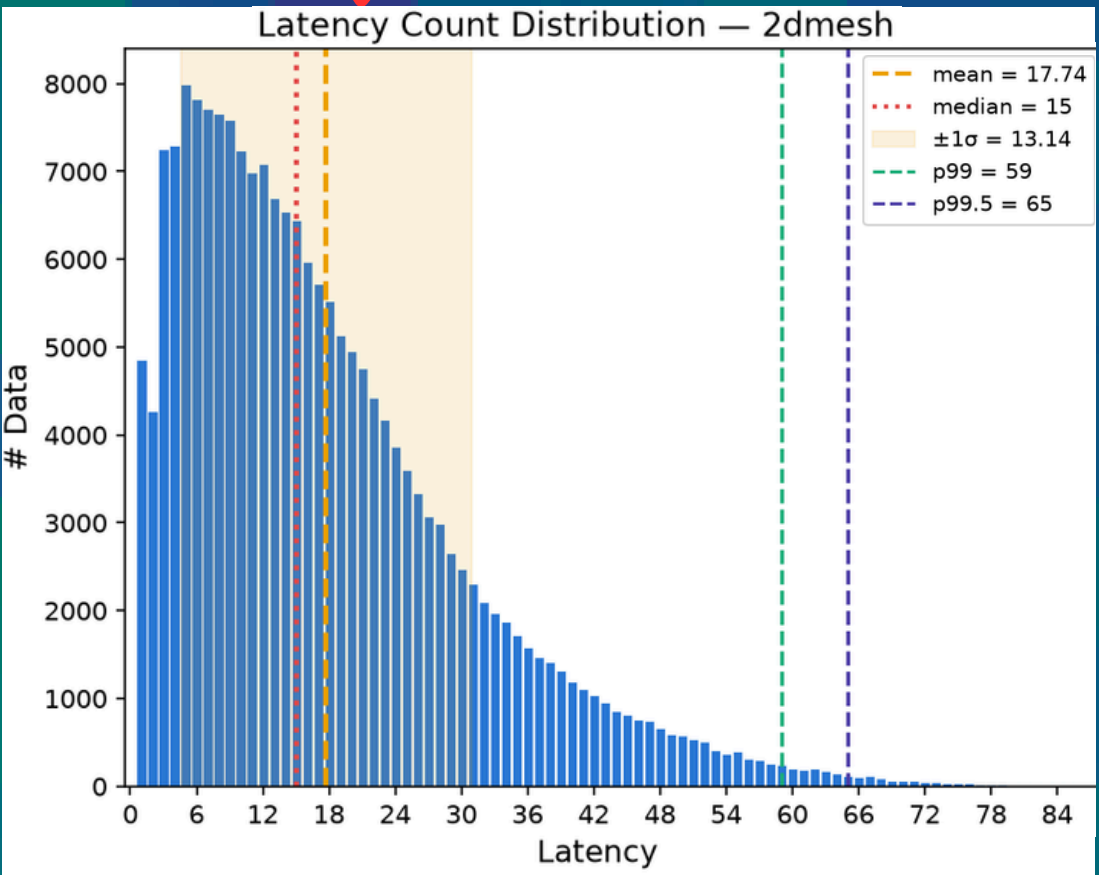
- Our custom simulator written in C++ allows for testing various chip designs before we implement them in silicon
- We tested topologies, routers, error detection, and more

Highly accurate simulated data injected into nodal system

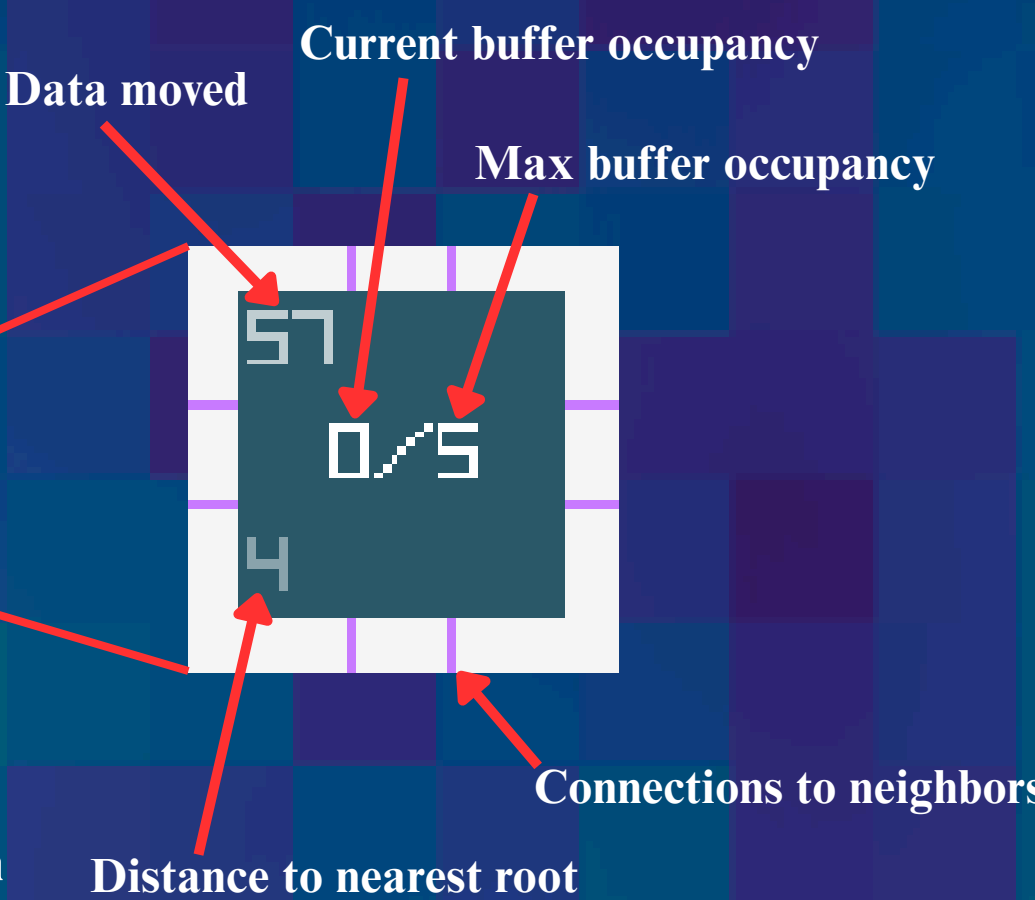


Data flows down to the bottom of the chip

The success rate and latency of data that reaches the bottom of the chip is used to compare the various chip designs



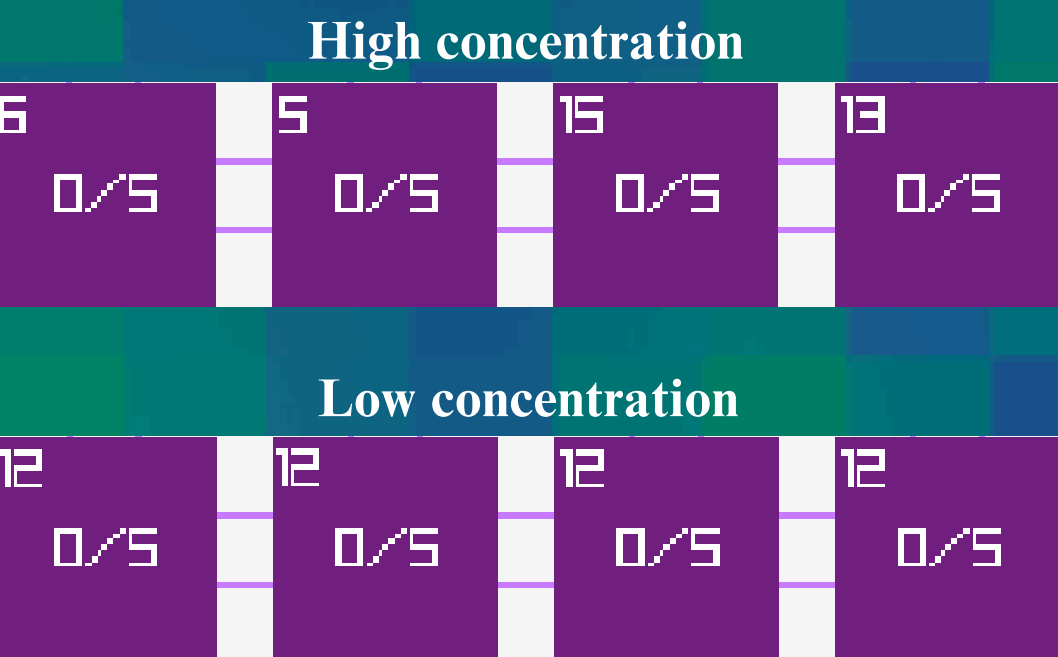
Latency is measured in number of cycles not spent actively moving towards destination



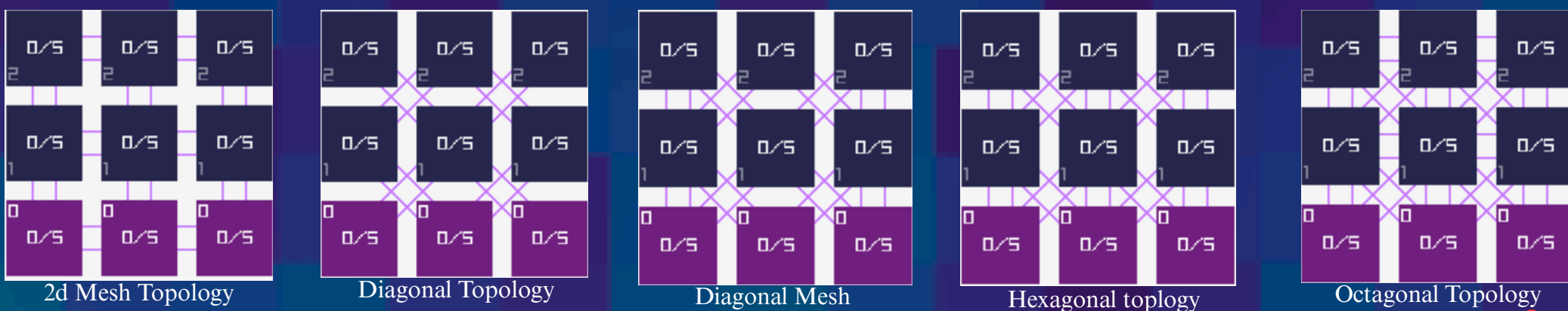
Nodes decide where to send data based on how far a neighbor is from destination and how full a neighbor's buffer is

- Root nodes route data out of the network into the end of column network
- They represent the destination for packets in the system

- Root concentration is a metric that measures how evenly used the root nodes are
- The lower the better

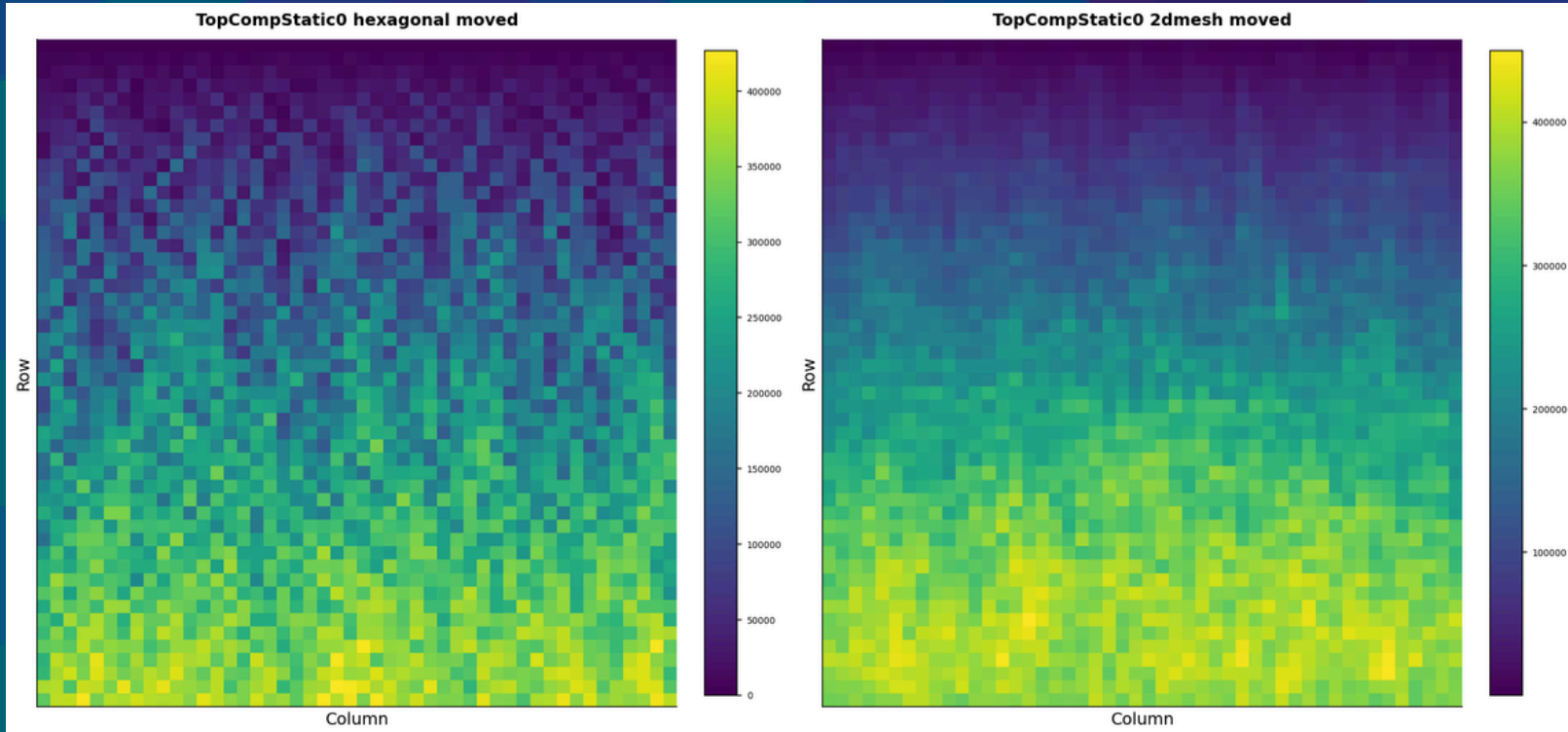


Topologies



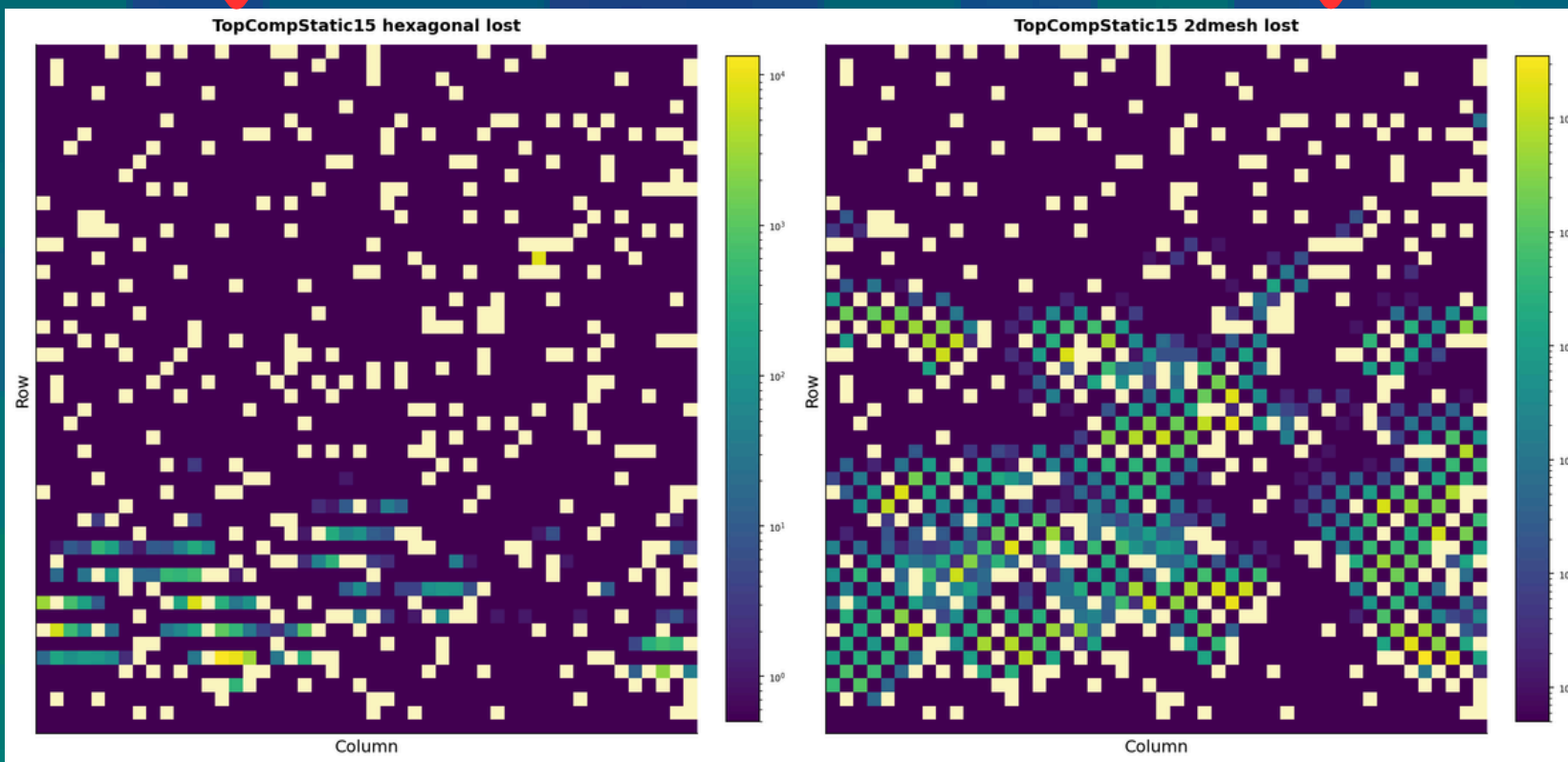
Increasing complexity

Different topologies, different movements

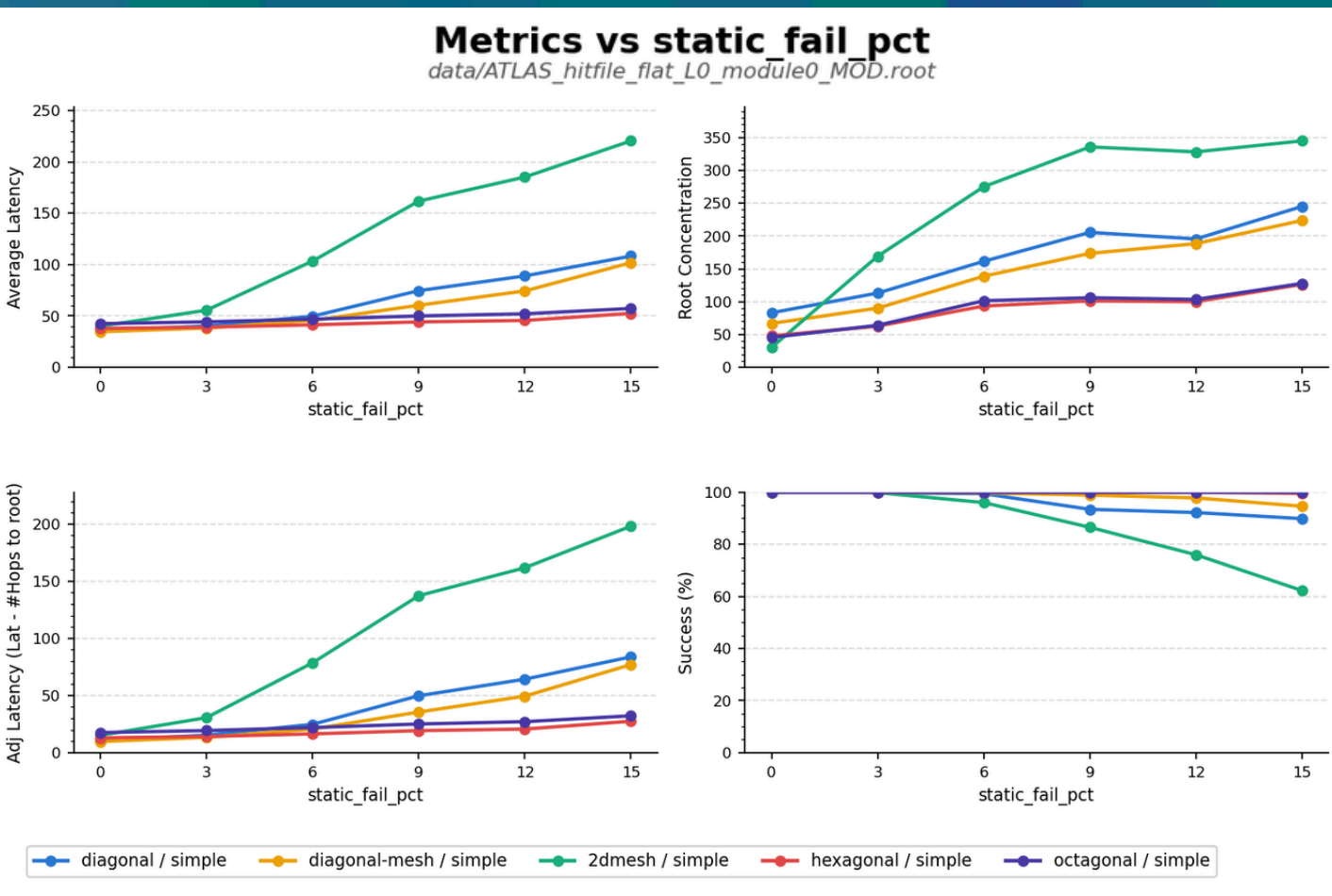


Adding static failures (beige squares) helps us evaluate different topologies

Different losses



Topology Results



- Testing shows that diagonal topologies handle static failures much better than the typical 2d mesh topology
- 2d mesh spreads data more evenly in low failure conditions