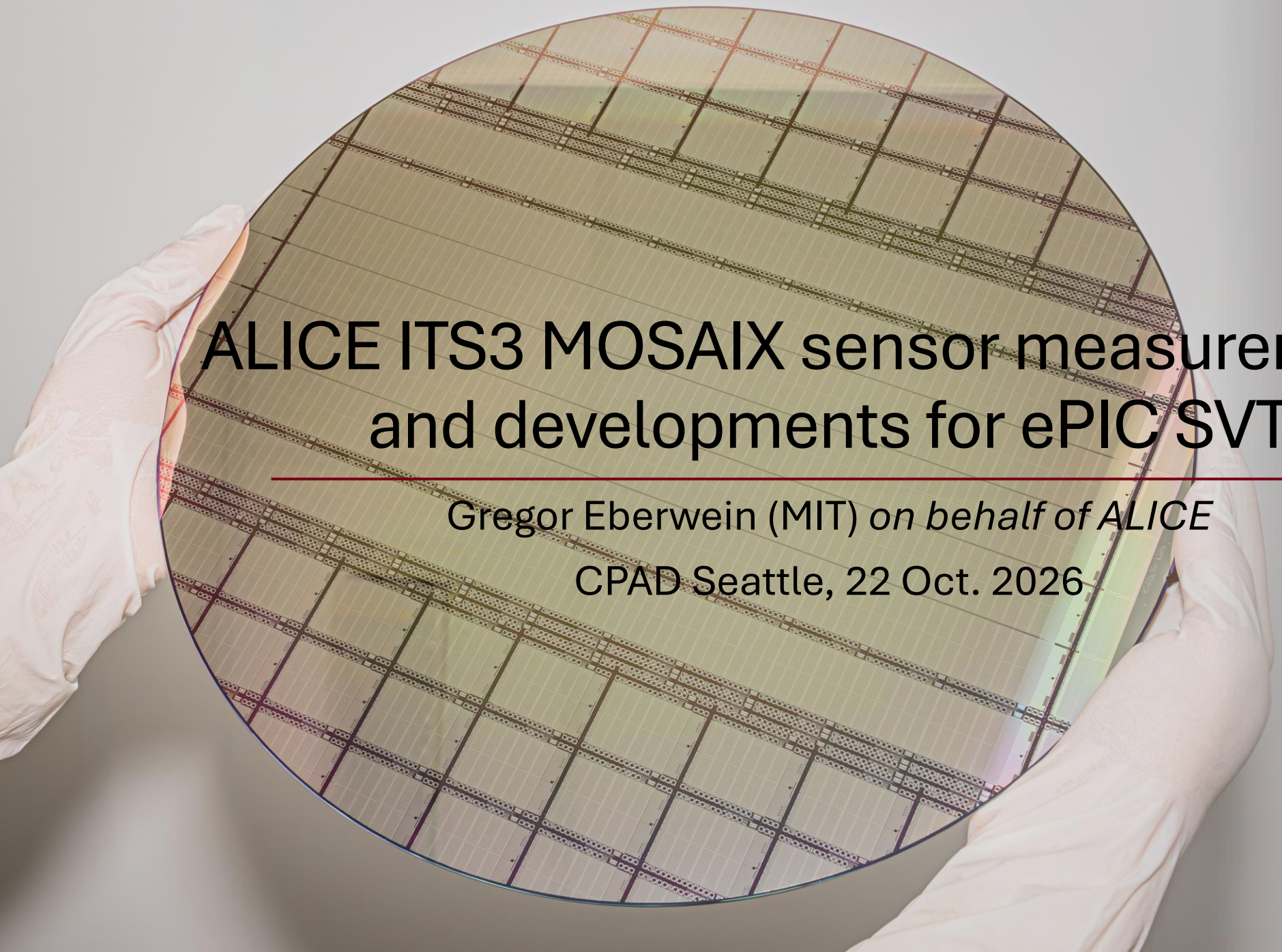


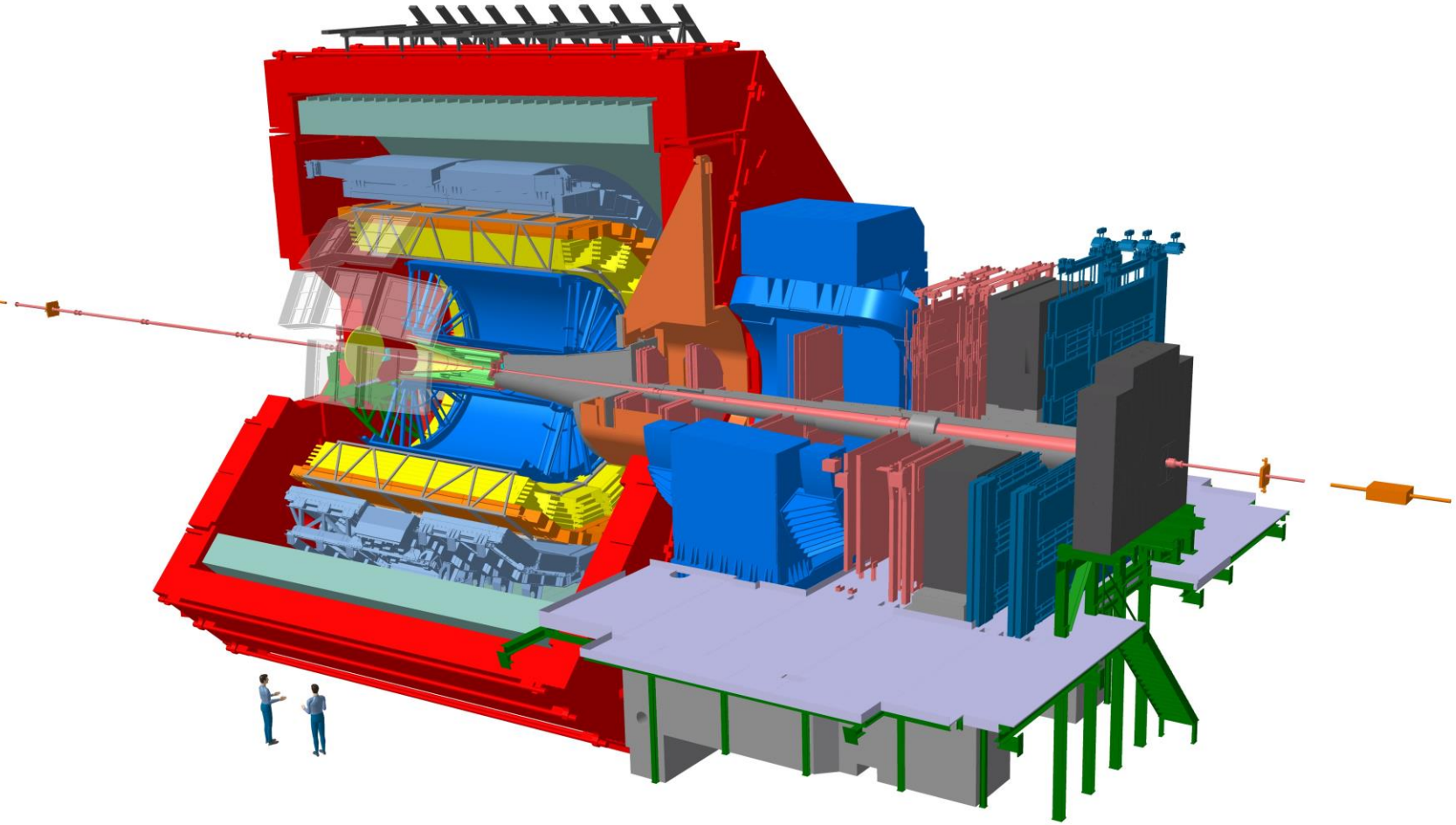
ALICE ITS3 MOSAIX sensor measurements and developments for ePIC SVT

Gregor Eberwein (MIT) *on behalf of ALICE*

CPAD Seattle, 22 Oct. 2026

The work of the MIT HI group and MIT PixElφ Lab was supported by US DOE-NP and by the SVT-EIC project

ALICE – A Large Ion Collider Experiment



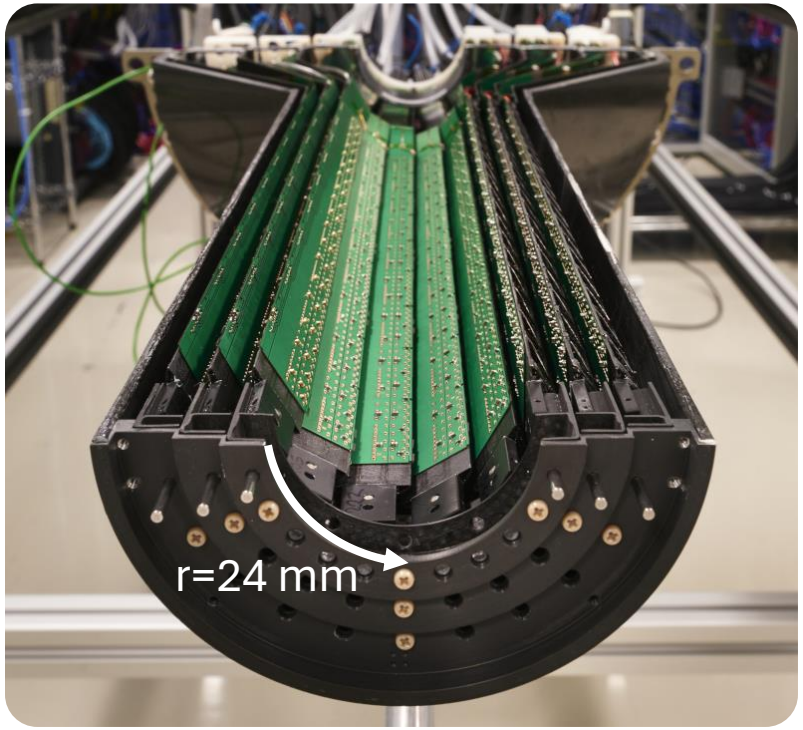
Study of strongly interacting matter at extreme densities (QGP) in heavy-ion collisions at the LHC (CERN)

Low momentum ($\lesssim 1$ GeV/c) particle reconstruction

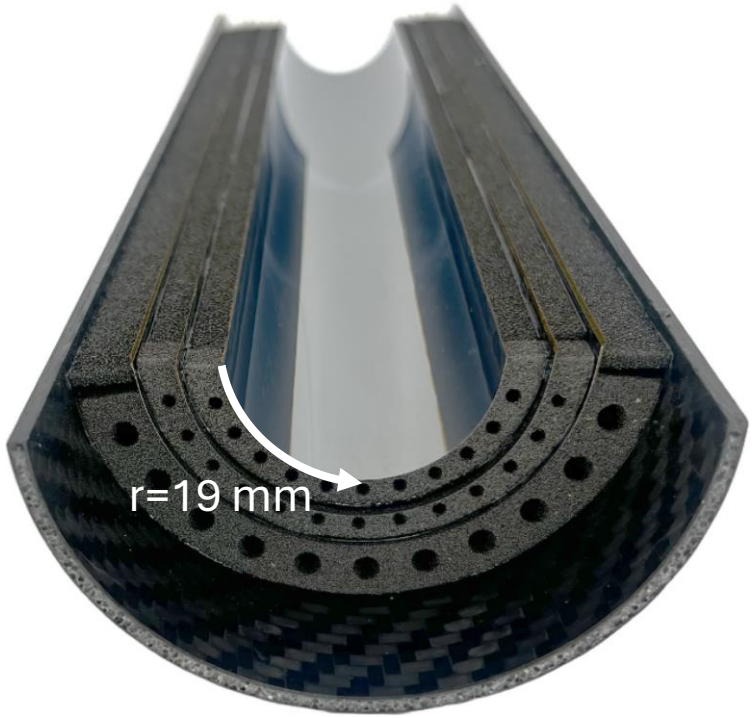
- New inner tracker for Run 4 (2030)

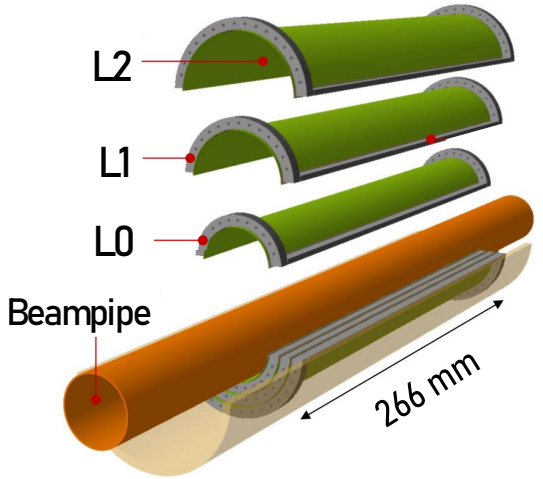
ALICE Inner Tracking System 3 (ITS3)

ITS2 half-barrel – currently installed



ITS3 half-barrel – engineering model

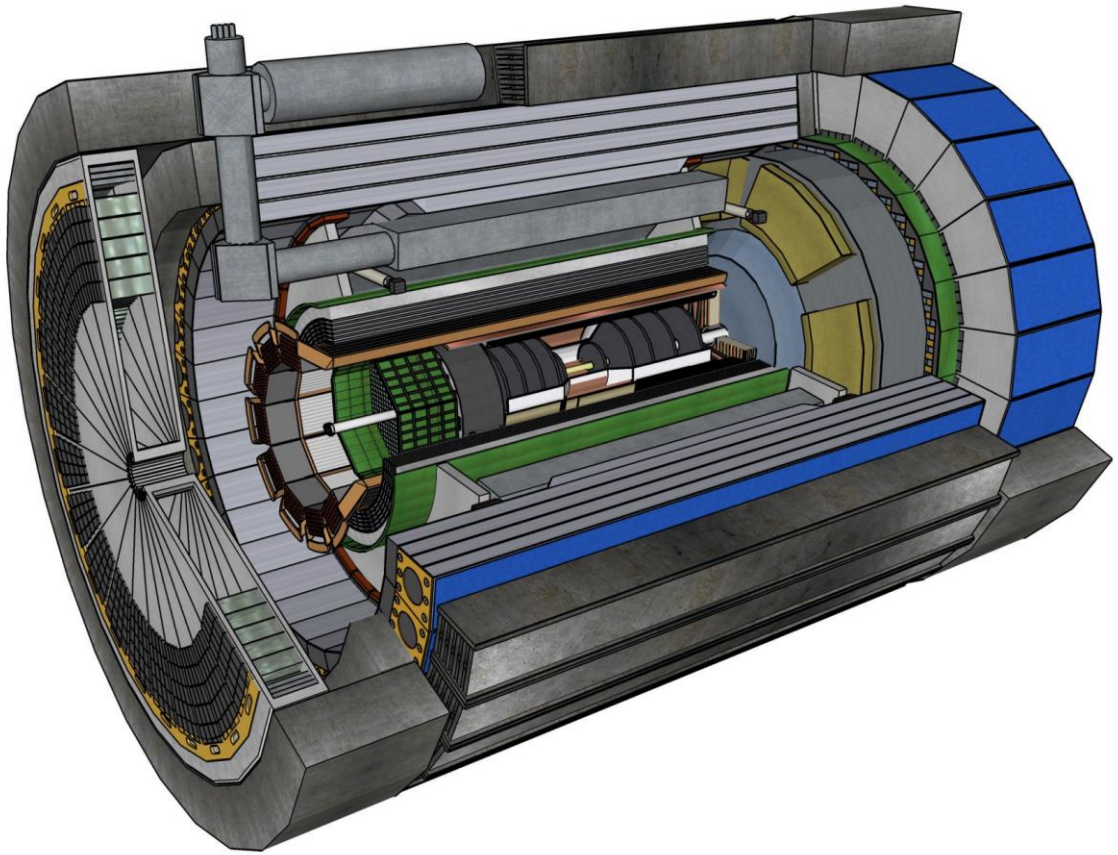




Improved low p_T physics performance – low material budget, air cooling, small inner radius

→ bent, wafer-scale monolithic active pixel sensors (MAPS) – in total just 6 sensors for entire inner barrel

ePIC – electron-Proton and Ion Collider

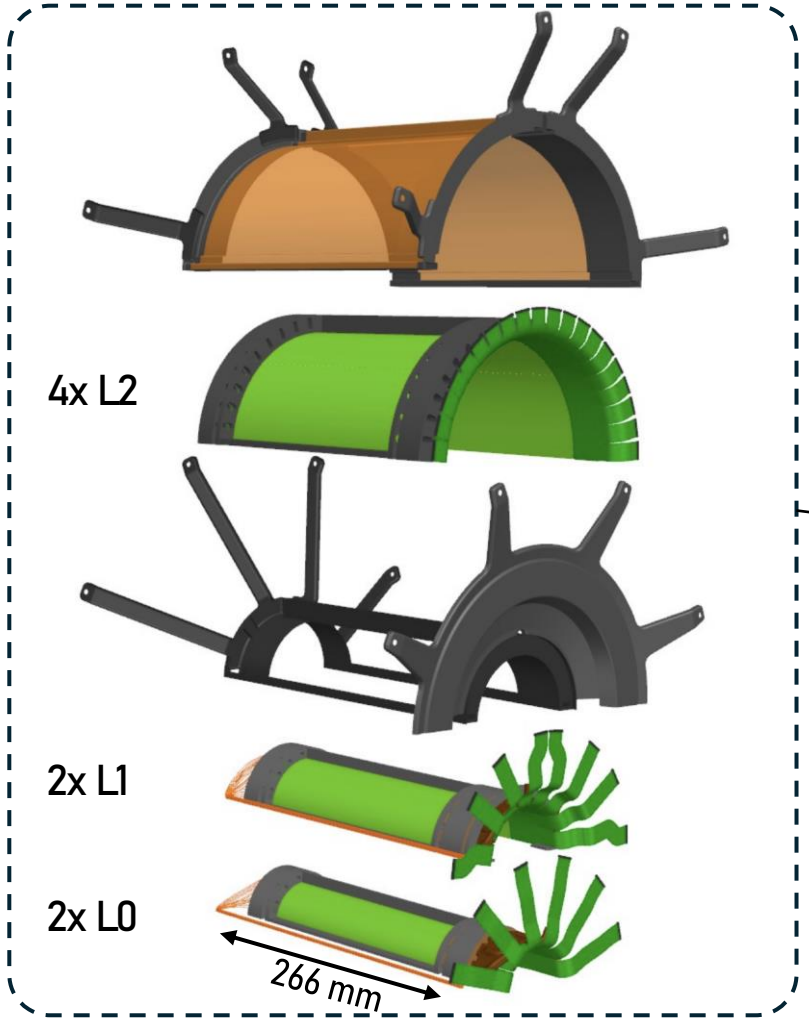


Study of strongly interacting matter in electron-ion collisions at the future Electron-Ion Collider (EIC) at BNL

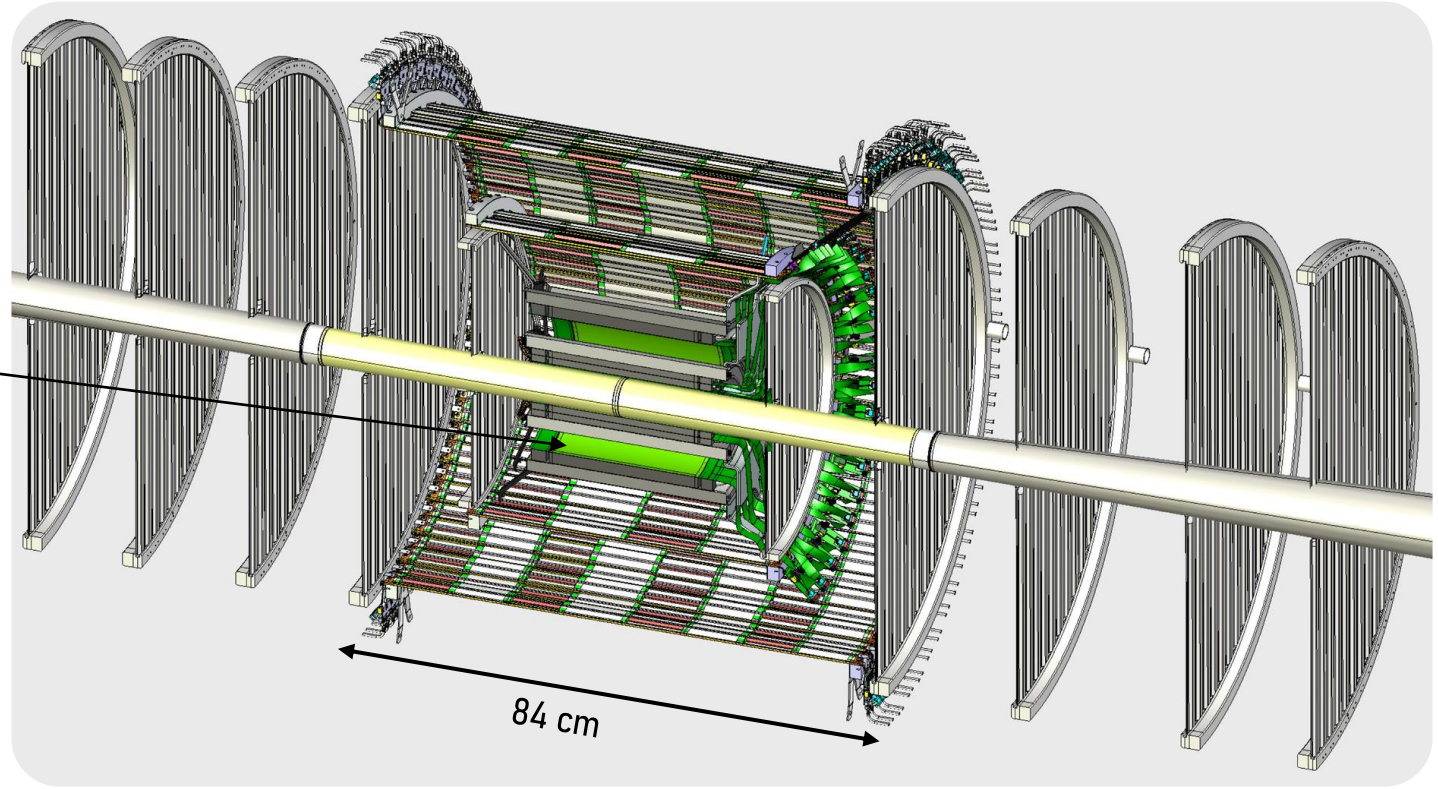
Low mass detectors with high spatial resolution tracking essential (e.g. scattered e^- measurements)

- Tracker installation in 2032

ePIC Silicon Vertex Tracker (SVT)

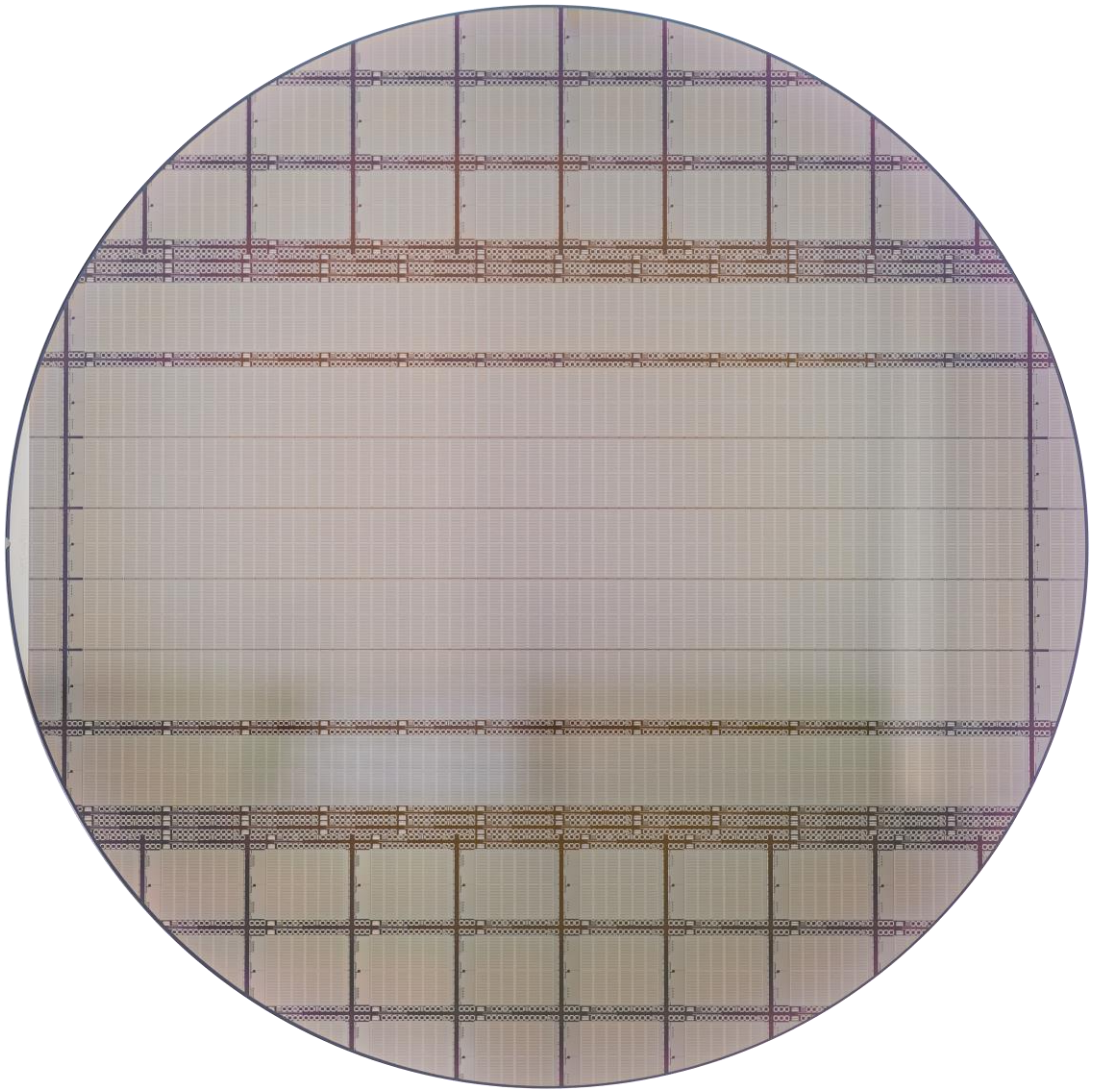


Inner barrel - based on
bent, wafer-scale MAPS



Outer tracker - based on large-area MAPS of same type
Total ~8.5 m^2 of silicon

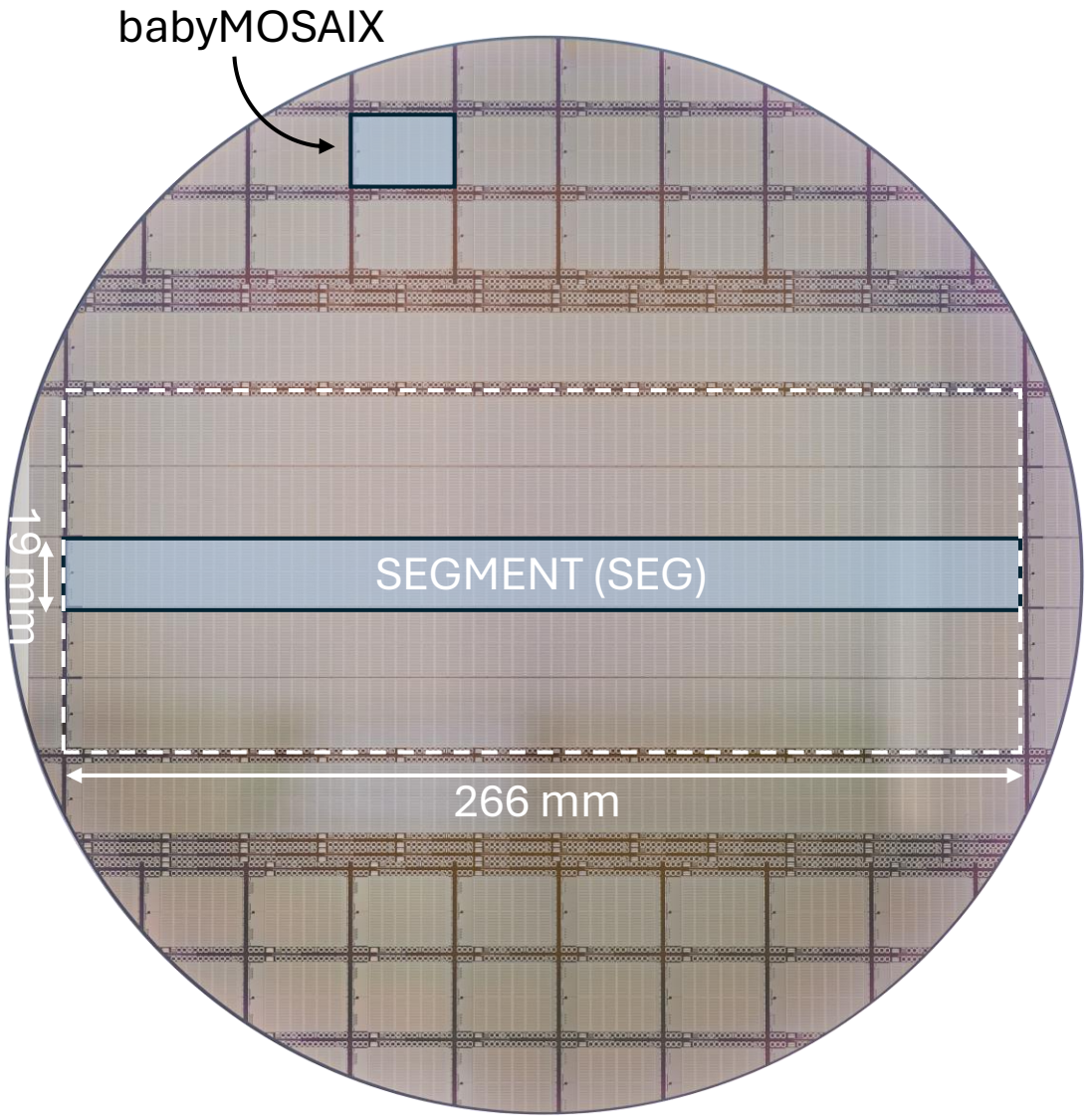
MOSAIX



∅ 300 mm (12 in)

ER2 run: 65nm, stitched, wafer-scale, CMOS, MAPS

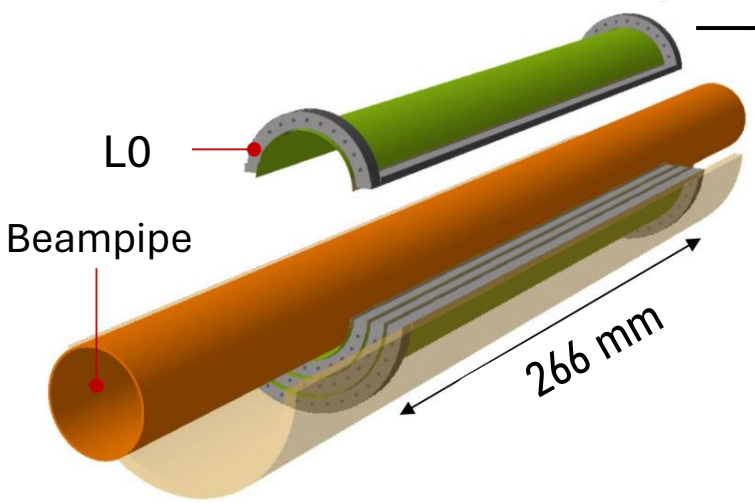
MOSAIX

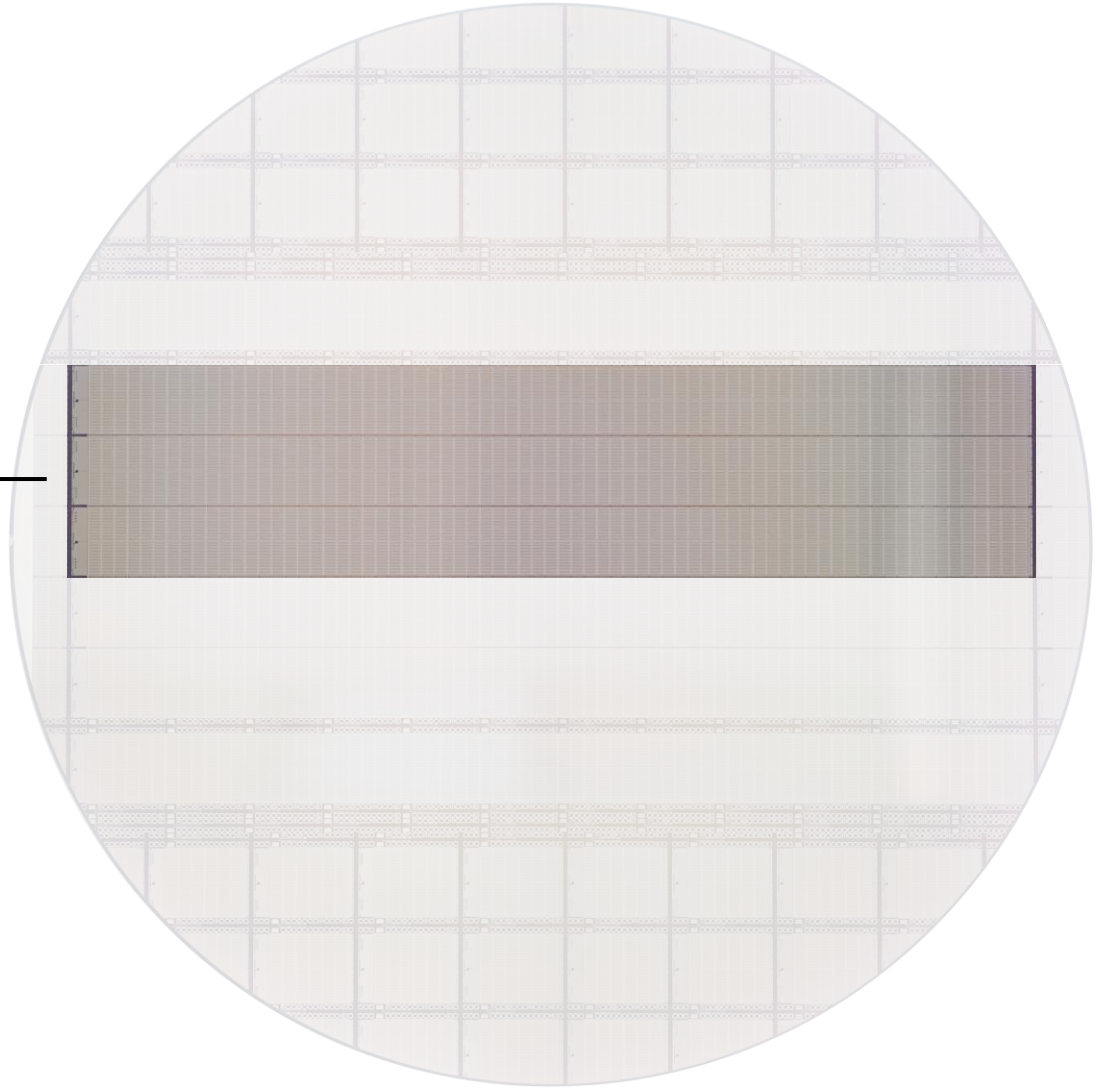


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ER2 run: 65nm, stitched, wafer-scale, CMOS, MAPS

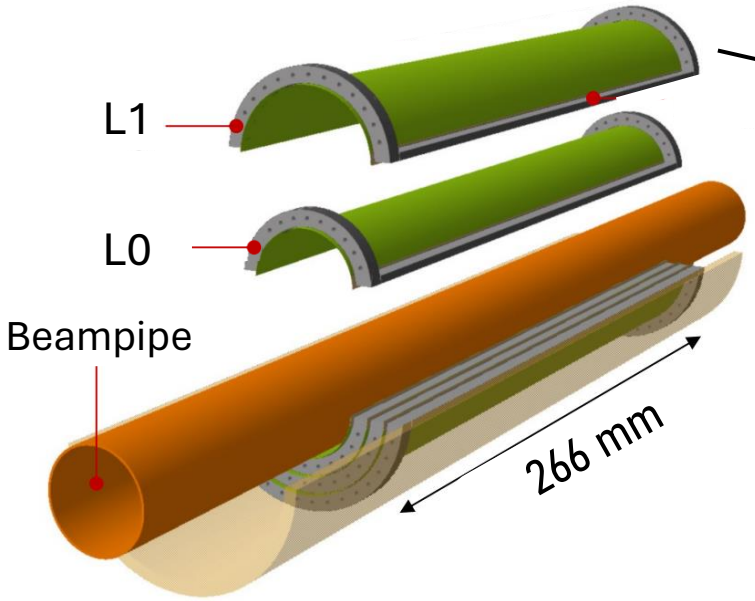
MOSAIX

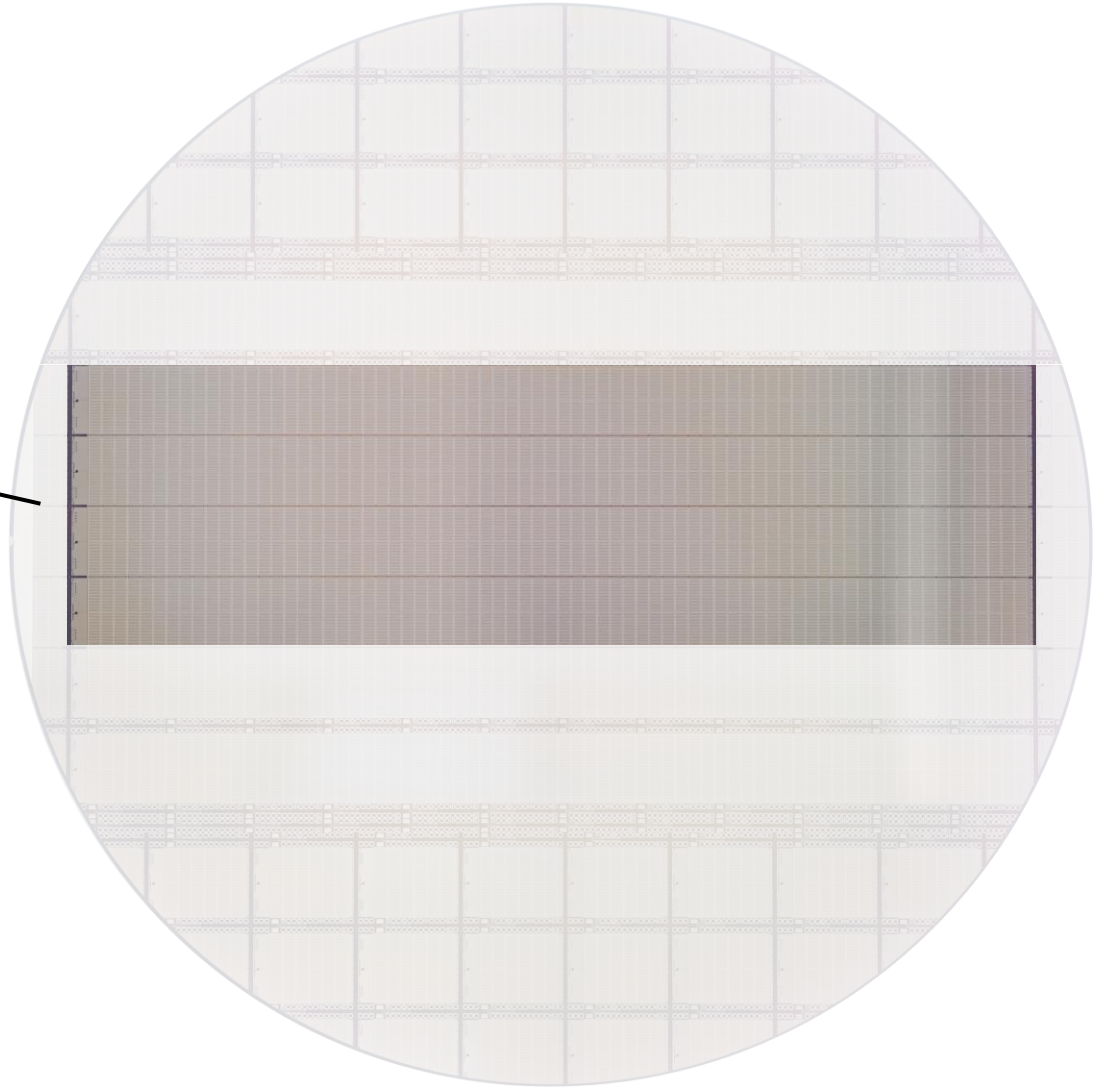




⌀ 300 mm (12 in)

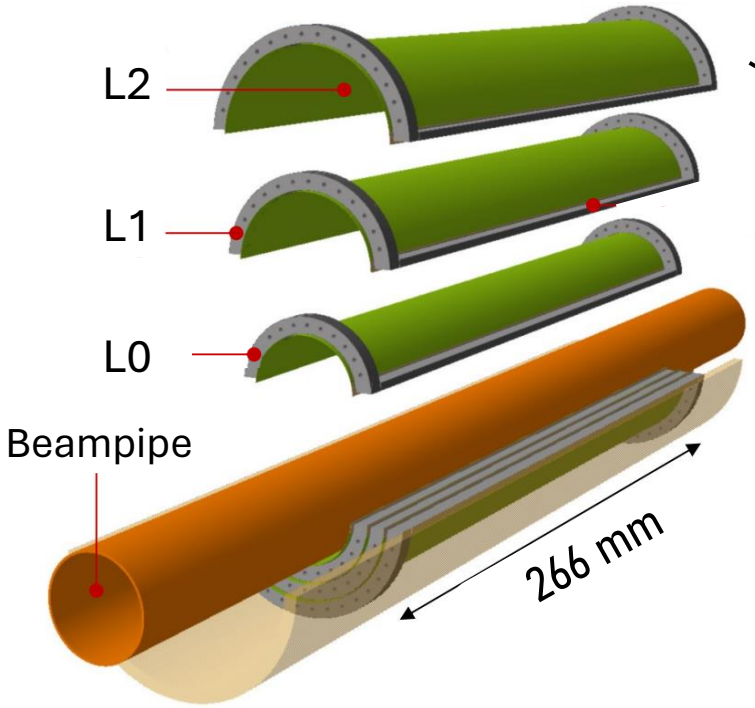
MOSAIX

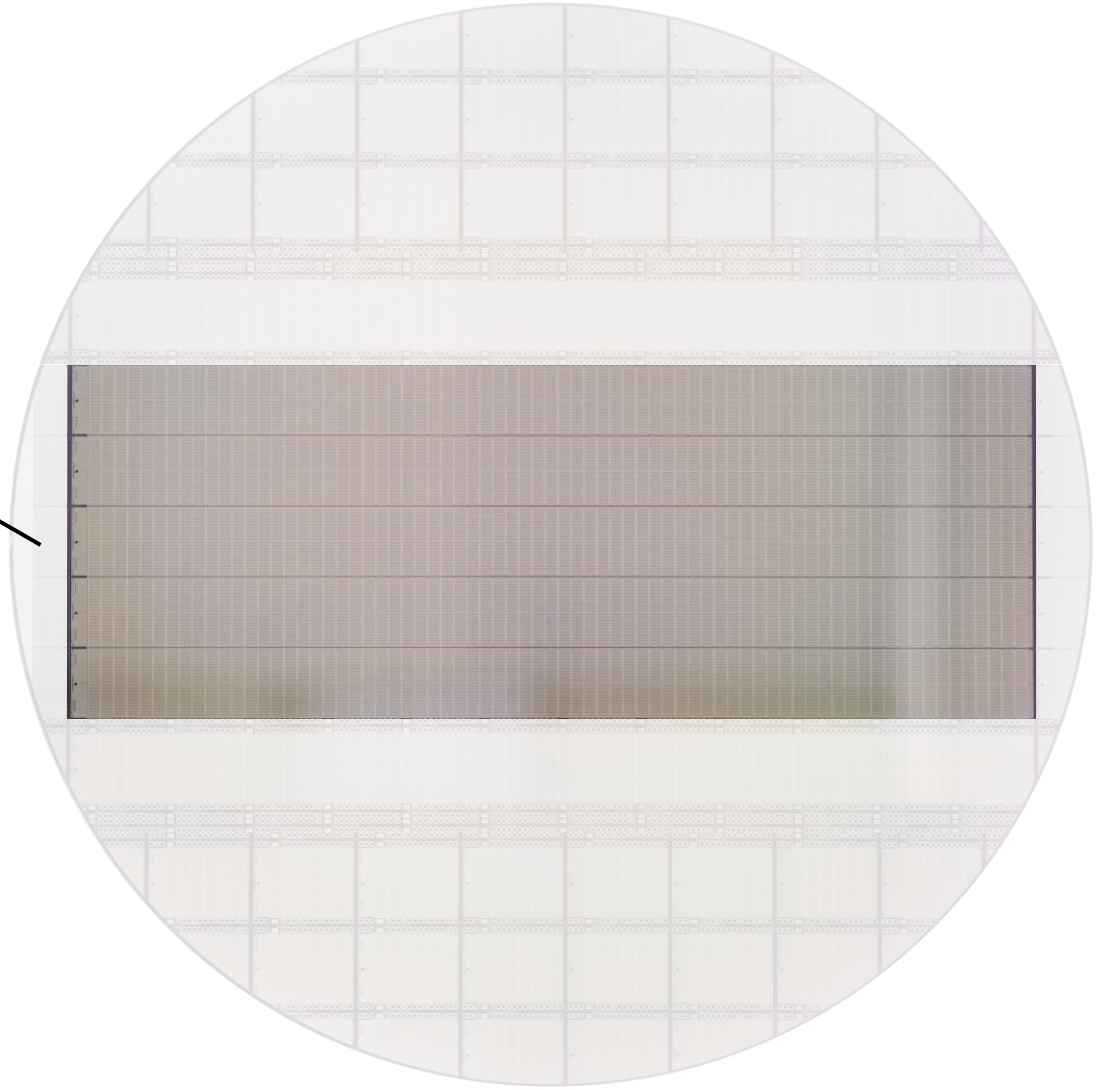




∅ 300 mm (12 in)

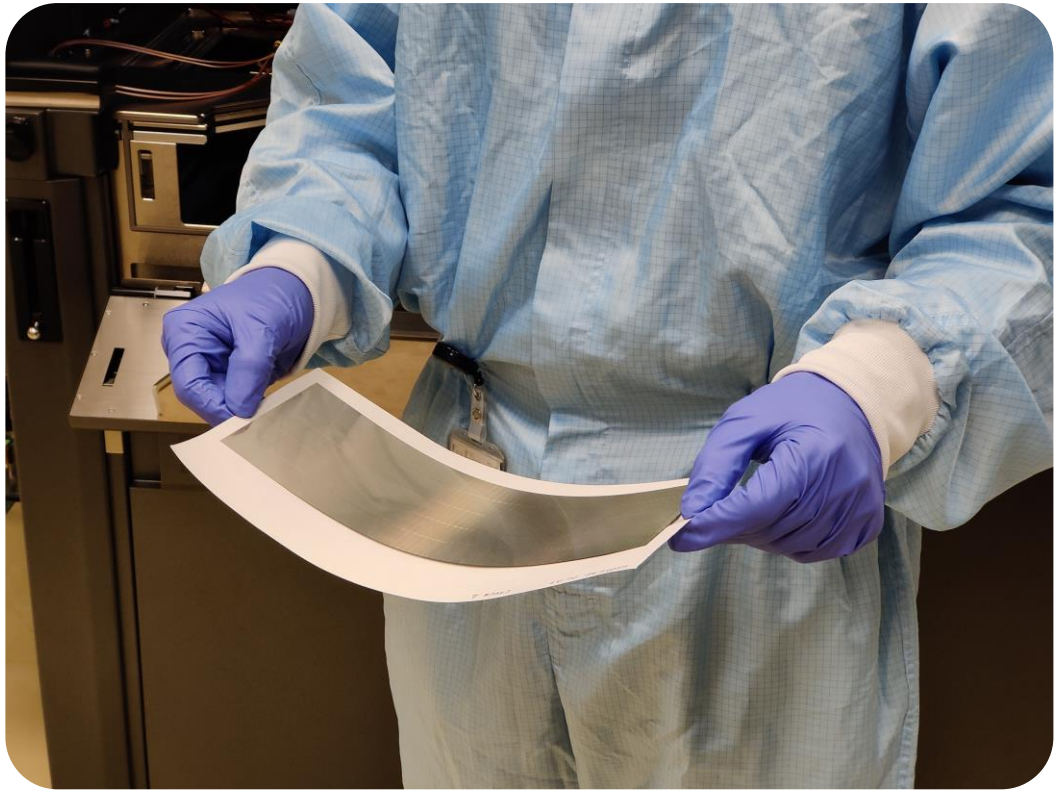
MOSAIX



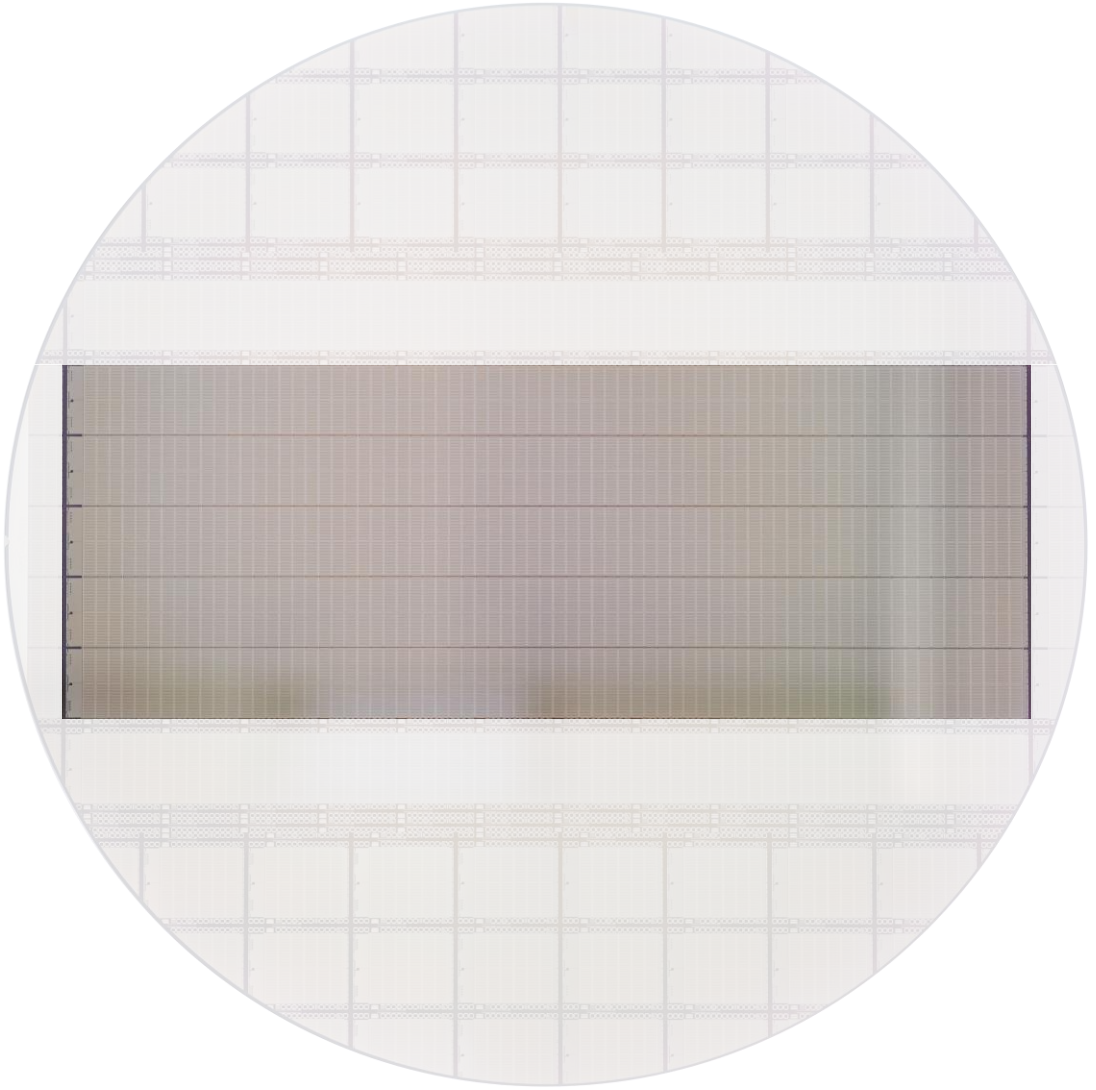


∅ 300 mm (12 in)

MOSAIX



flexible when thinned to <50 µm !

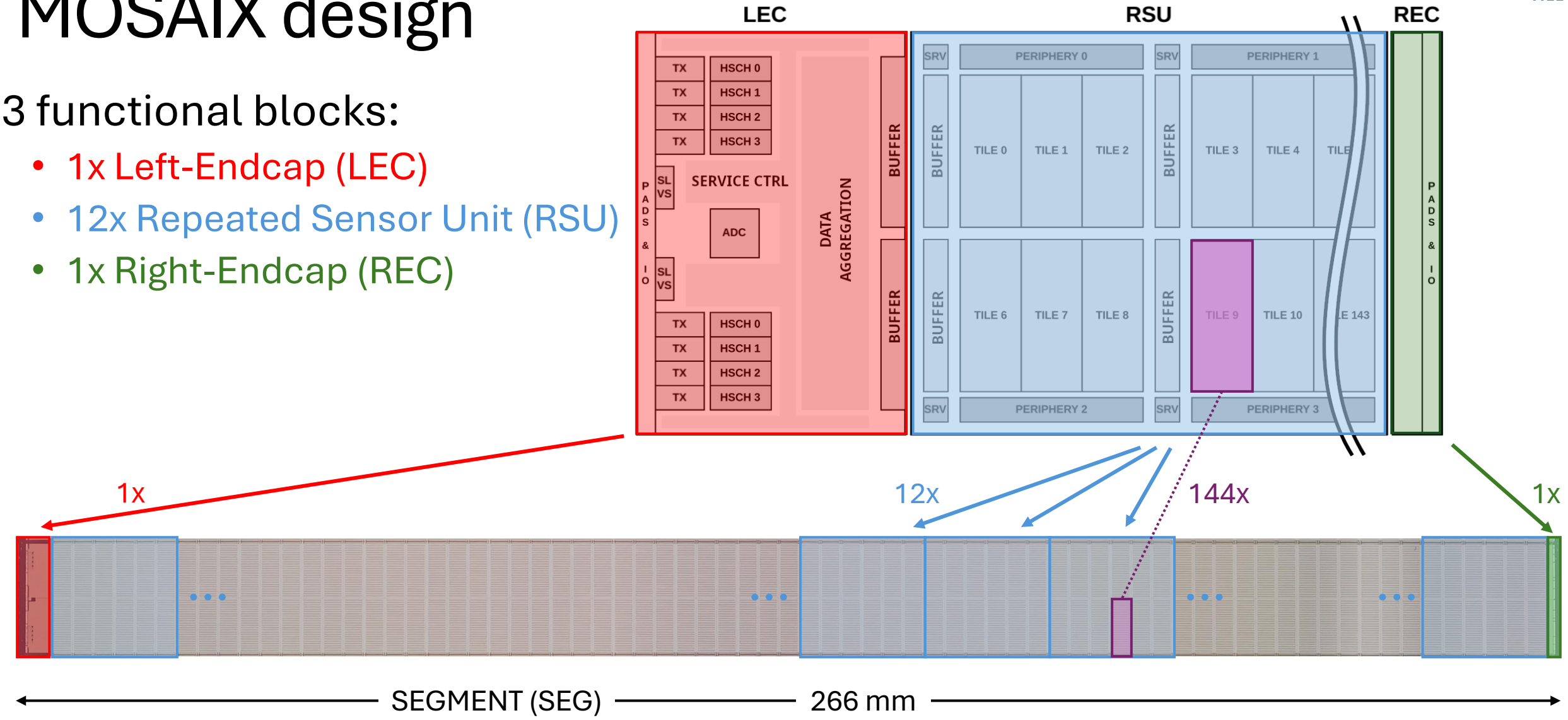


⌀ 300 mm (12 in)

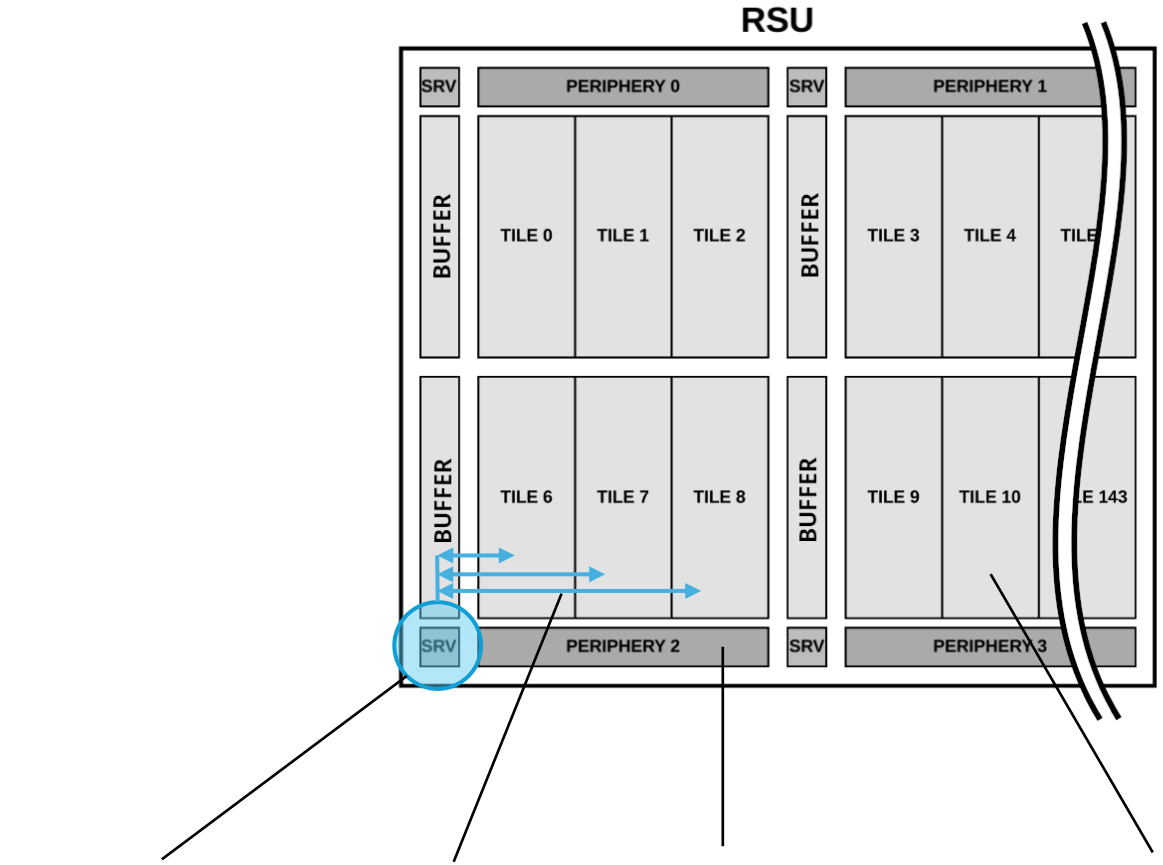
MOSAIX design

3 functional blocks:

- 1x Left-Endcap (LEC)
- 12x Repeated Sensor Unit (RSU)
- 1x Right-Endcap (REC)



MOSAIX design



- 12 independent tiles per RSU
- Each tile is switched (service node)

- Overall: 12 RSUs x 12 tiles = **144 tiles**
- 144 x 160 Mb/s transmission
- 144 biasing/periphery blocks
- 288 local power domains

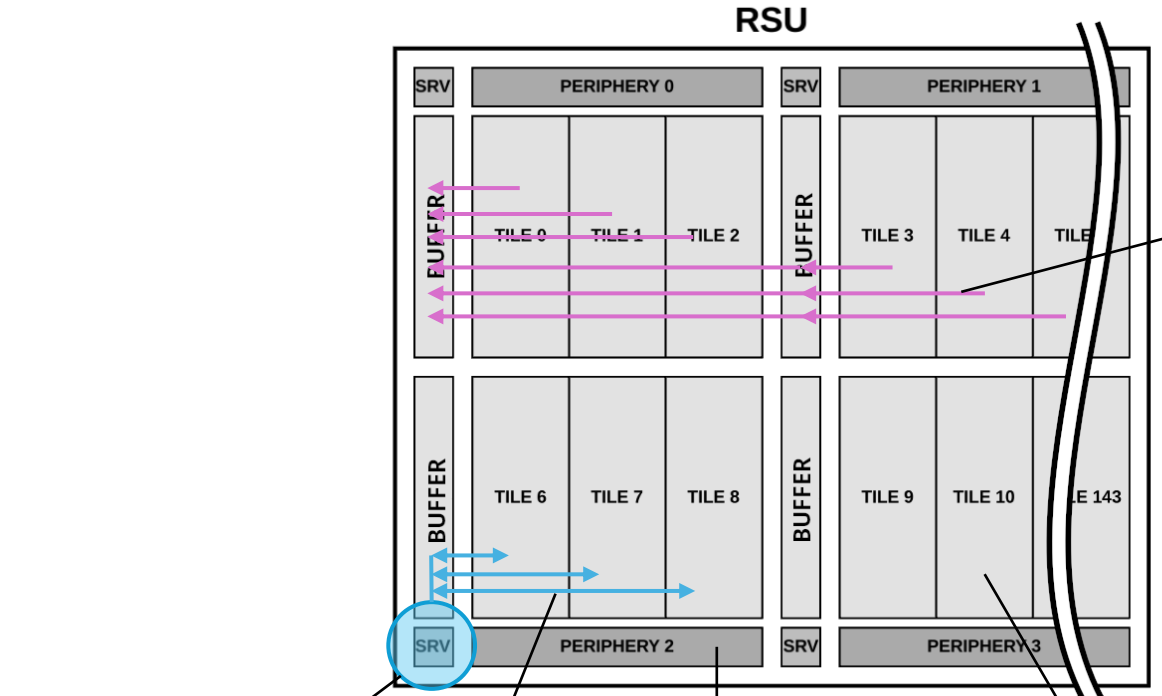
Service Node

Clk & ctrl

Biasing/periphery blocks for each tile

444 × 156 pixels/tile
20.8 x 22.8 μm^2 pixels
~ 10 Mpx/SEGMENT

MOSAIX design



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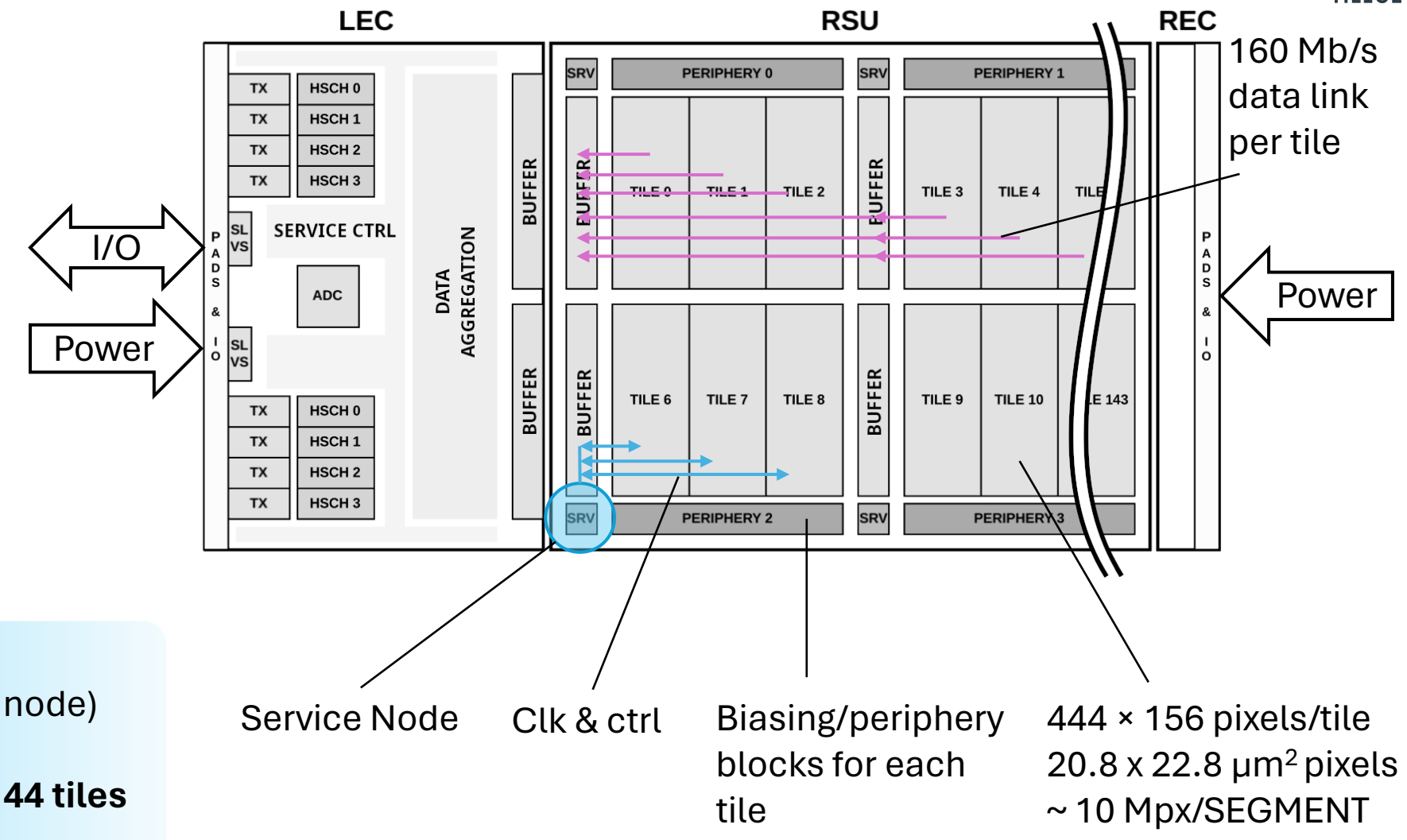
12x

MOSAIX design

- 8 x 10 Gb/s transmitter with lpGBT logic encoded
- 4 x global power domains +TX domain
- Analog monitoring ADC
- 2 slow control endpoints
- CLK, SYNC, RST

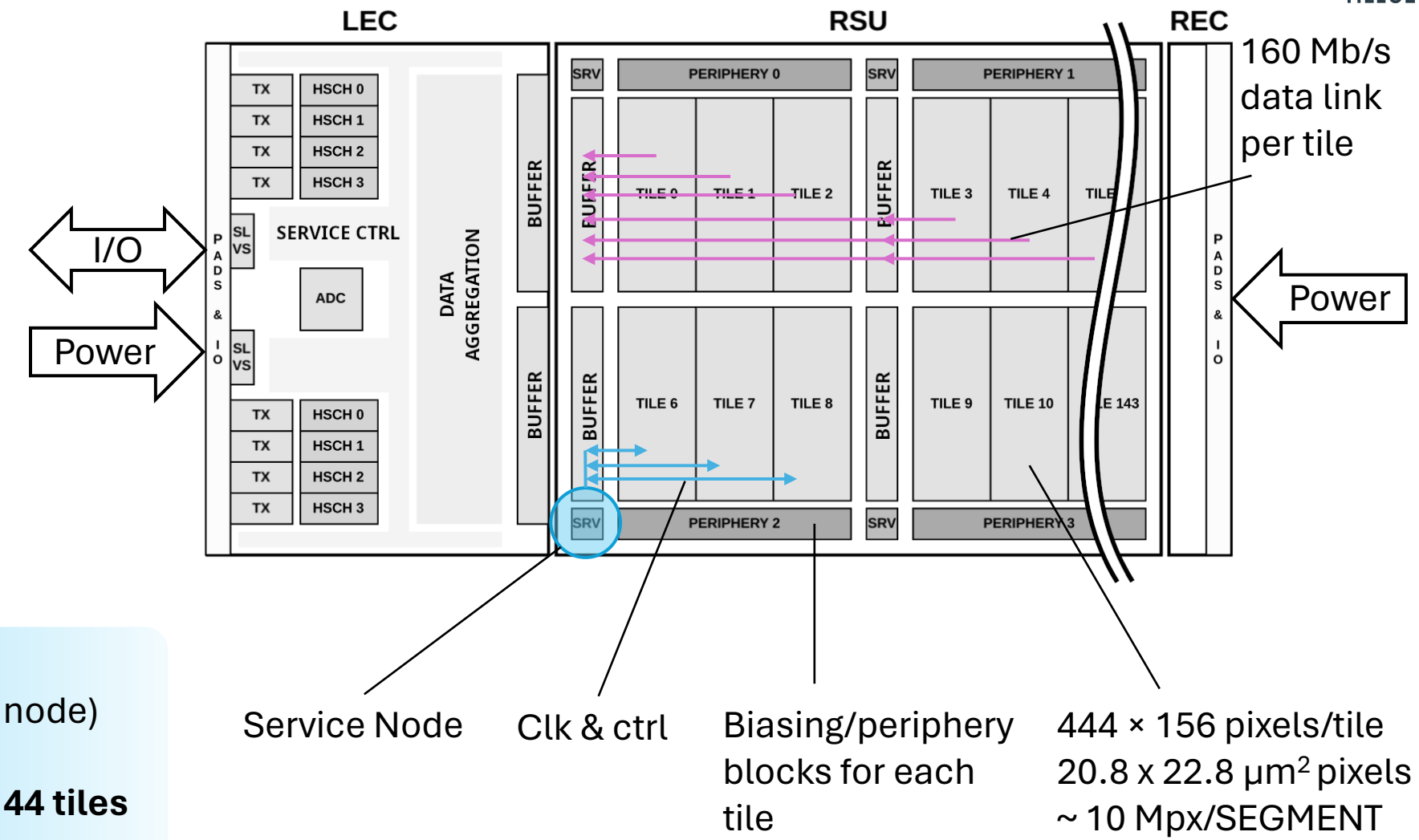
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MOSAIX design

- 8 x 10 Gb/s transmitter with lpGBT logic encoded
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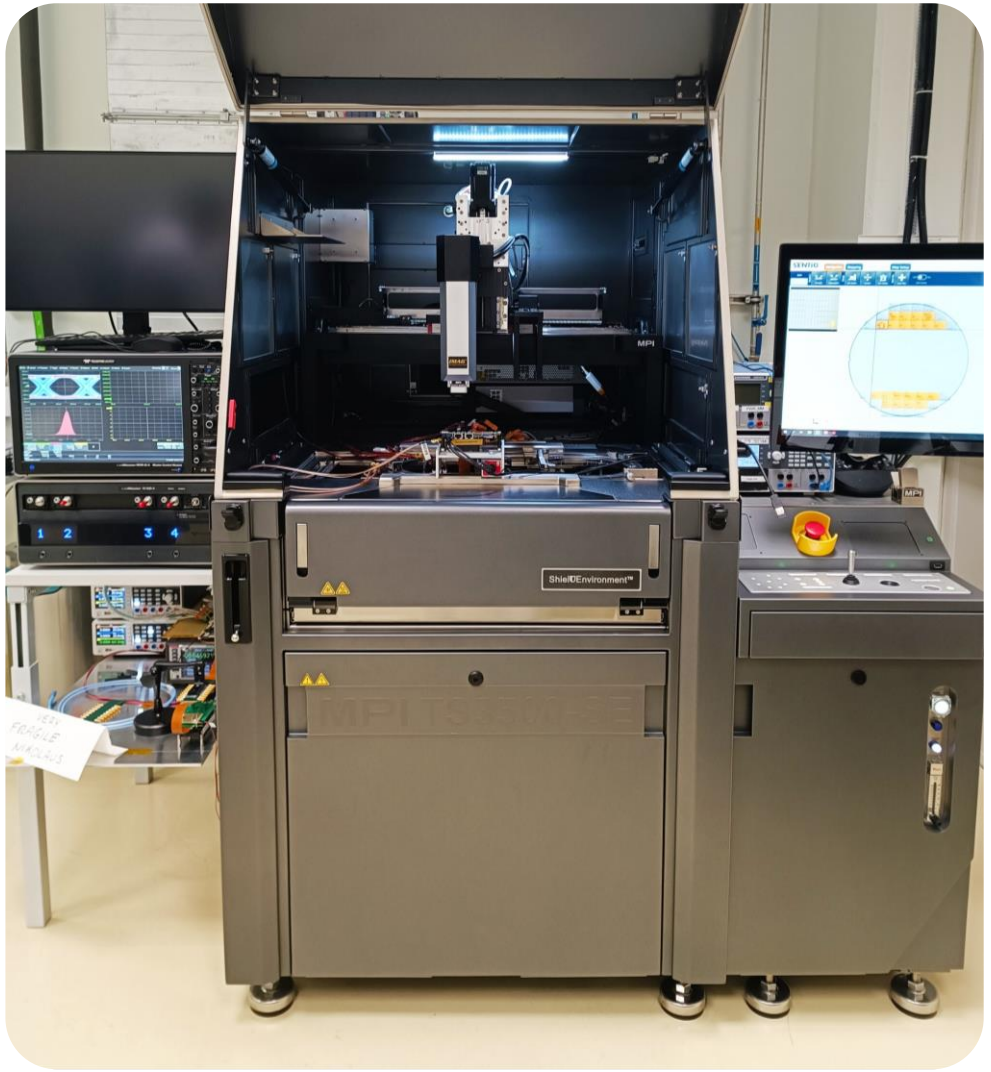
12x

Note: powering from **LEC only** feasible when limiting the number of enabled tiles

MOSAIX wafer probing

On-wafer testing of full MOSAIX production (2 x 25 wafers): **max. coverage on functionality, including high-speed tests**

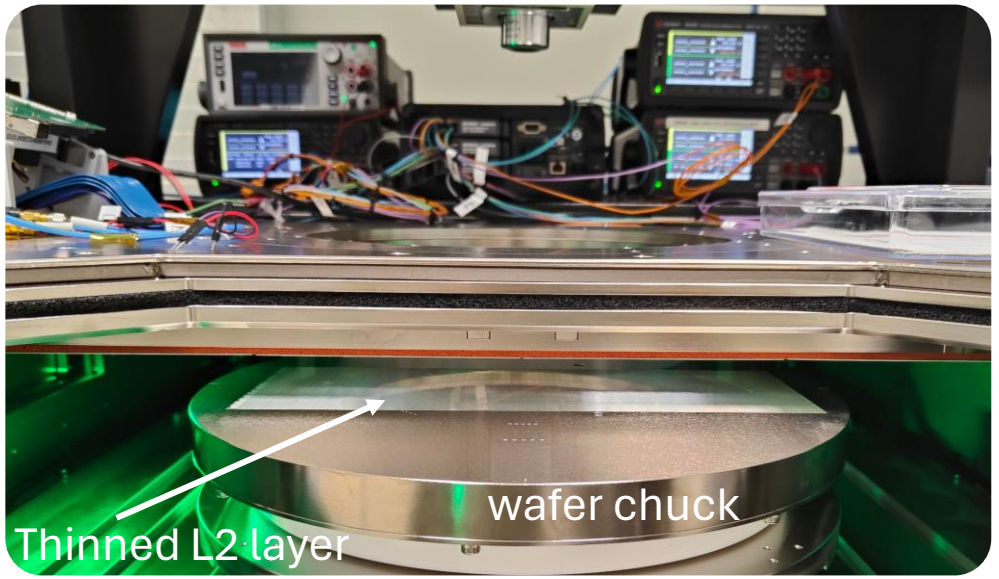
Note: Test beam measurements and irradiation campaigns performed on carrier PCB's, not covered here

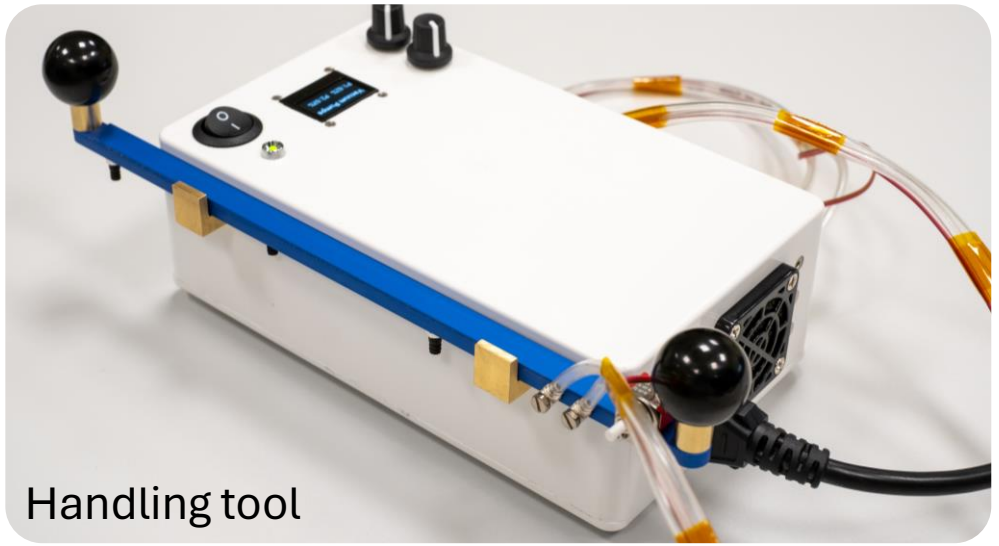


MOSAIX wafer probing – thinned layers

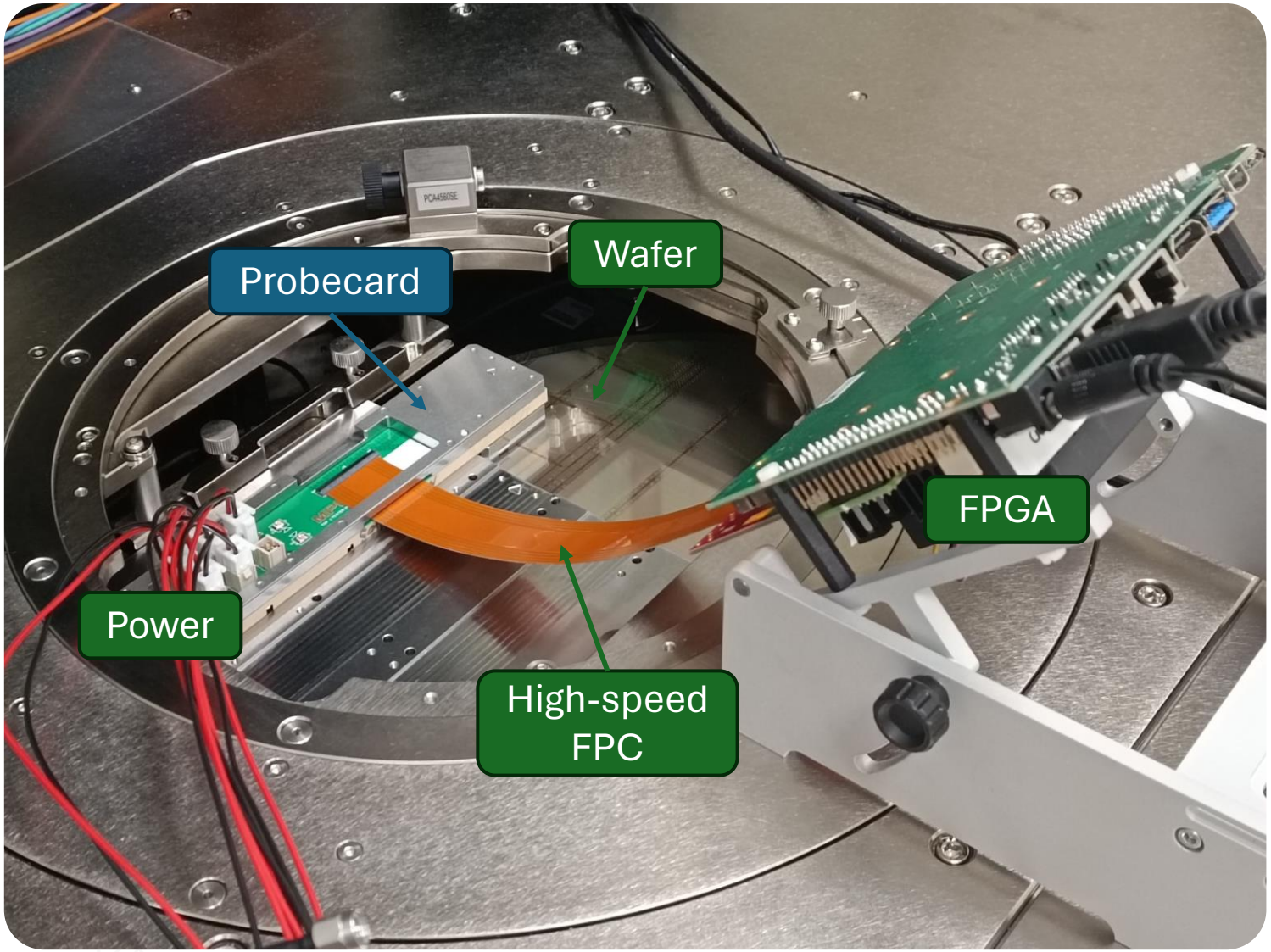
Developed procedure to test 50 µm thinned layers of any size

- Custom handling tool to pick-up and transfer thinned layers
- Custom mylar cover sheet allows to uniformly suck silicon layers flat onto the chuck



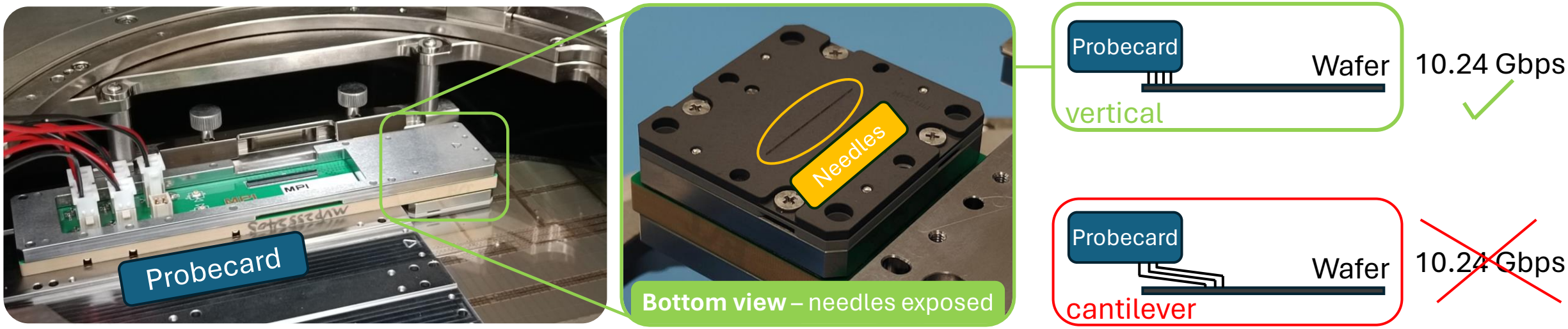


MOSAIX wafer probing – high-speed



- Commercial FPGA (Arria10 + Enclustra baseboard) – uniform test infrastructure across carrier PCB's/test beams/detector models
- Custom high-speed FPC (flexible printed circuit) – simulations and material choice, in-house production

MOSAIX wafer probing – high-speed

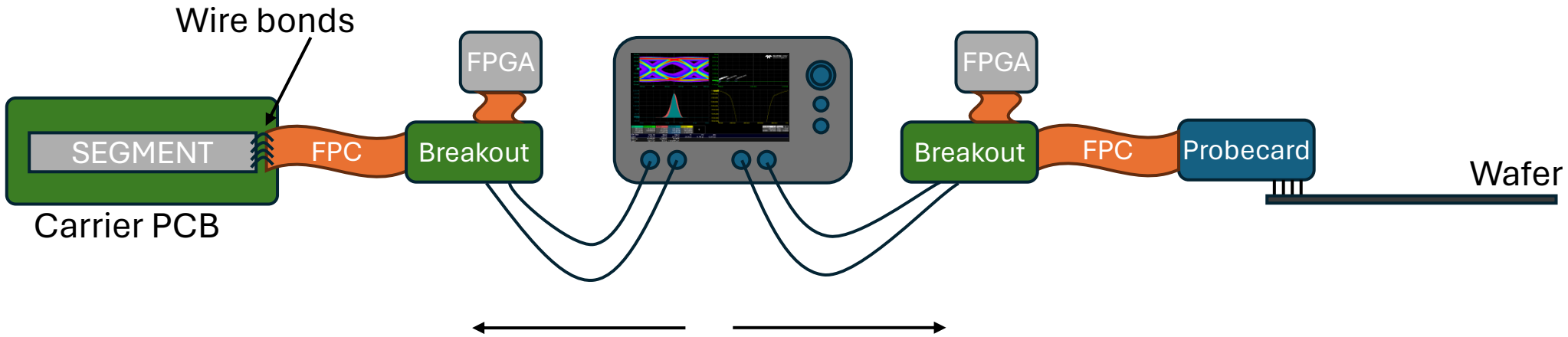


Vertical probe needles, embedded in MLO (multilayer organic material)

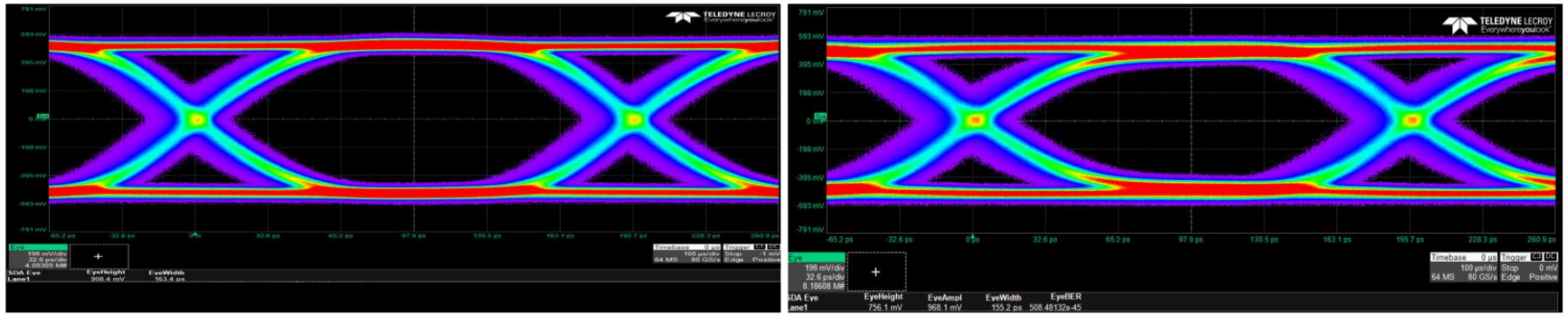
- High-speed vertical probecard co-developed with industry partner – low inductance, and impedance matching for stable 10.24 Gbps transmission

Large advancement over standard cantilever probecards (also produced, baseline, no high-speed tests possible)

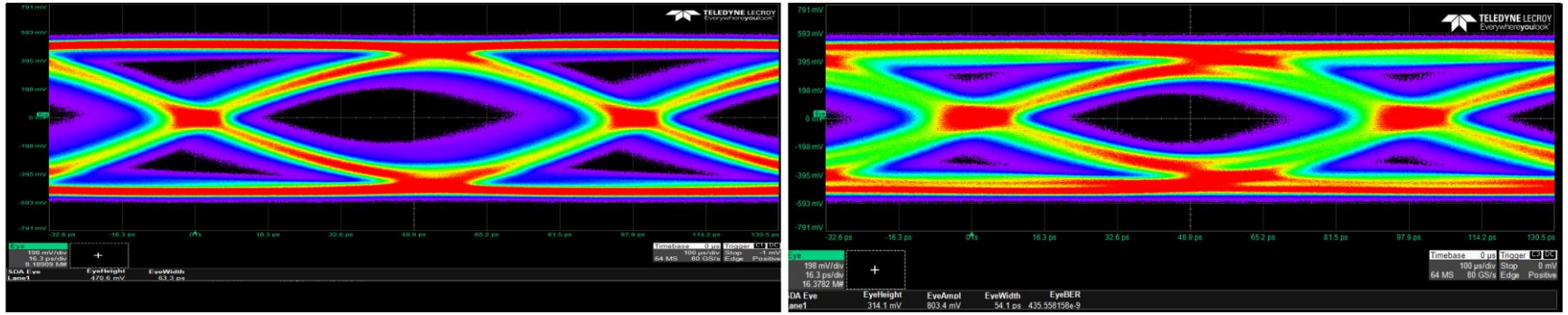
High-speed capability



5.12 Gbps PRBS



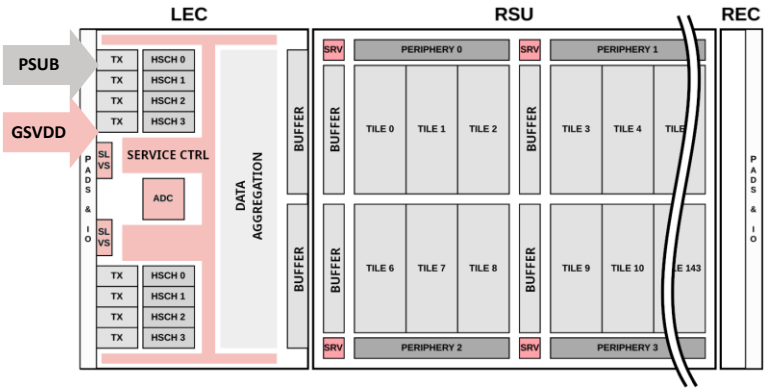
10.24 Gbps PRBS



Wafer probing at 10.24 Gbps achieved! (BER@FPGA <1e-12, see later)

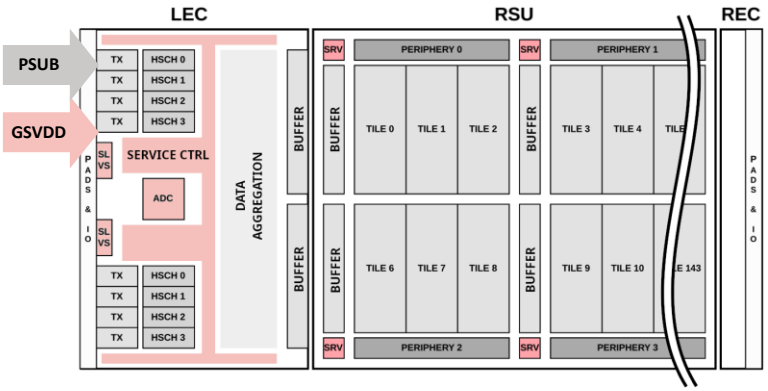
Testing sequence

Primary sequence

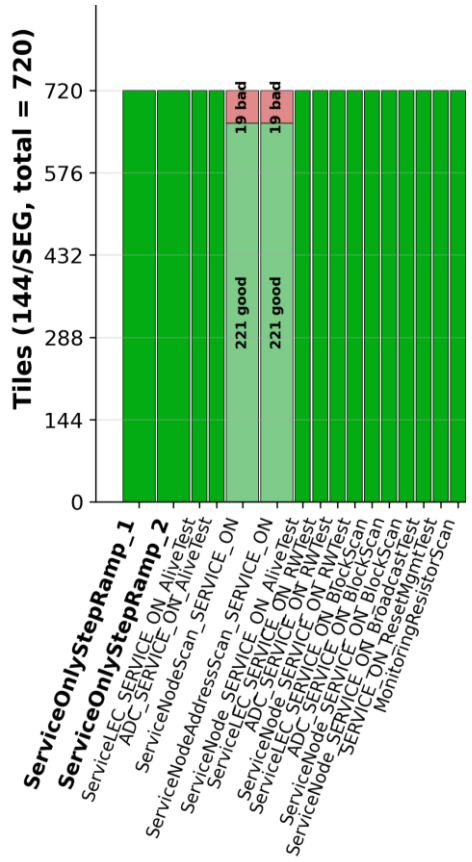


Testing sequence

Primary sequence



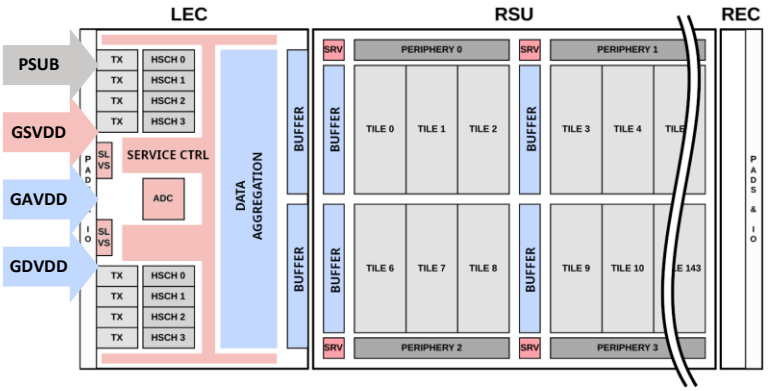
1 wafer, 5 SEG

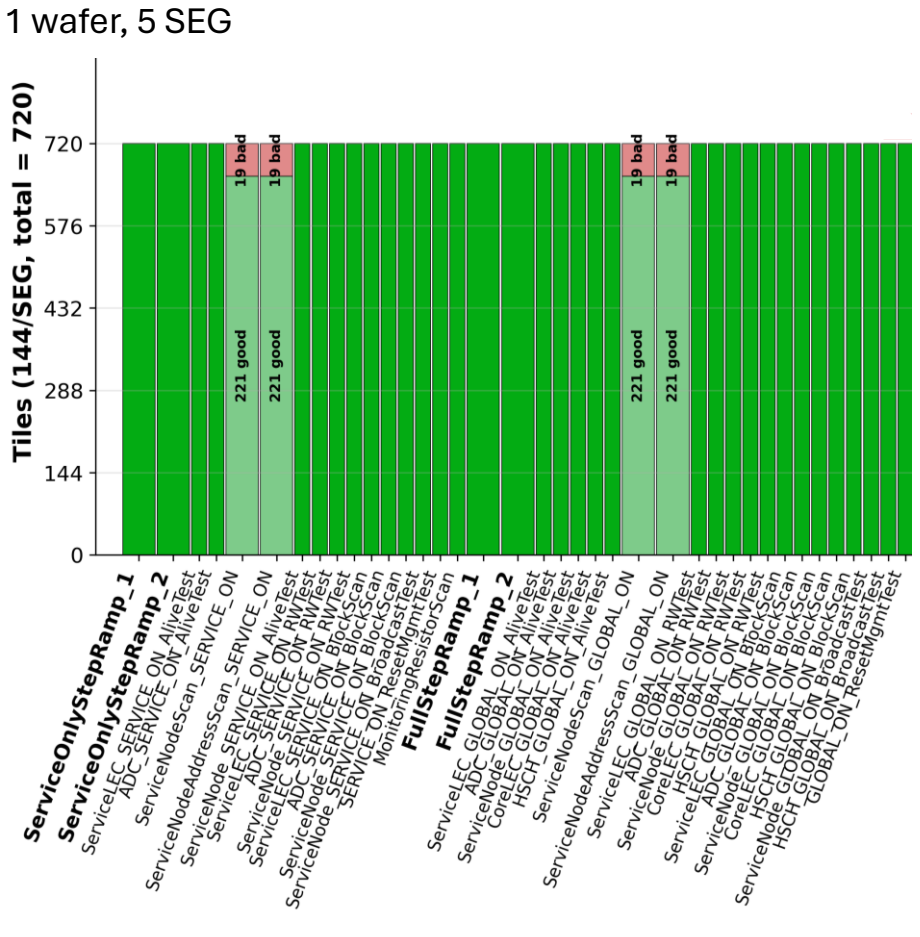


Checking Service registers and Service Nodes

Testing sequence

Primary sequence



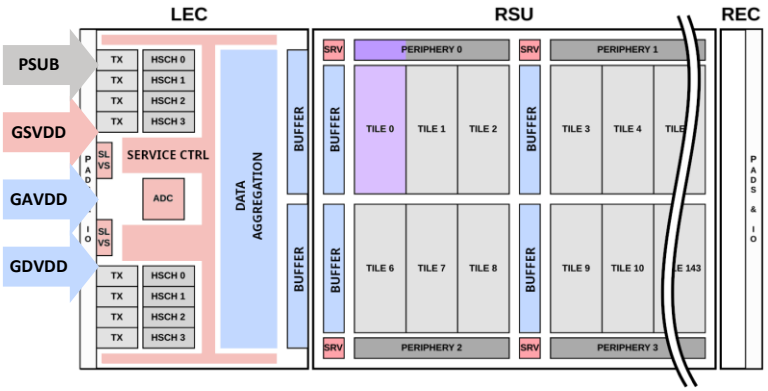


Global power up
Core and service registers

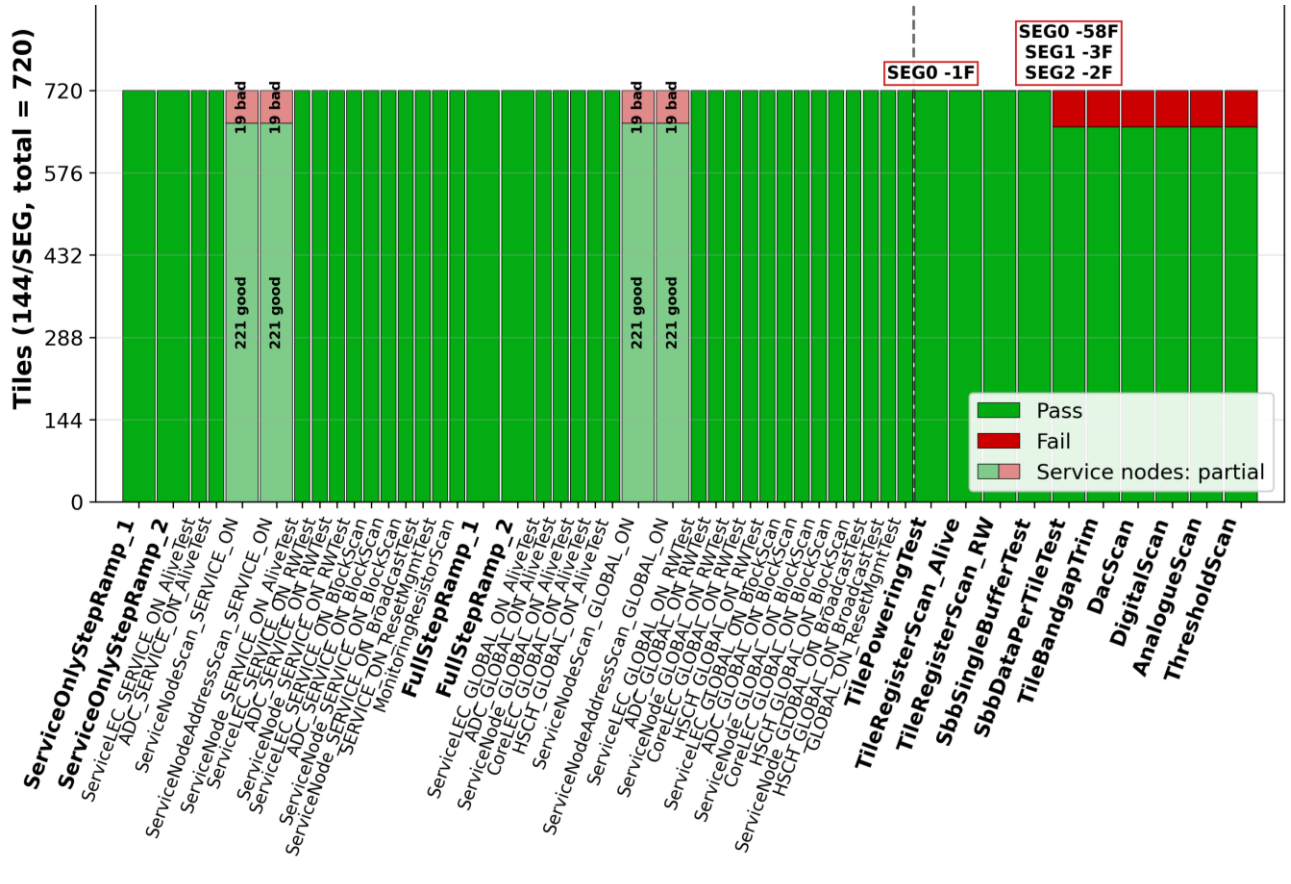
Testing sequence

Primary sequence

Tile sequence



1 wafer, 5 SEG

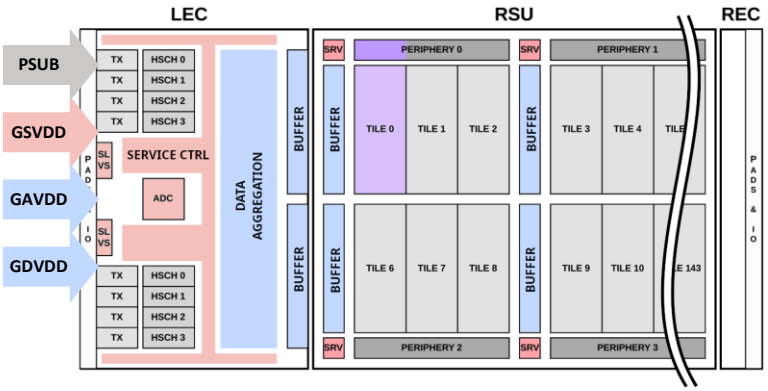


1-by-1 tile testing: power, registers, data, DACs, pixels

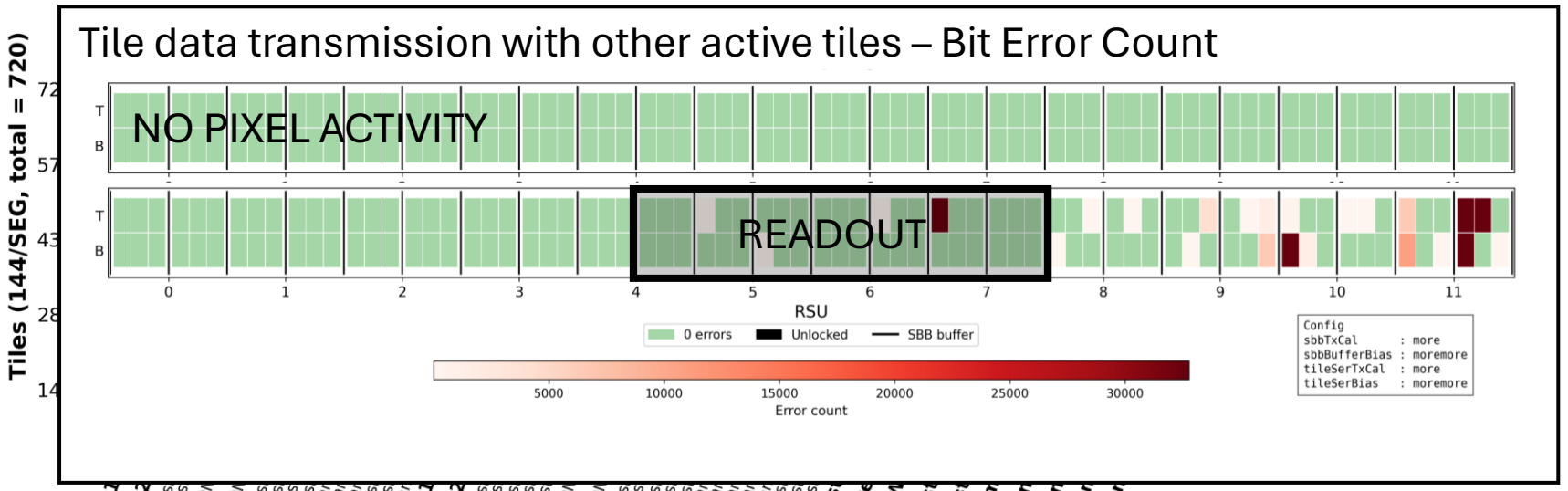
Testing sequence

Primary sequence

Tile sequence



1 wafer, 5 SEG



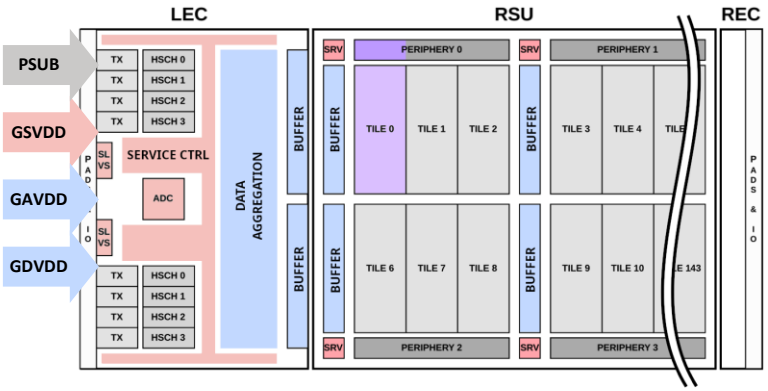
Weakness solved: unshielded in-metal stack area found and closed (next run)

1-by-1 tile testing: power, registers, data, DACs, pixels

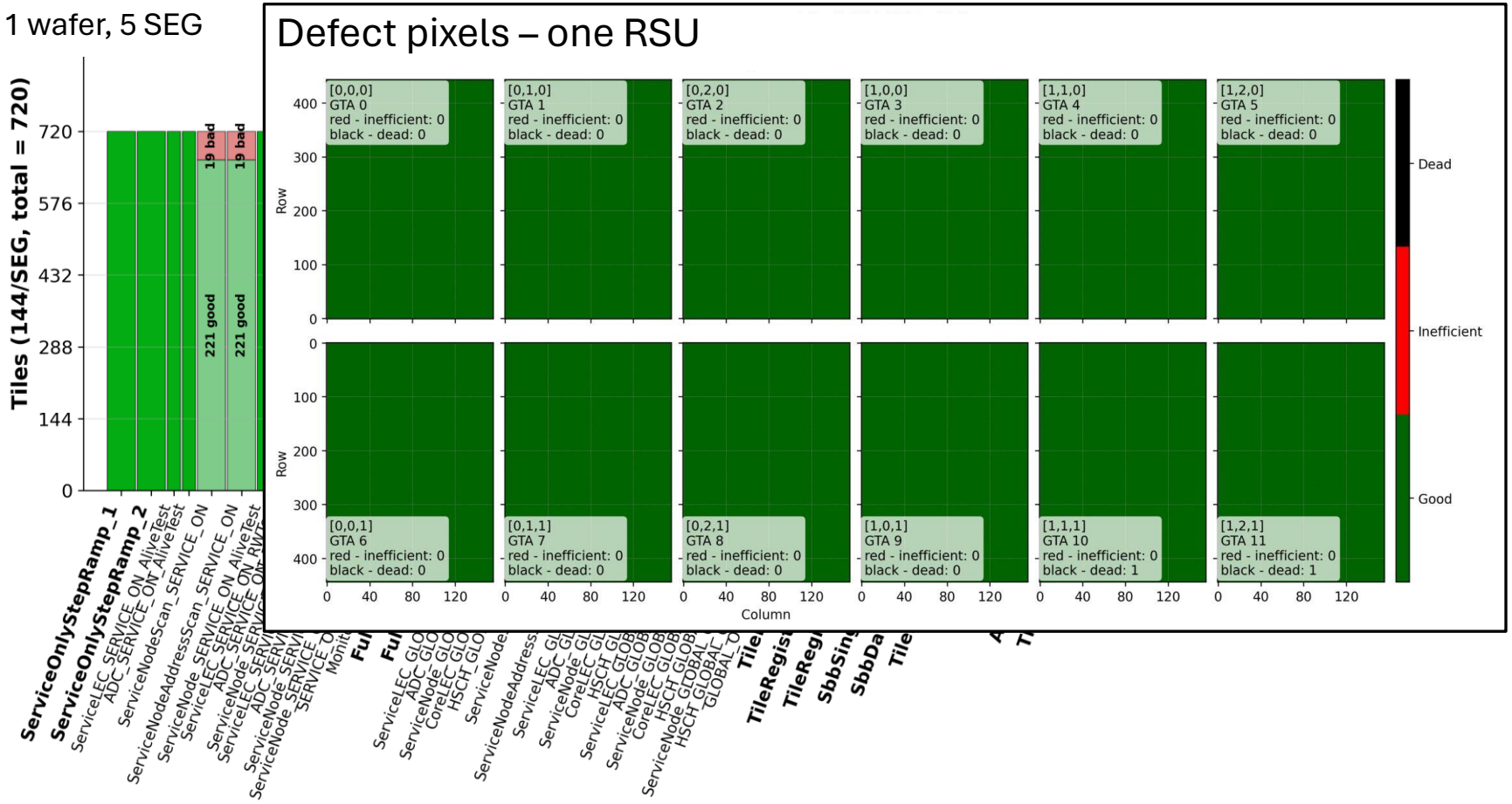
Testing sequence

Primary sequence

Tile sequence



1 wafer, 5 SEG

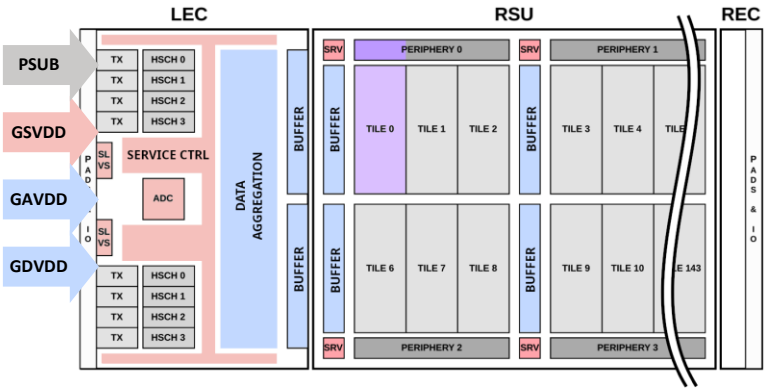


1-by-1 tile testing: power, registers, data, DACs, pixels

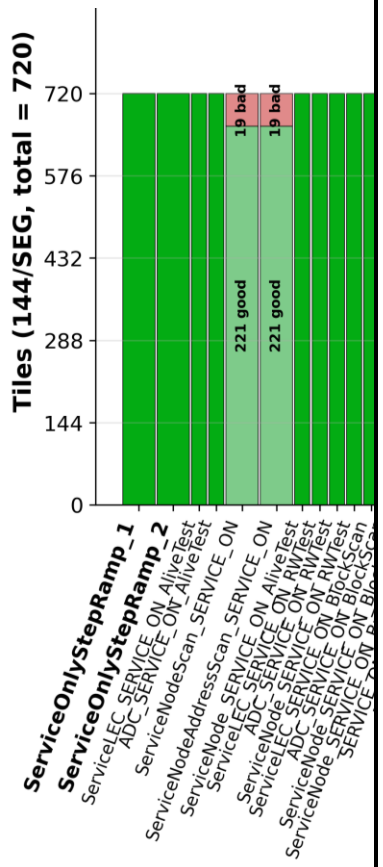
Testing sequence

Primary sequence

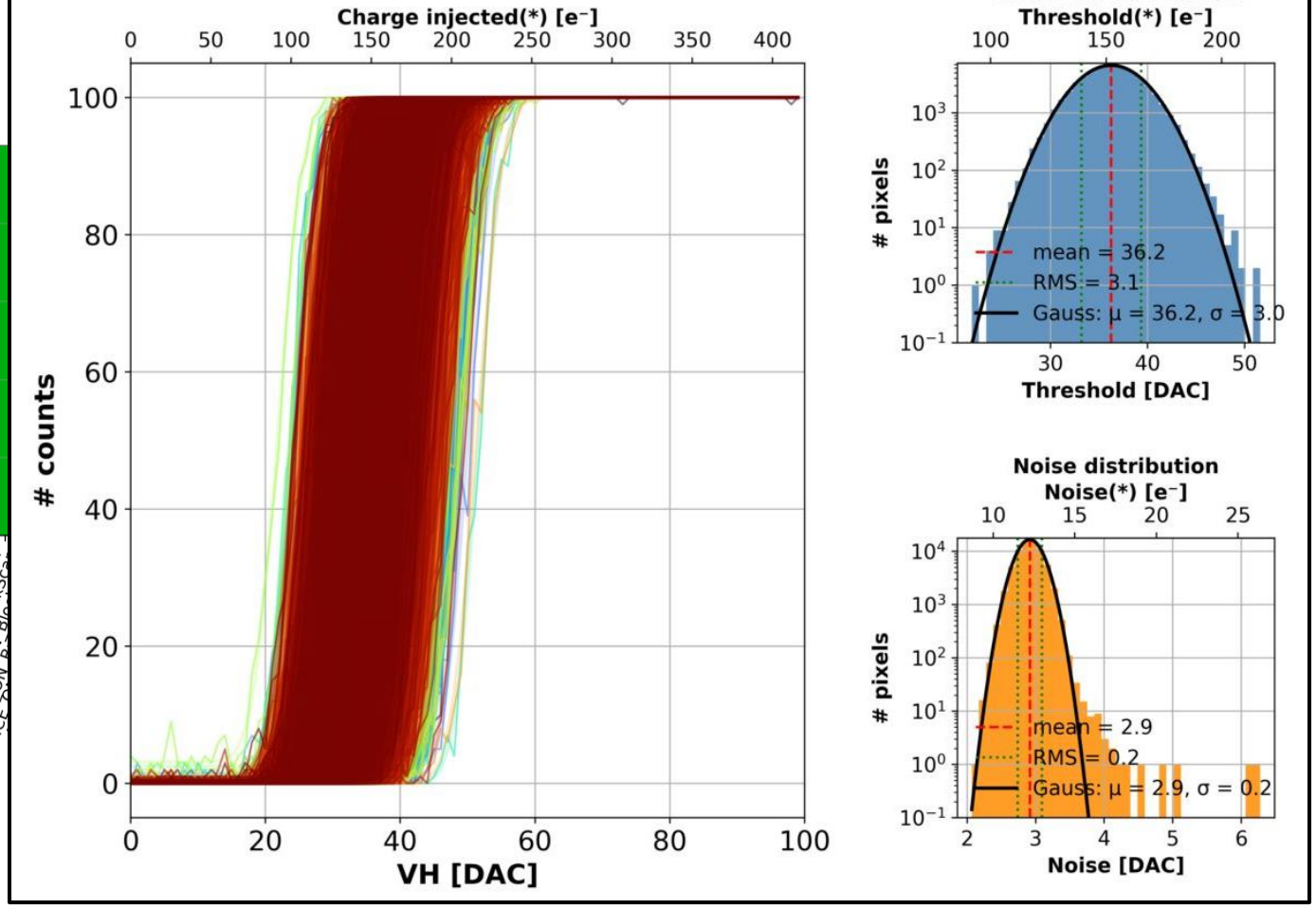
Tile sequence



1 wafer, 5 SEG



Threshold scan – one tile



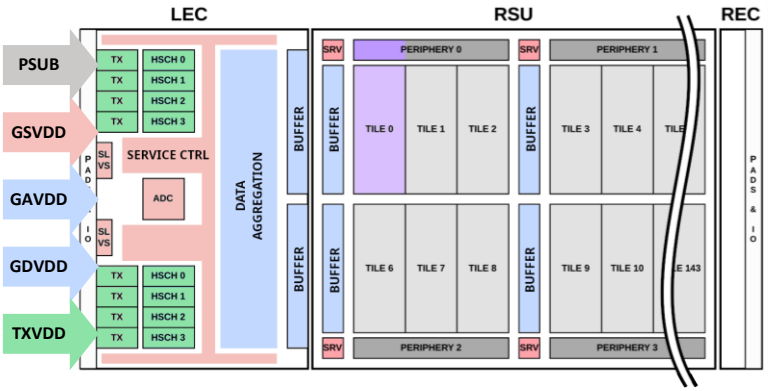
1-by-1 tile testing: power, registers, data, DACs, pixels

Testing sequence

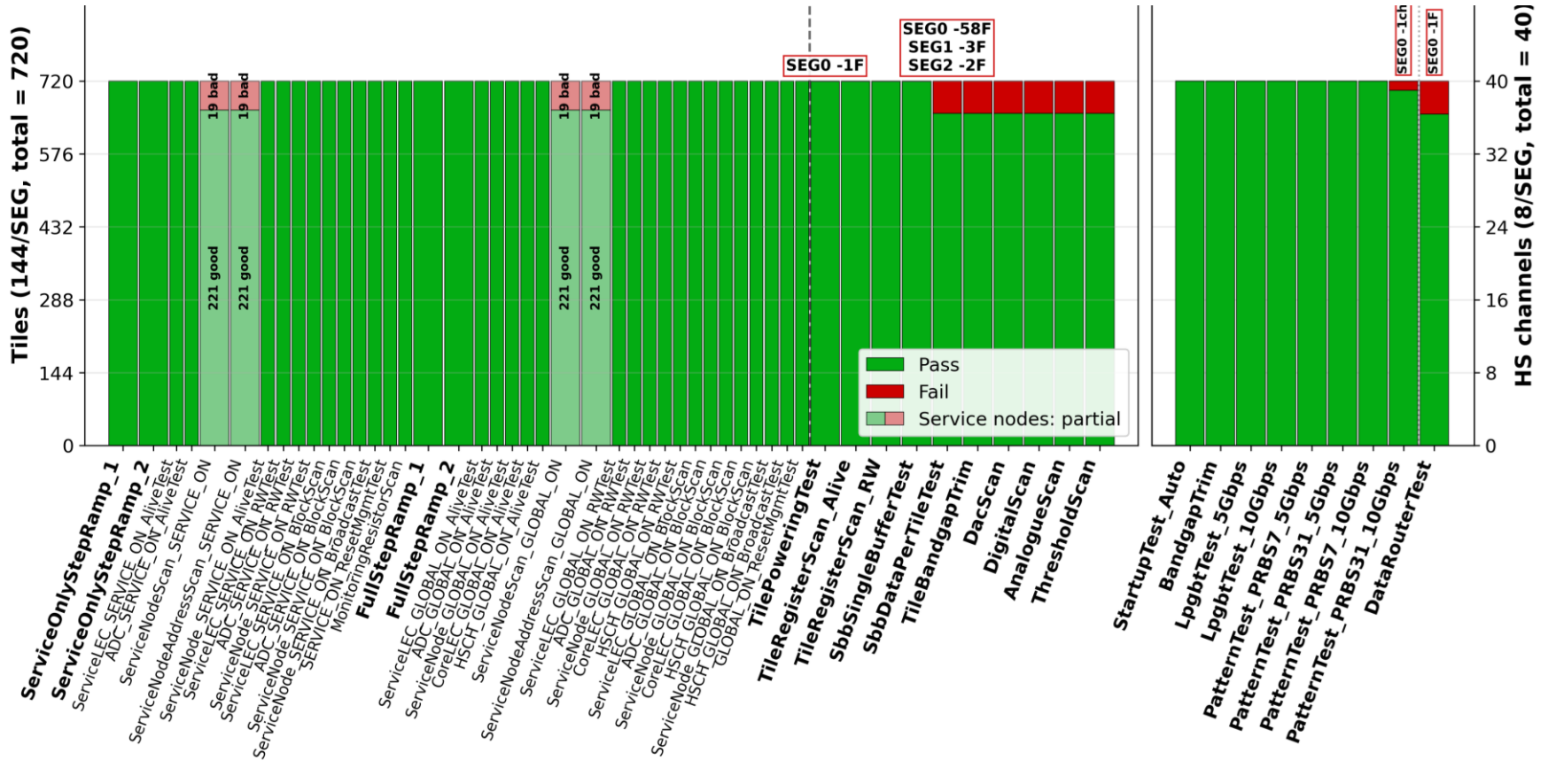
Primary sequence

Tile sequence

High-speed sequence



1 wafer, 5 SEG



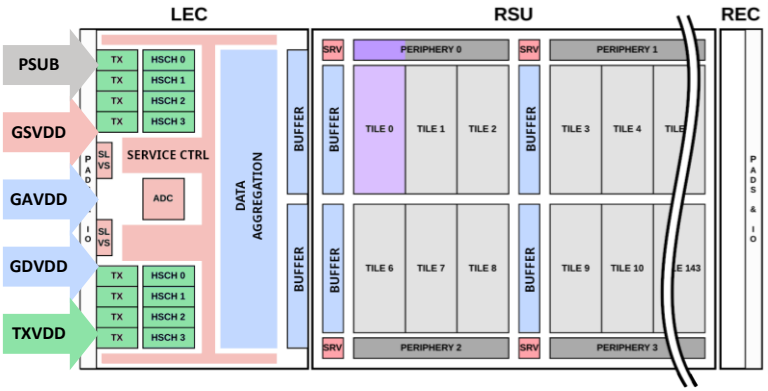
High-speed serializer and full data path

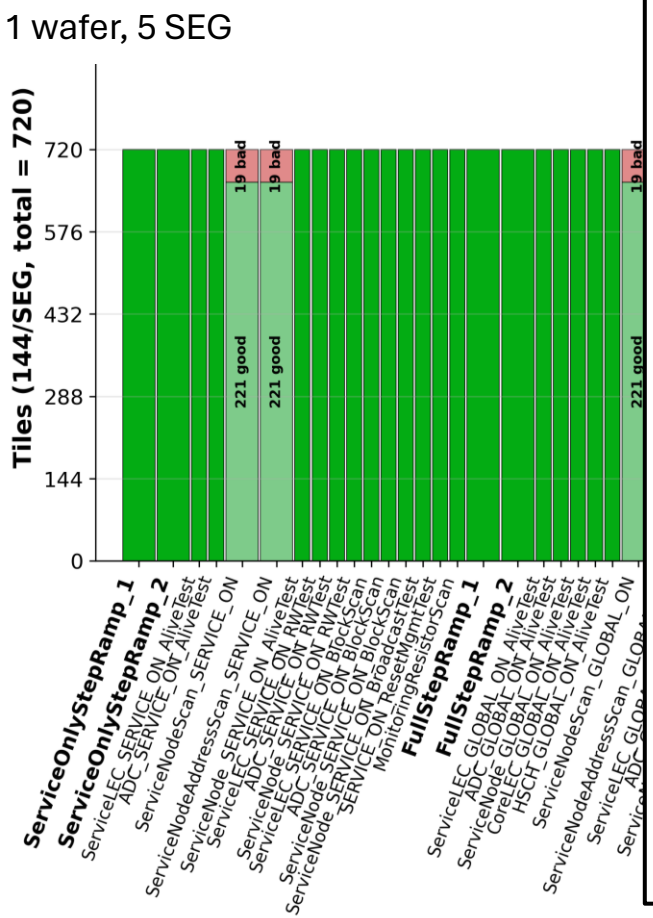
Testing sequence

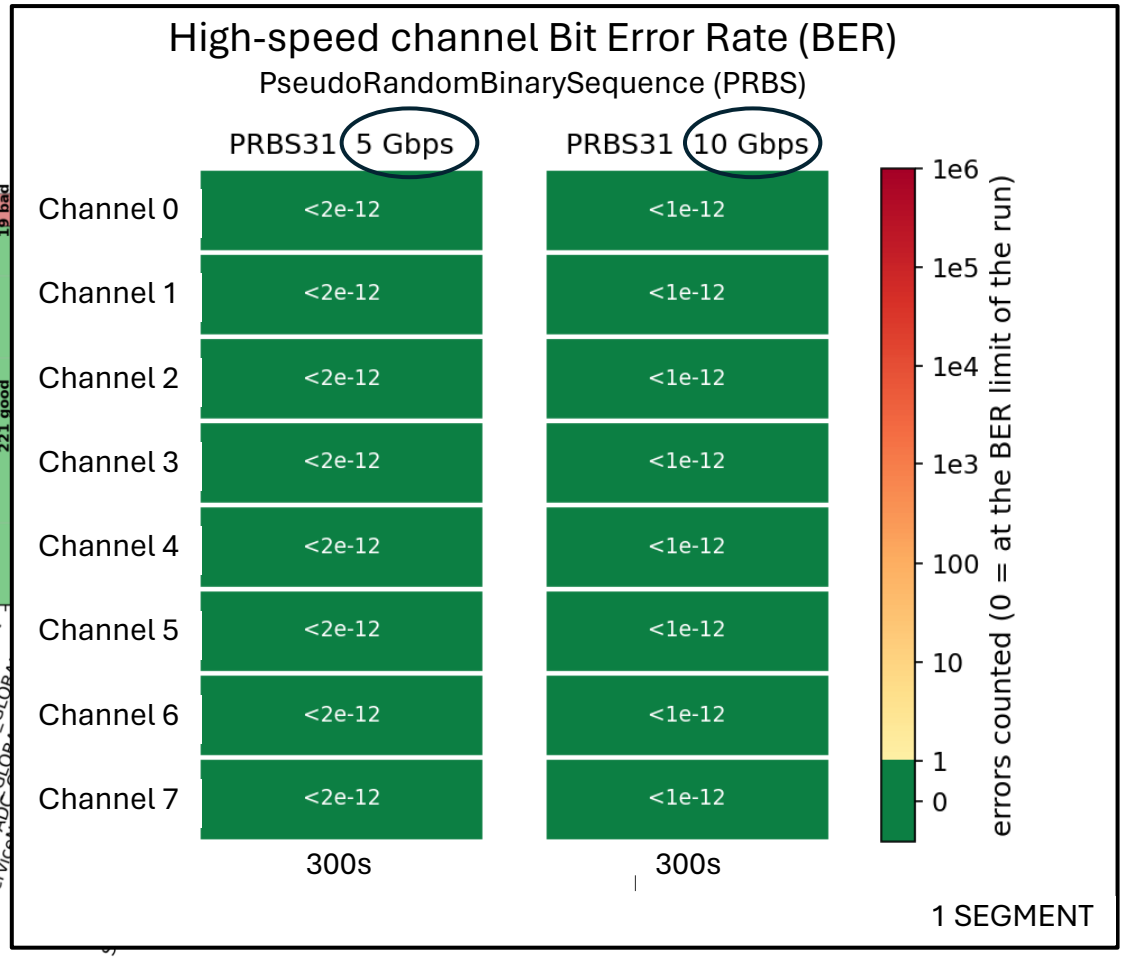
Primary sequence

Tile sequence

High-speed sequence







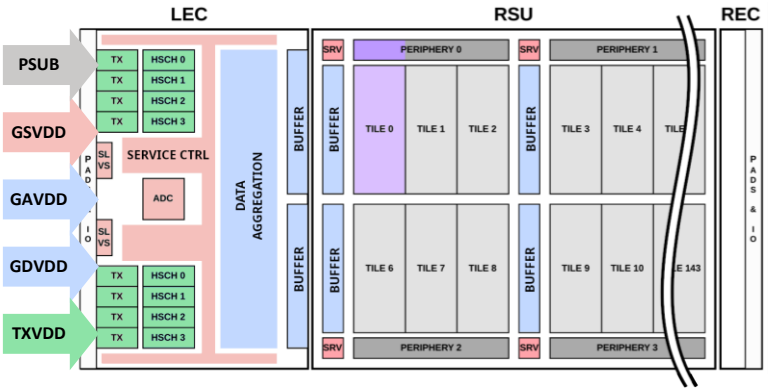
High-speed serializer and full data path

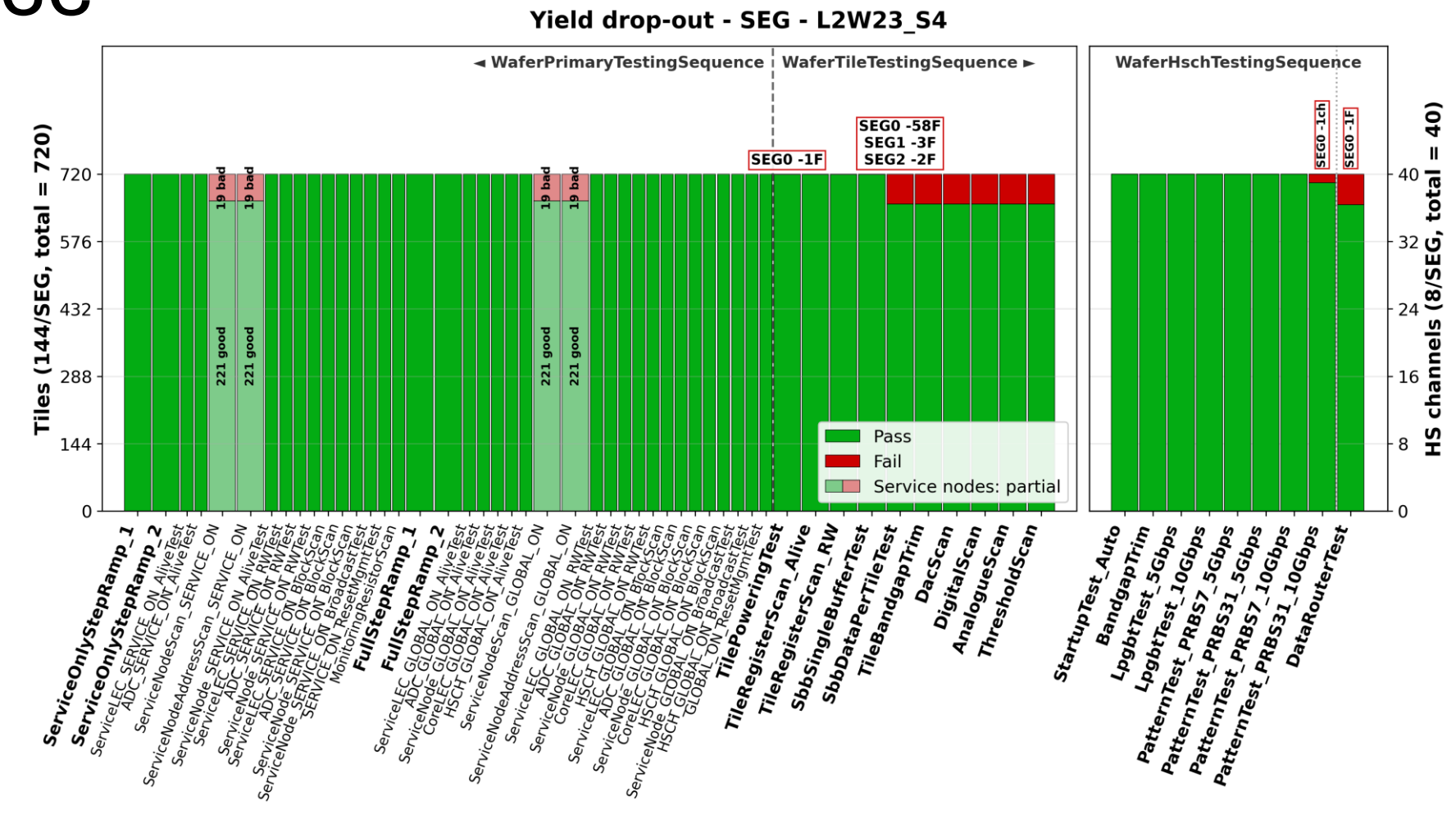
Testing sequence

Primary sequence

Tile sequence

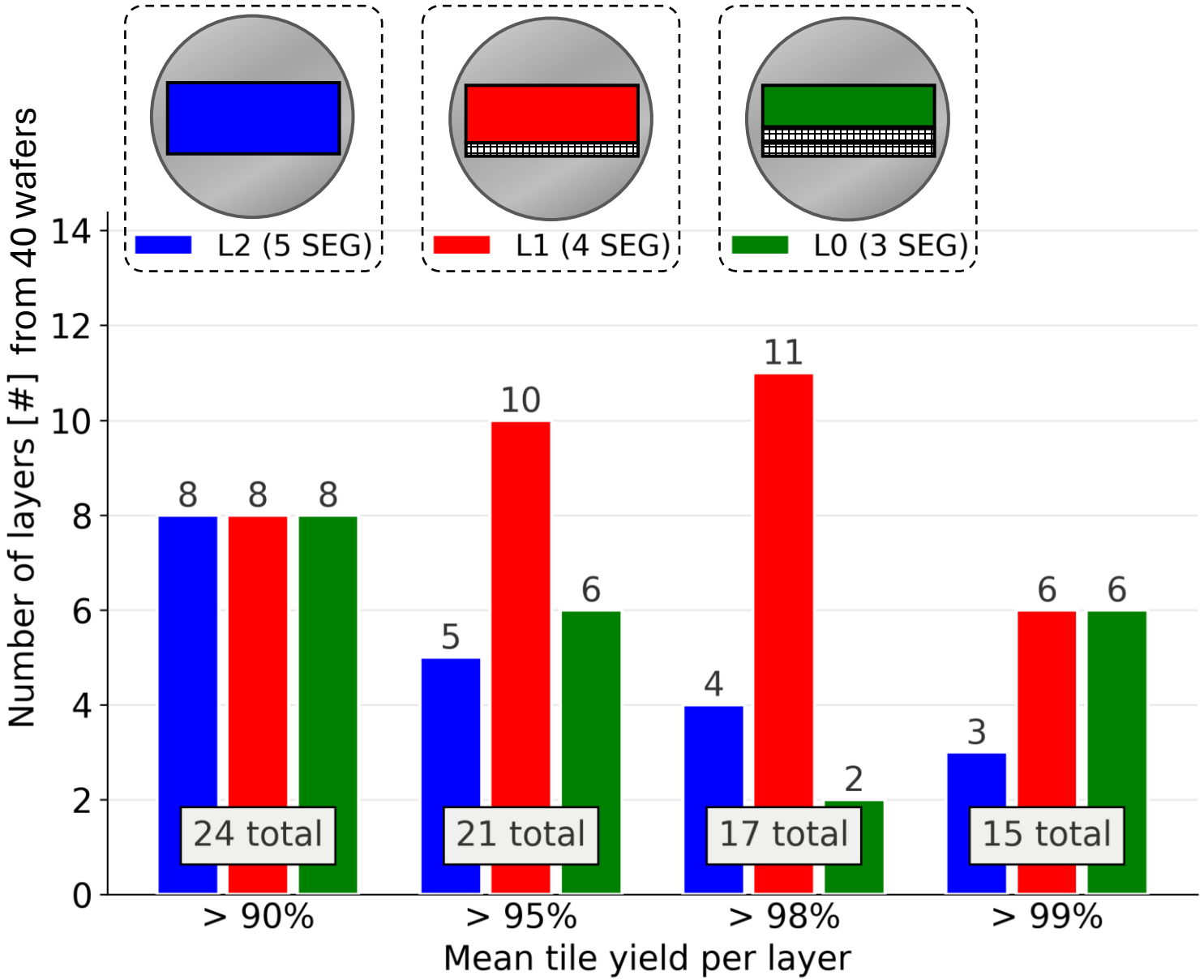
High-speed sequence



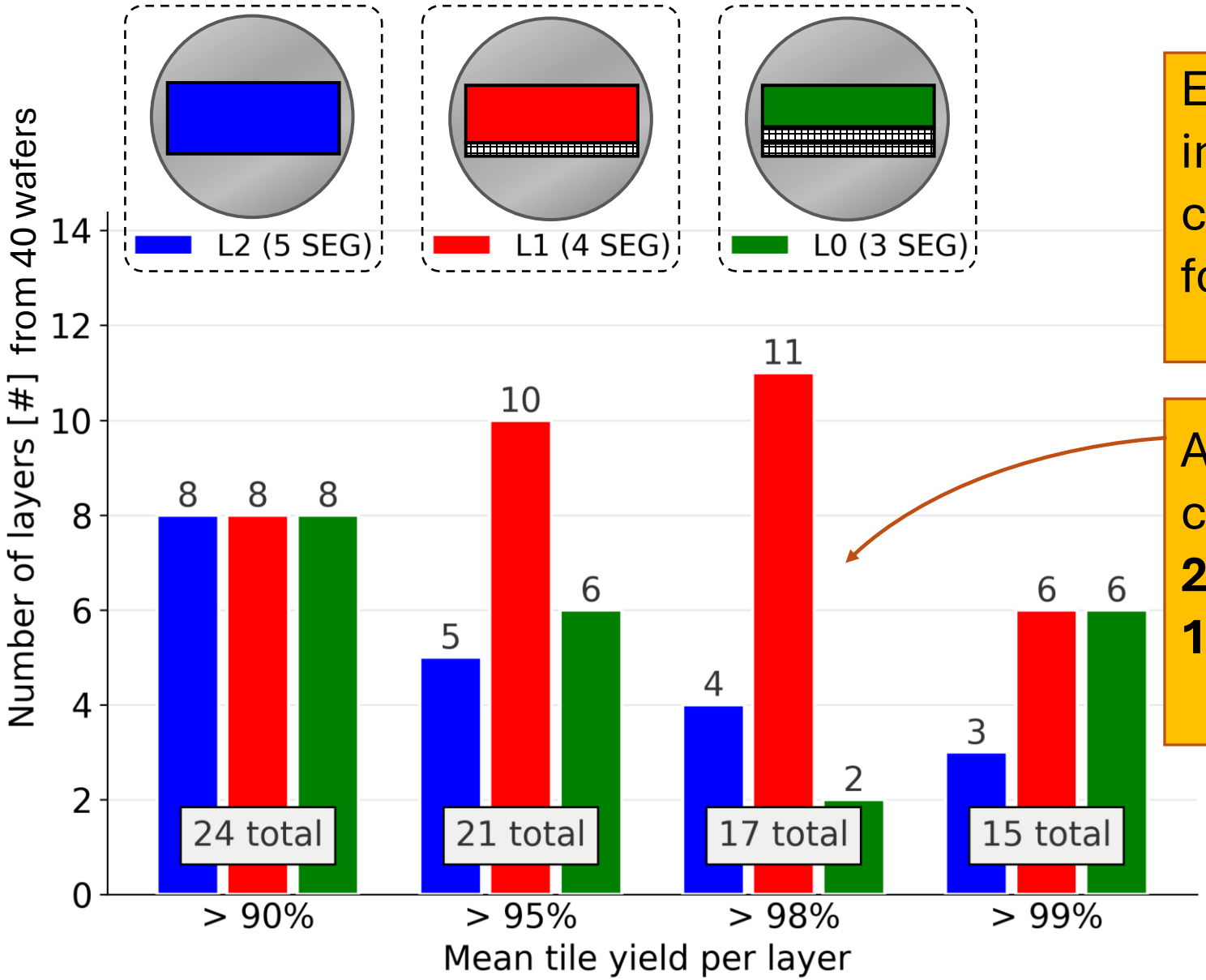


MOSAIX chip is (nearly) fully functional – crosstalk on tile links addressed in next submission (ER3)

Layer yield – maximum layer size



Layer yield – maximum layer size

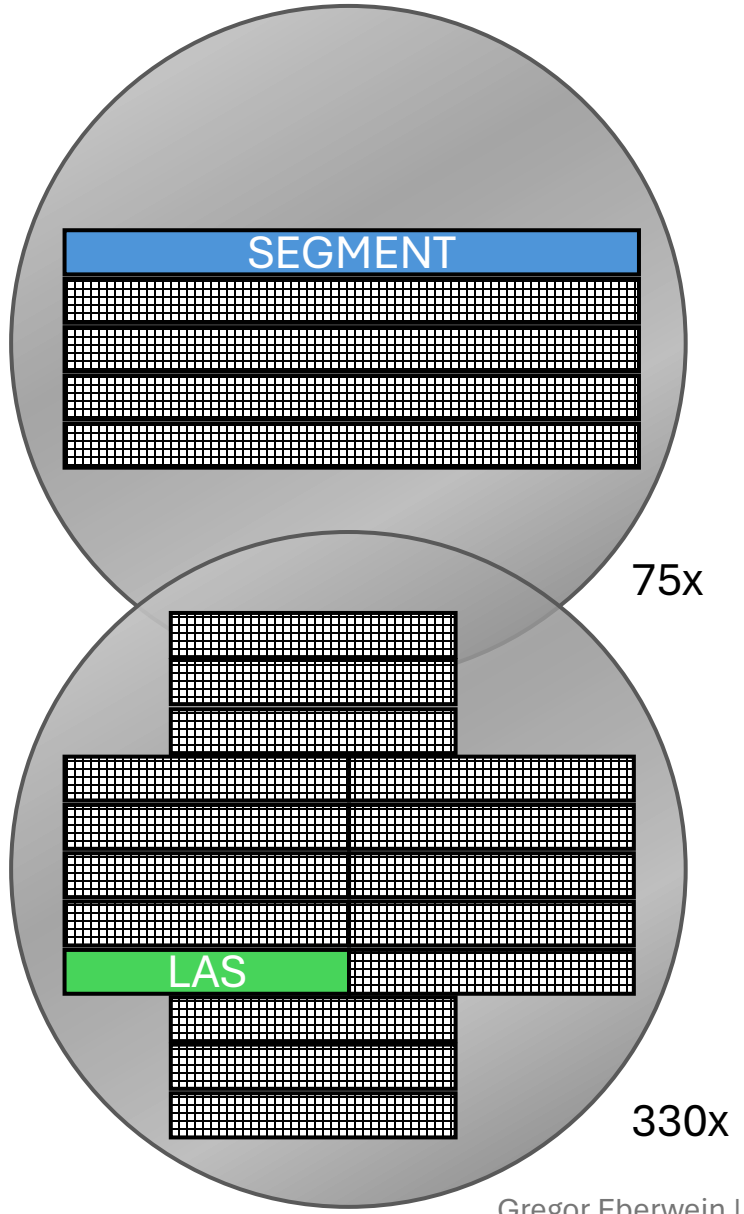


Effort on yield improvement in collaboration with the foundry ongoing

At >98% tile yield, we can build:
2x ITS3 or
1x SVT half barrel

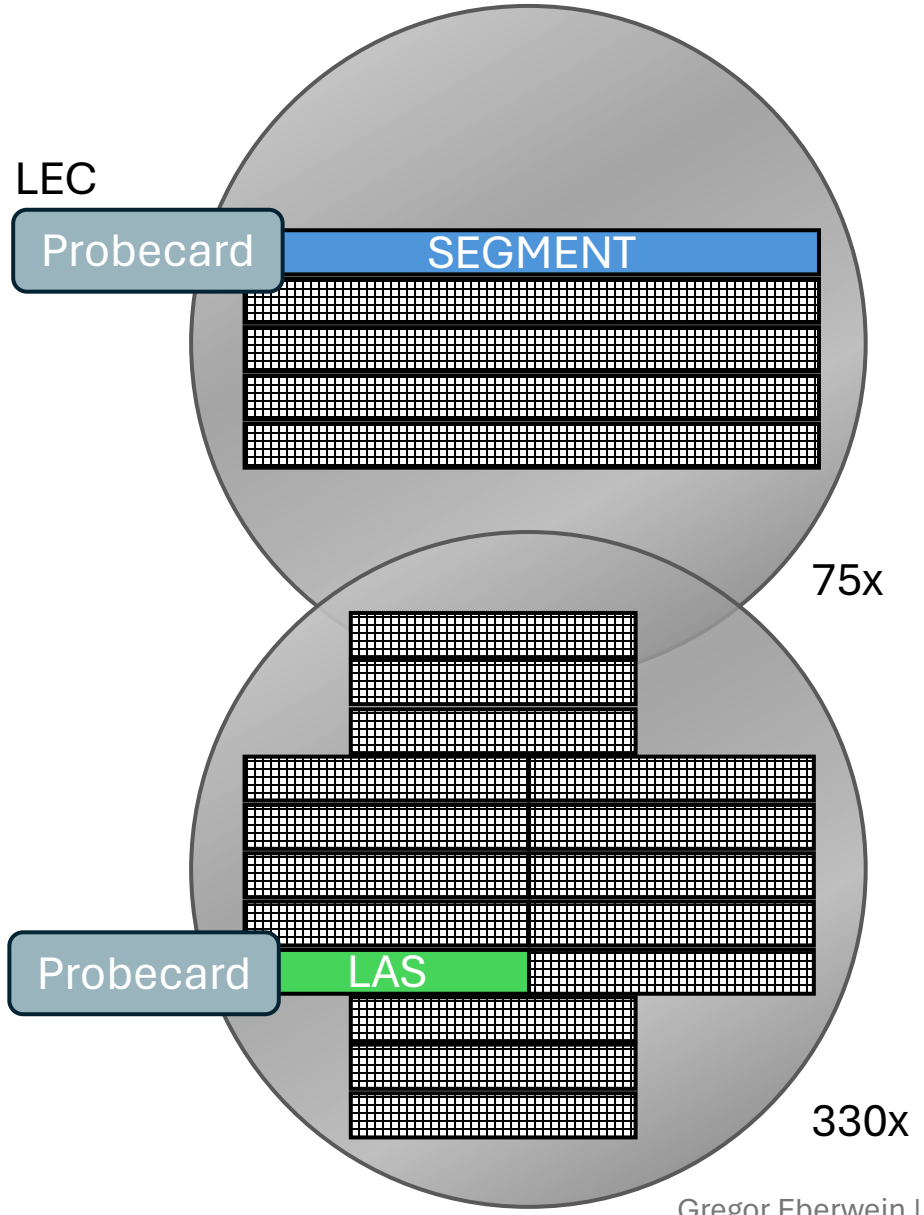
Wafer probing extensions and SVT QC

- SVT foresees a production of:
  - 75 ER3 wafers (inner barrel)
  - 330 LAS wafers (outer barrel)
  - LAS: Large Area Sensor – MOSAIX derived, with same pad structure



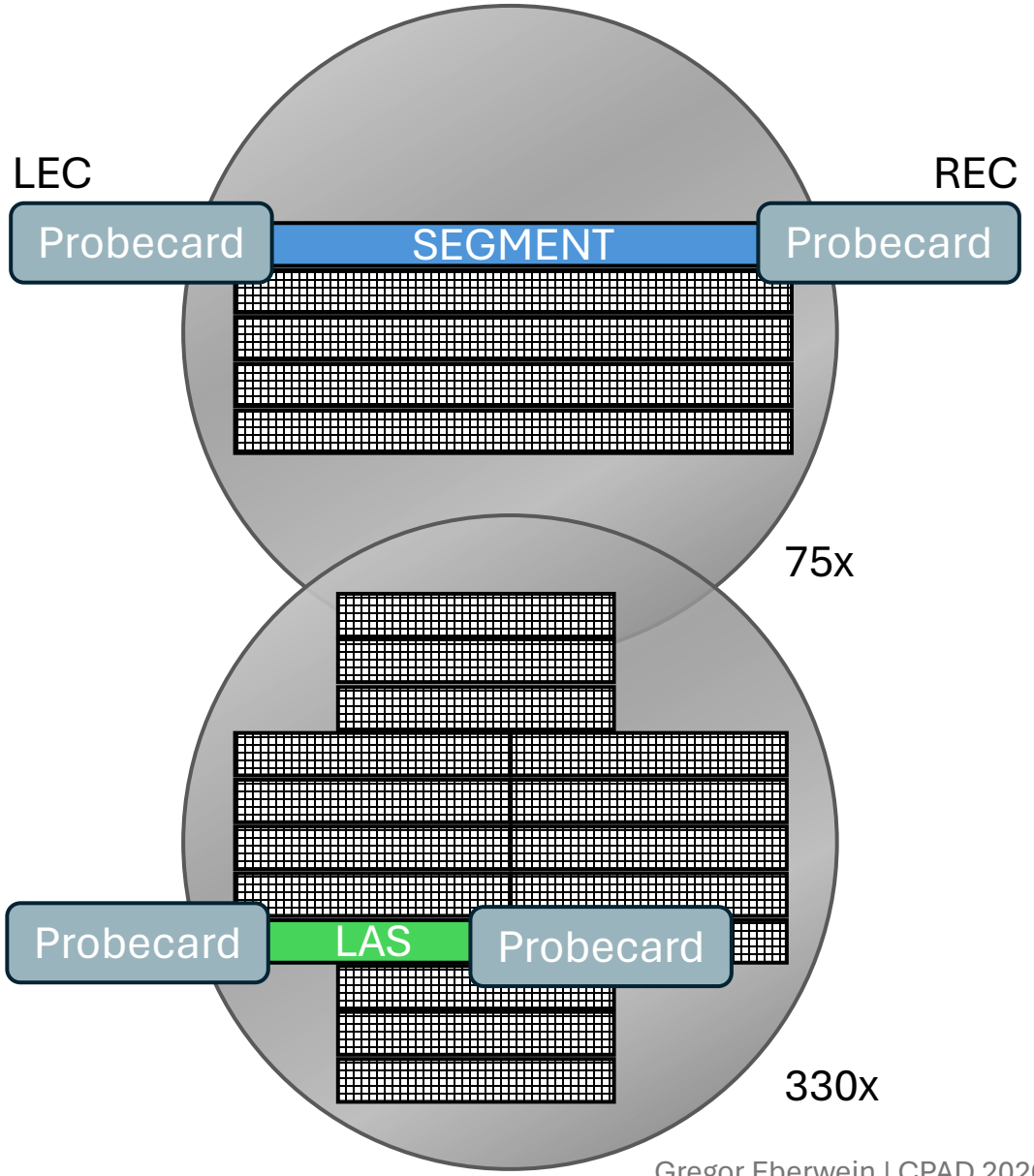
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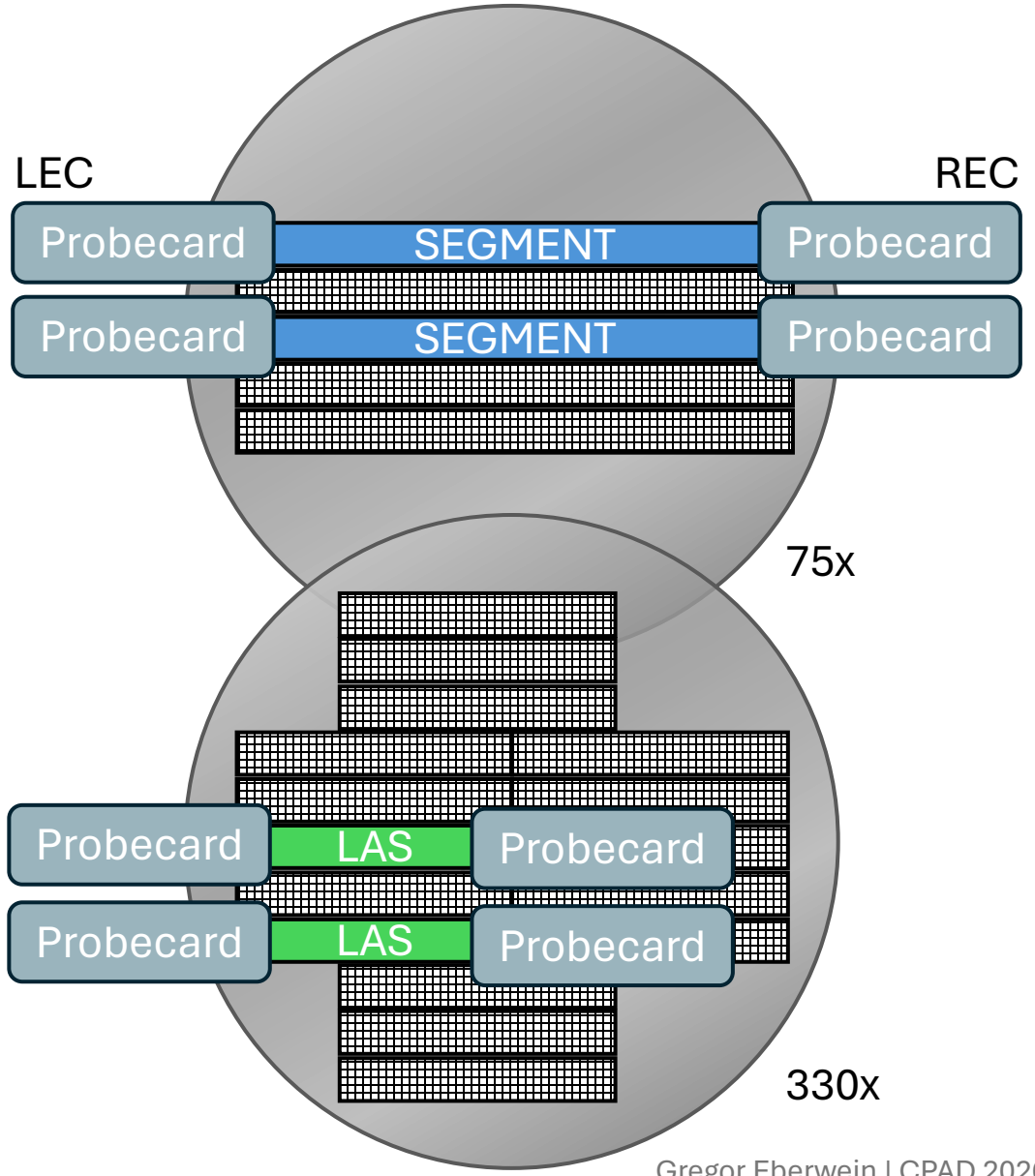
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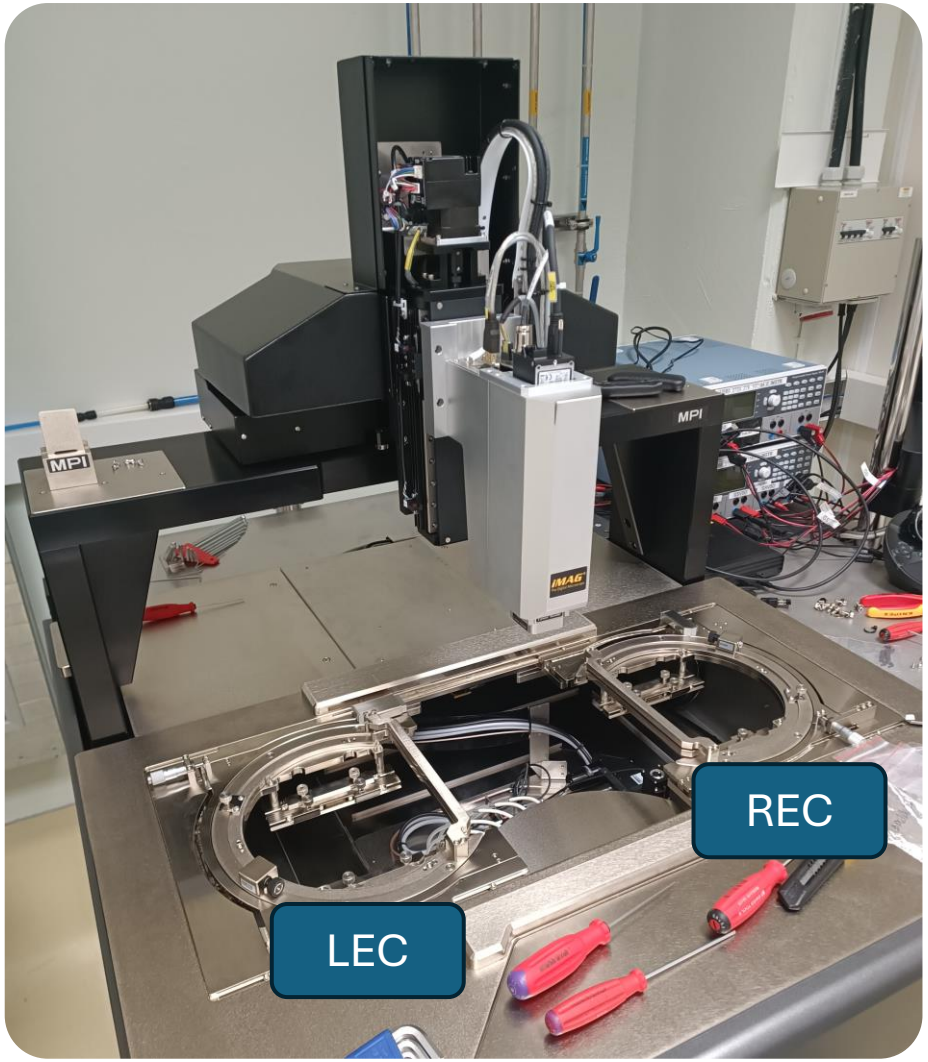
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  - LAS: Large Area Sensor – MOSAIX derived, with same pad structure
- Large volume requires fast QC procedures - paralellization required:
  - LEC + REC probecards -> allows full powering of all tiles in parallel
  - Multiple dies in parallel



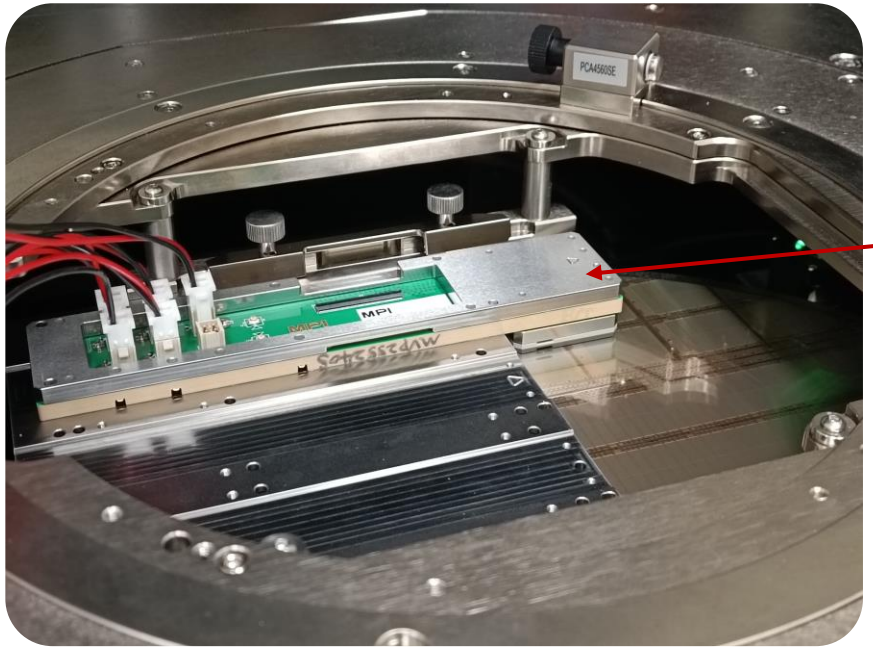
Wafer probing extensions and SVT QC

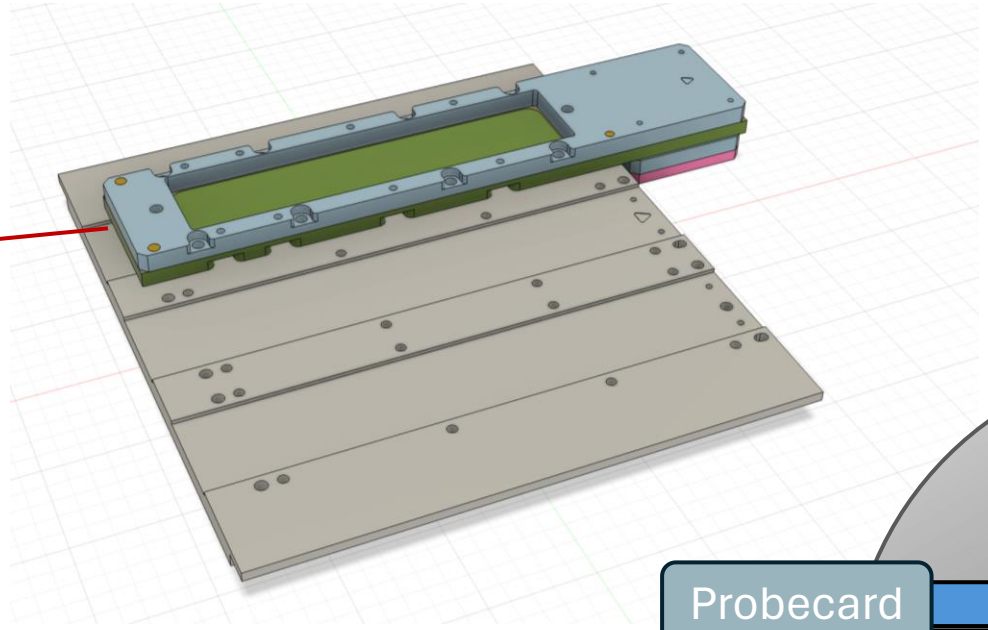
- Vertical probecard for LEC (current)
- **Additional REC probecard** (to be produced)

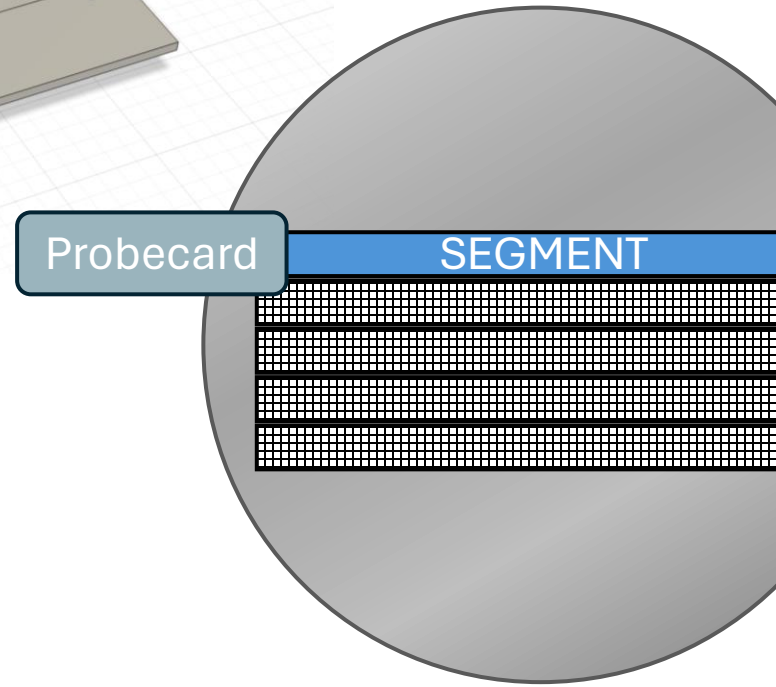
-> Full chip powering (all tiles in parallel)



Wafer probing extensions and SVT QC





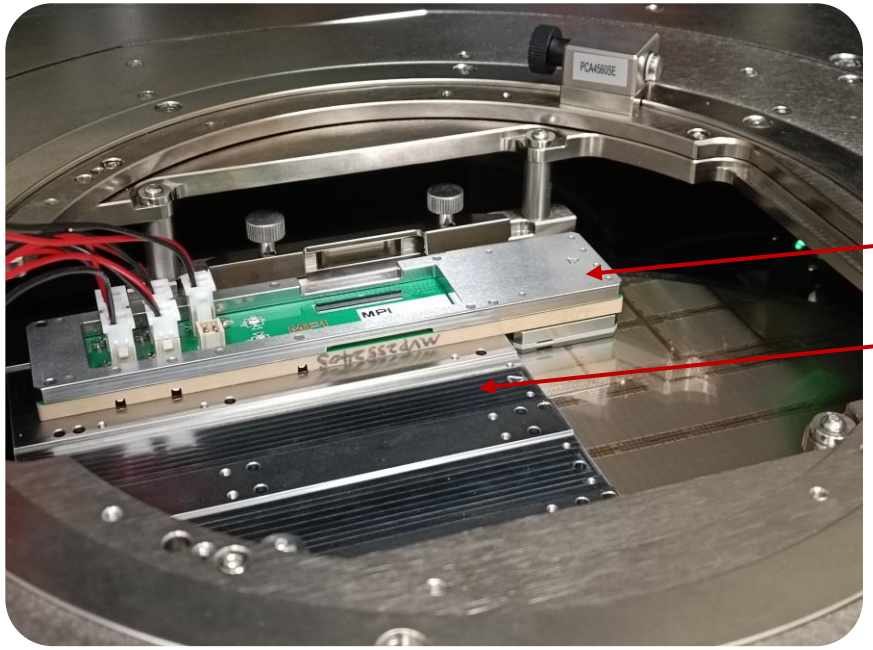


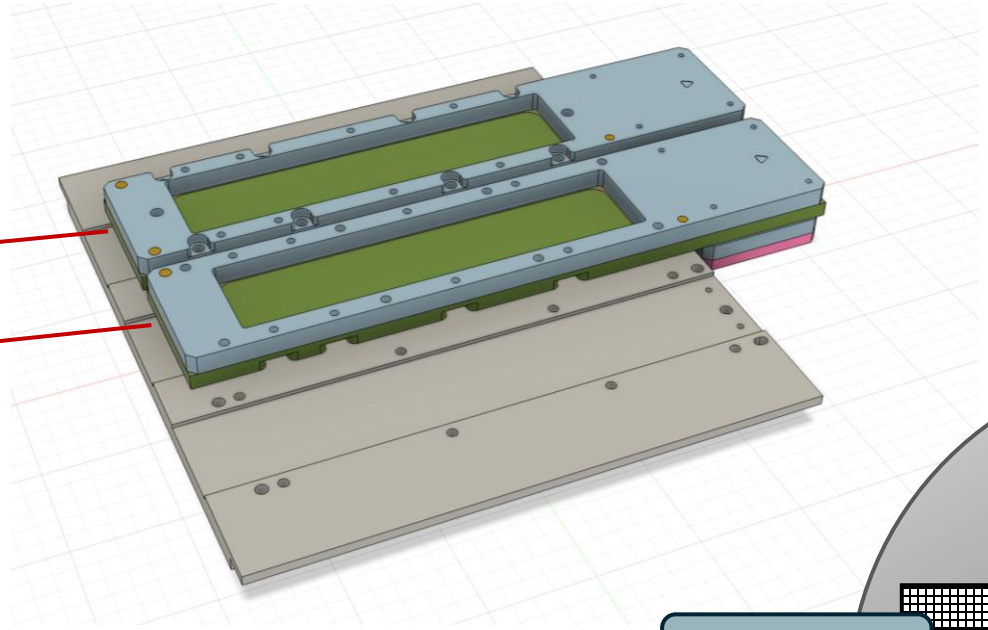
1x

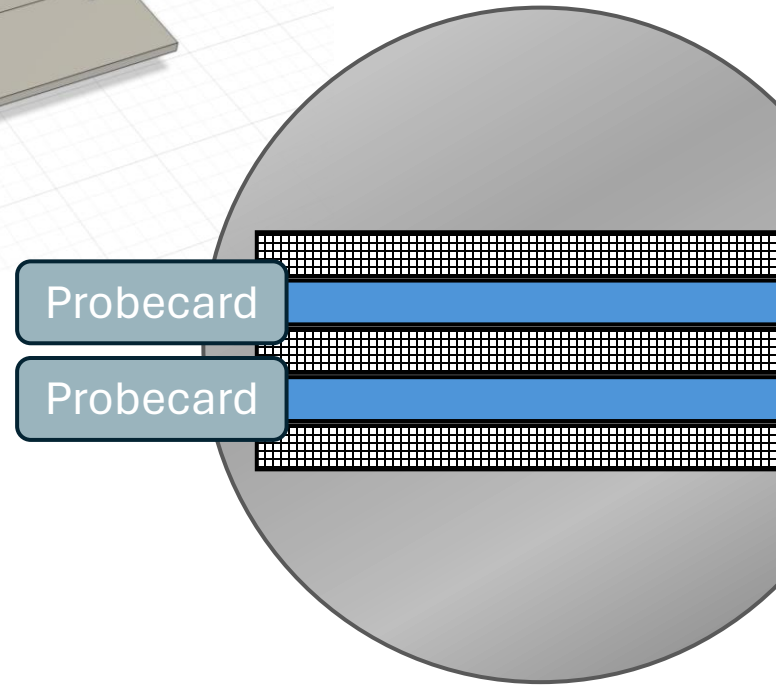
Parallelization of sensor testing:

- Up to 3 SEG in parallel (depending on arrangement)

Wafer probing extensions and SVT QC



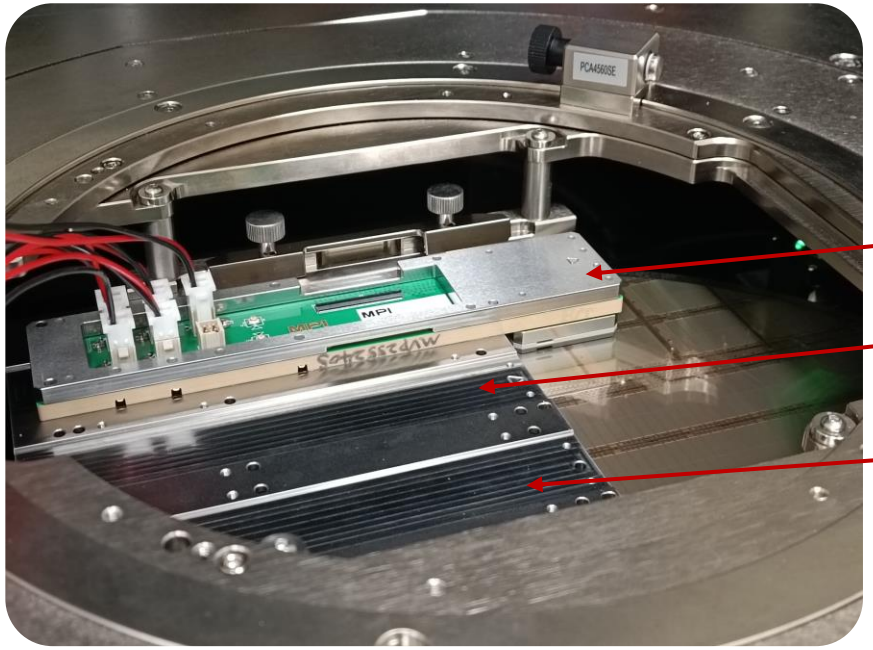


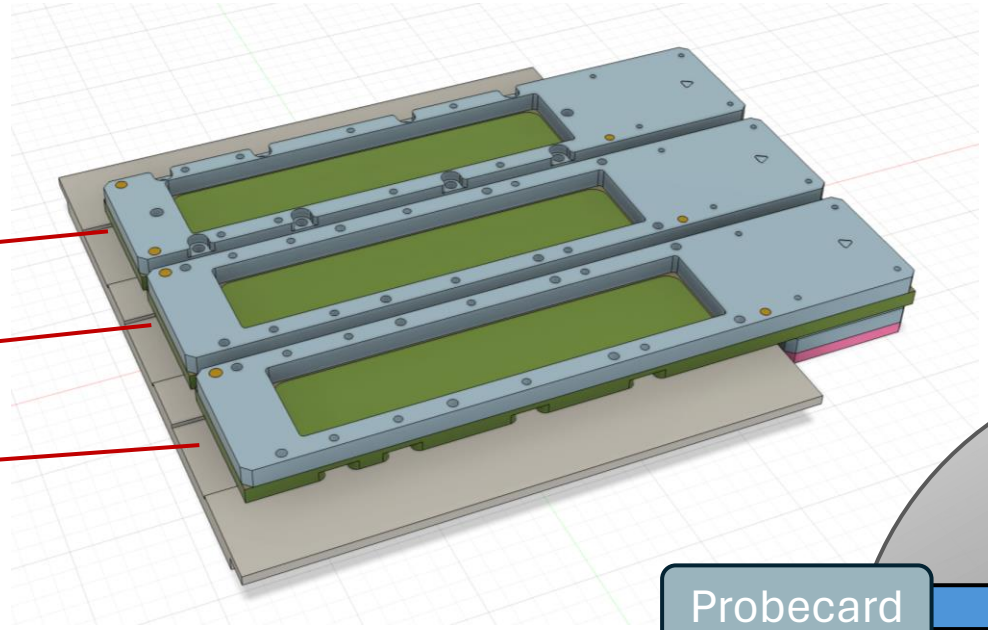


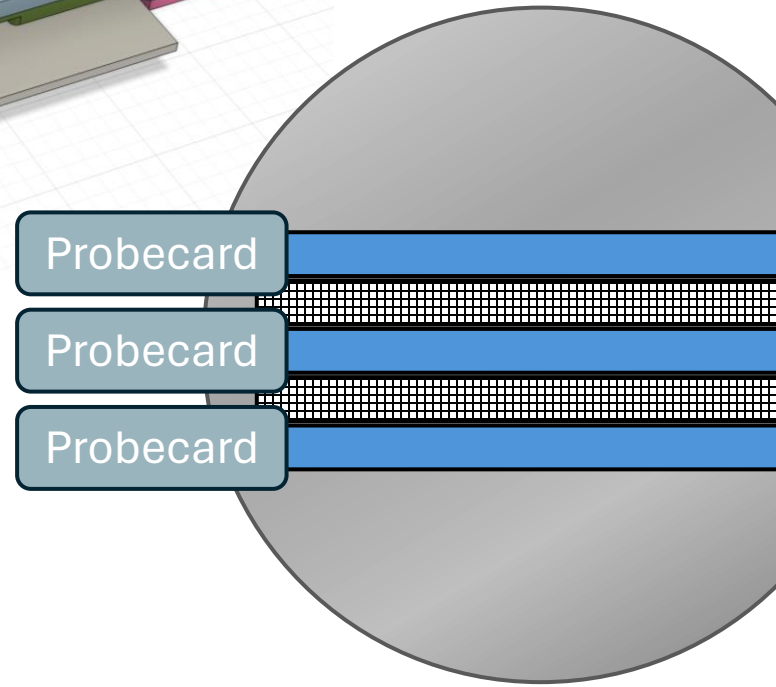
Parallelization of sensor testing:

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Wafer probing extensions and SVT QC







3x

Parallelization of se

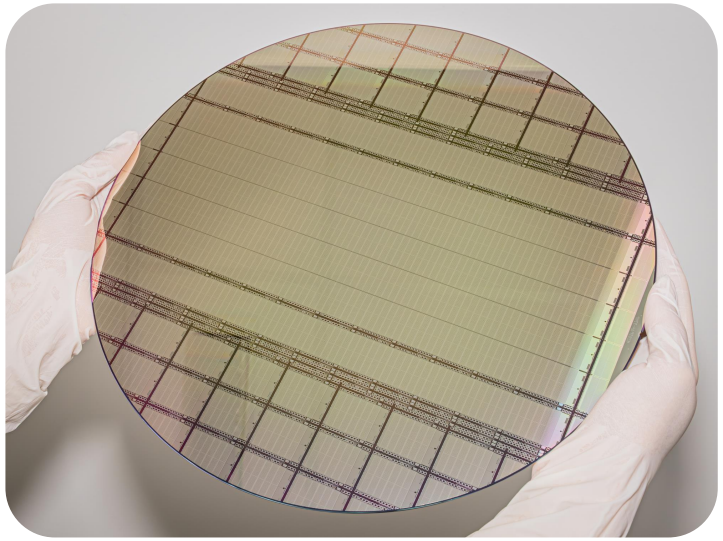
- Up to 3 SEG in par
  arrangement)
- Adaptable to LAS

Estimated reduction of total QC testing time for one site from **~560 to ~110 calendar days!**

Summary

MOSAIX chip (nearly) fully functional

- On track for ER3 submission by end of year
- Transmission weakness found and fix implemented
- Manufacturing yield improvement ongoing



Testing infrastructure for highly complex chip in full operation



Wafer probing at 10.24 Gbps achieved

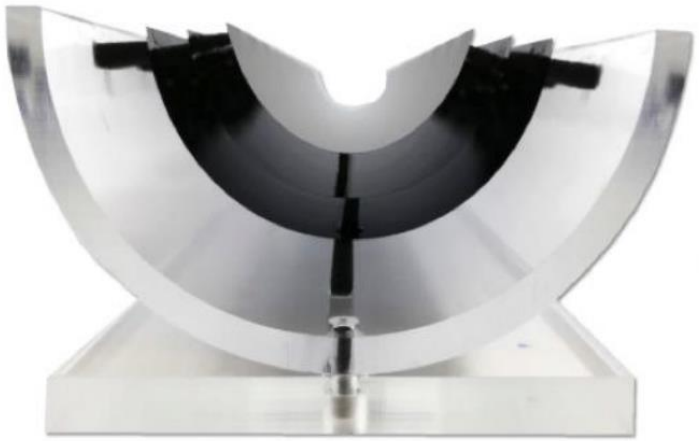
- Essential to fully exercise all chip blocks on-wafer
- Custom high-speed chain wafer-to-FPGA developed

High-volume SVT production QC readiness

- Dual-sided powering and multi-probecard system

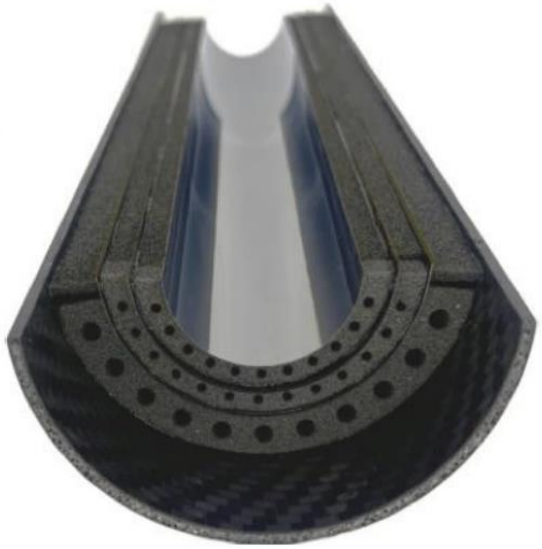
BACKUP

Mechanics integration



Engineering Model 1

Bending



Engineering Model 2

Cooling



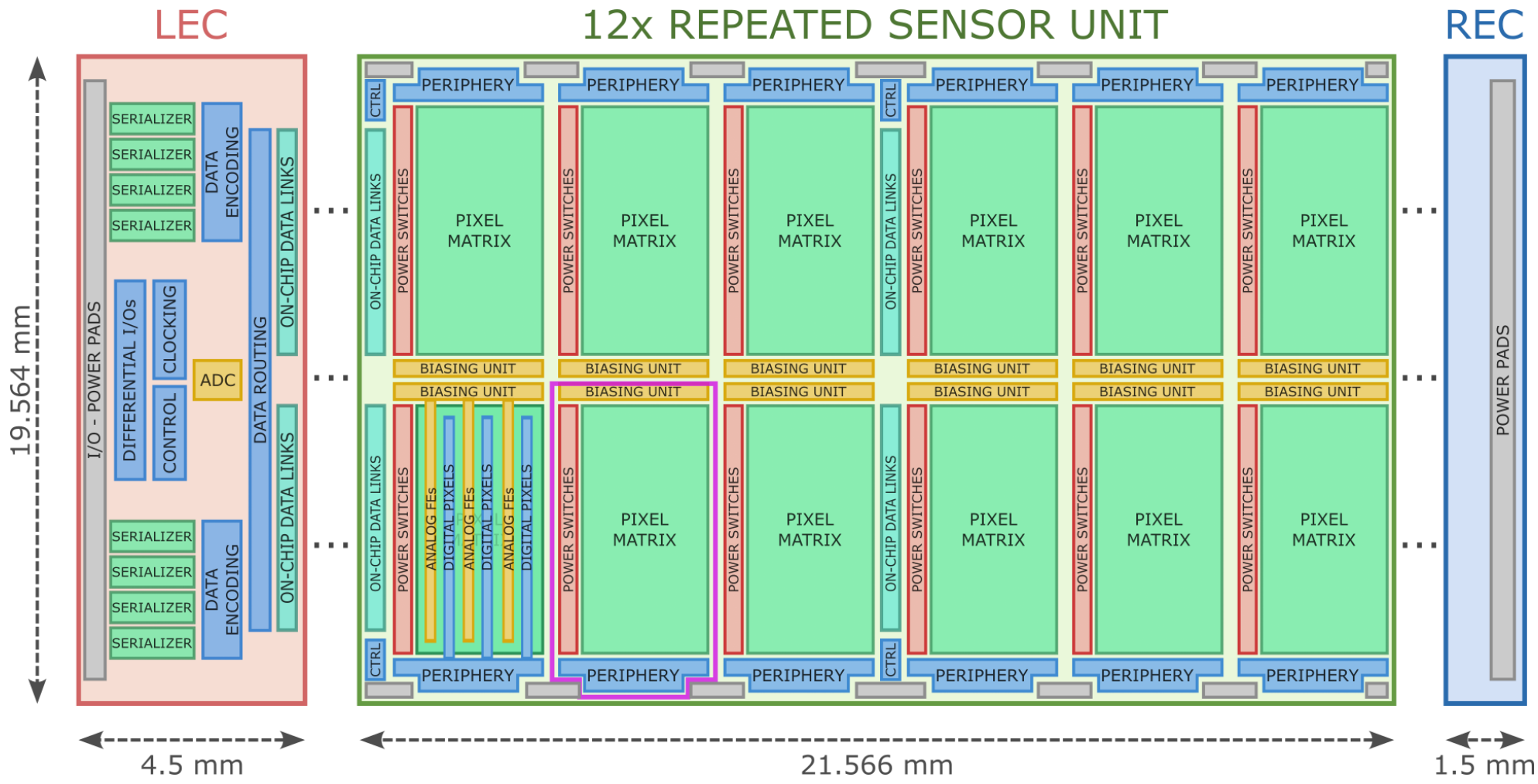
Engineering Model 3



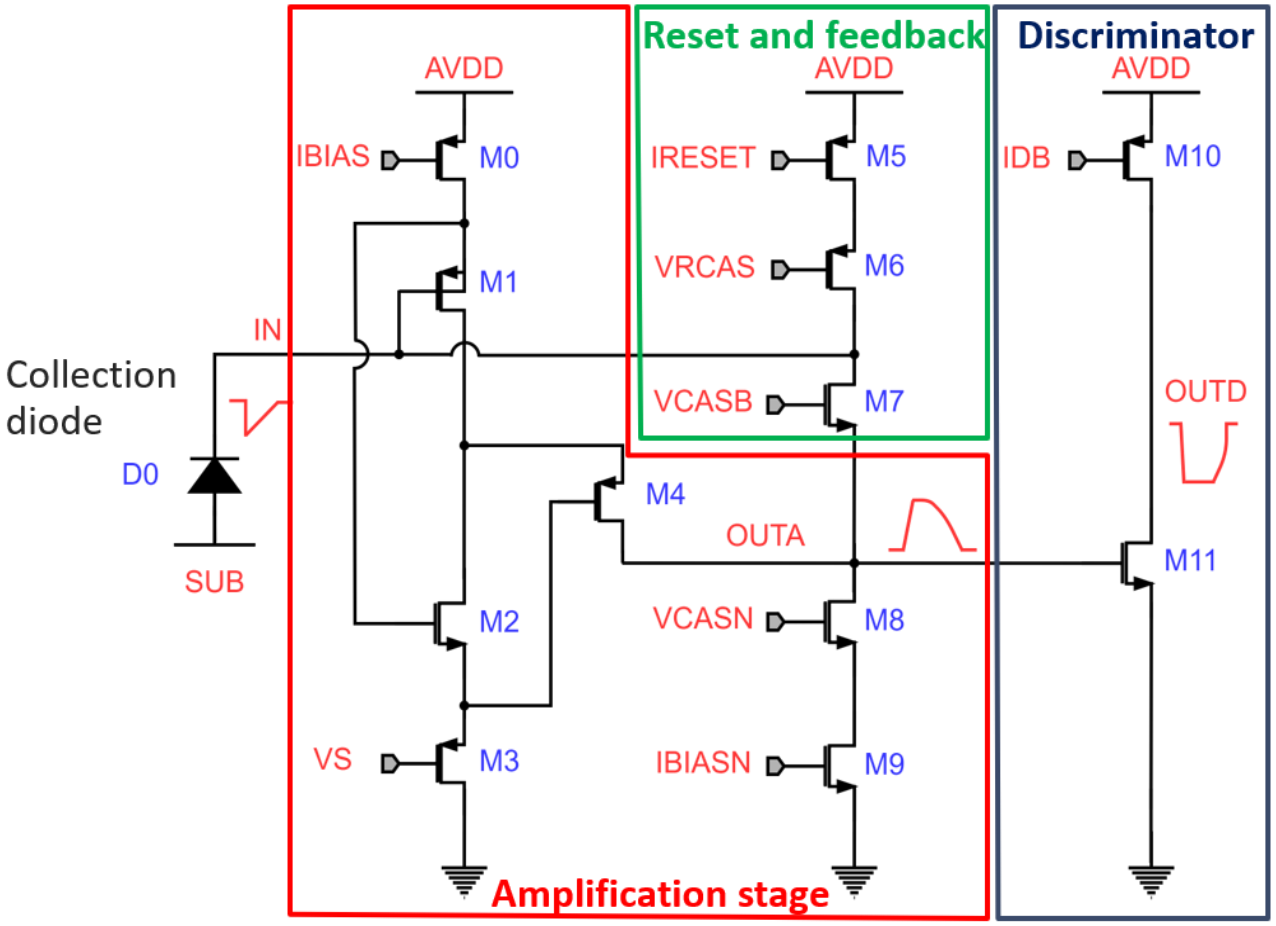
Engineering Model 4

Mechanical and Electronics Integration

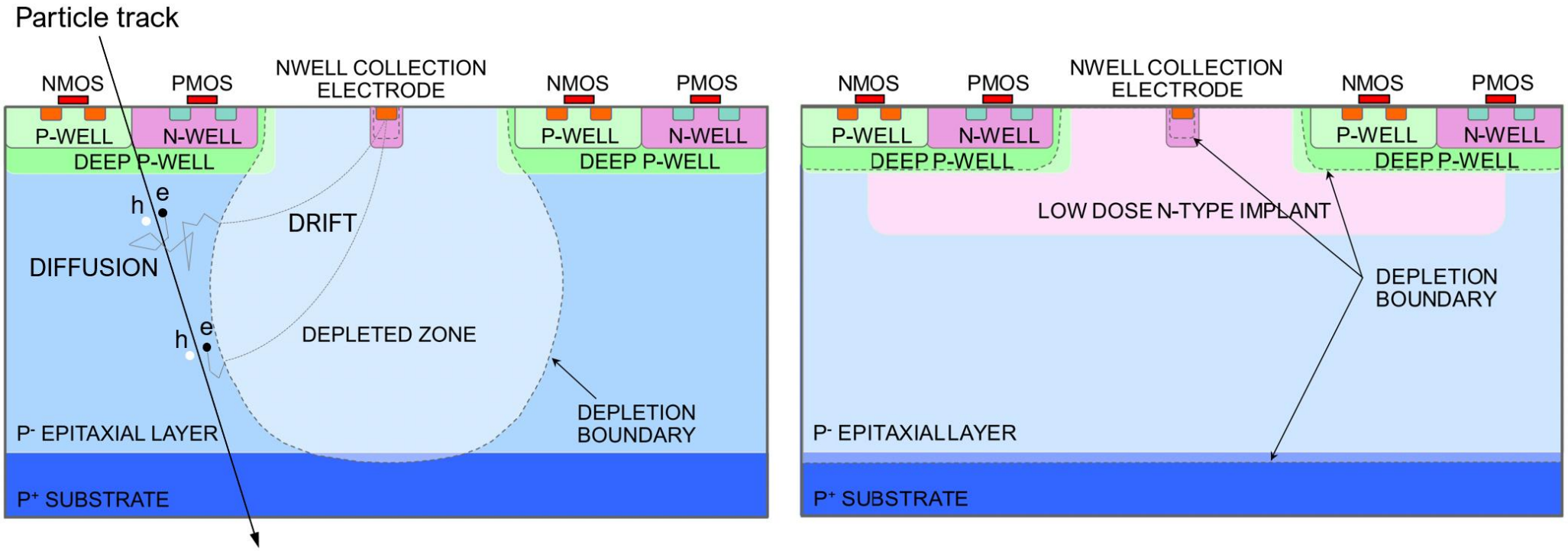
Block digaram detailed



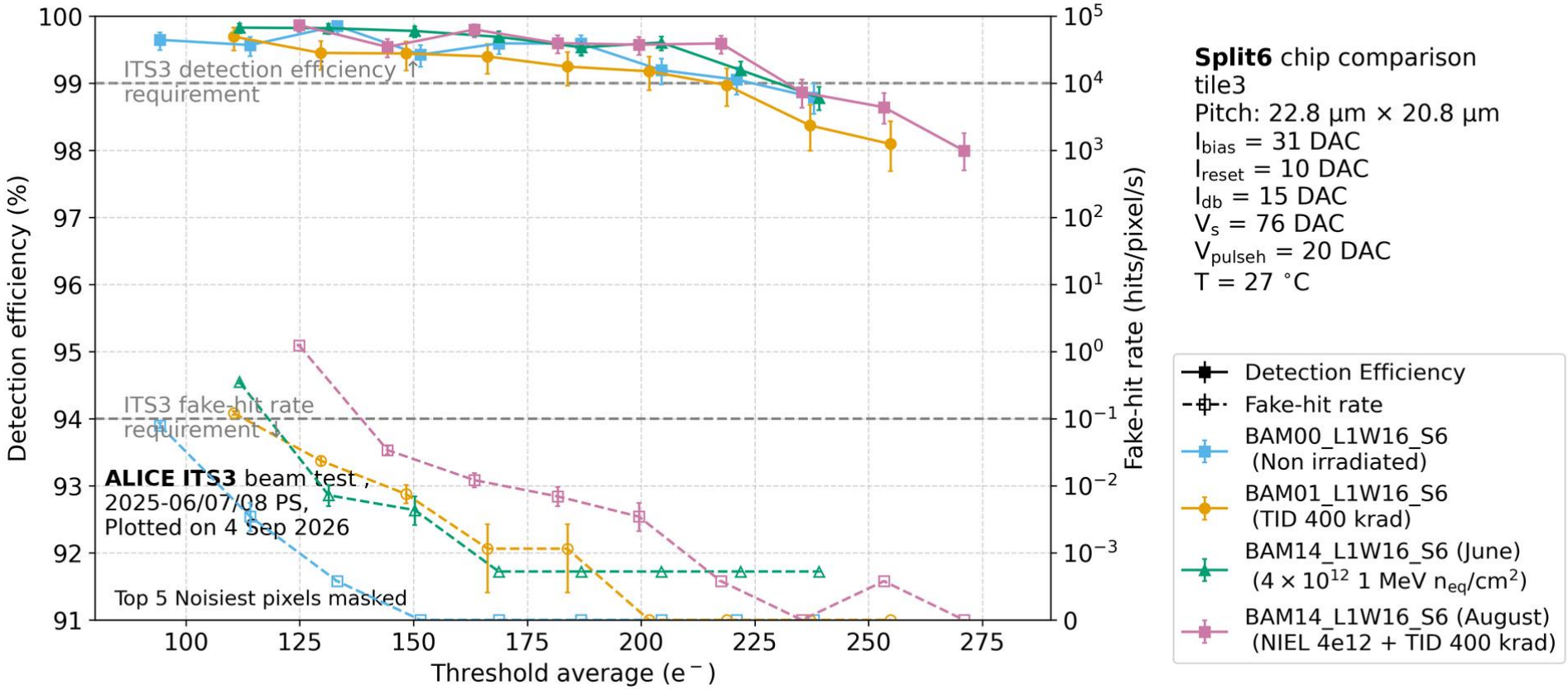
Analog pixel frontend



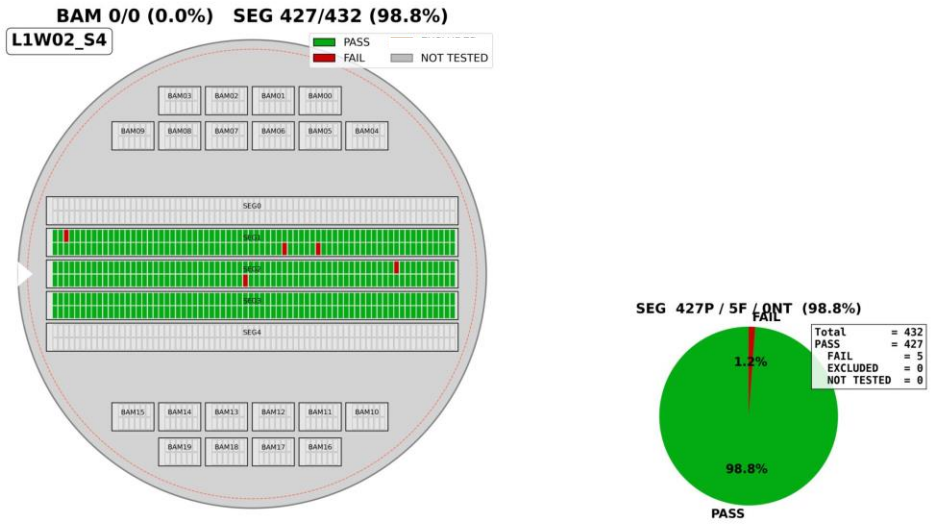
MAPS pixel cross section

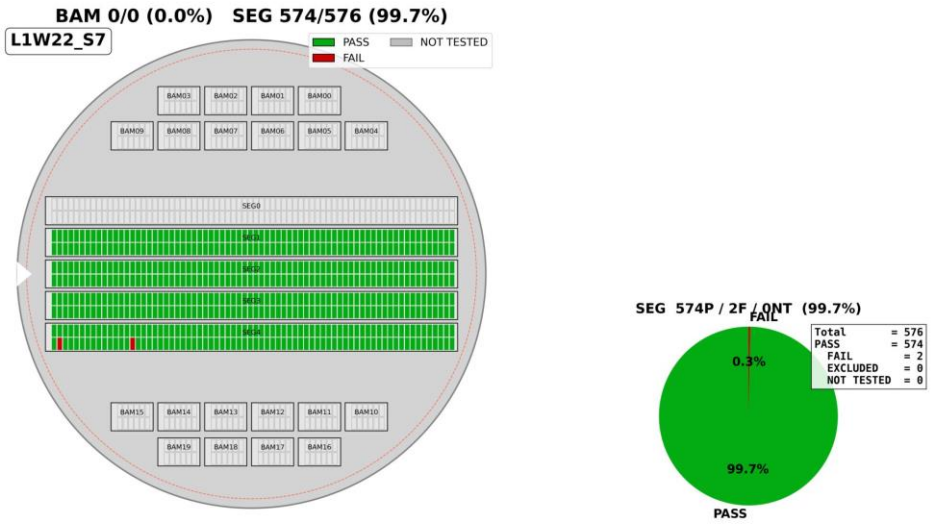


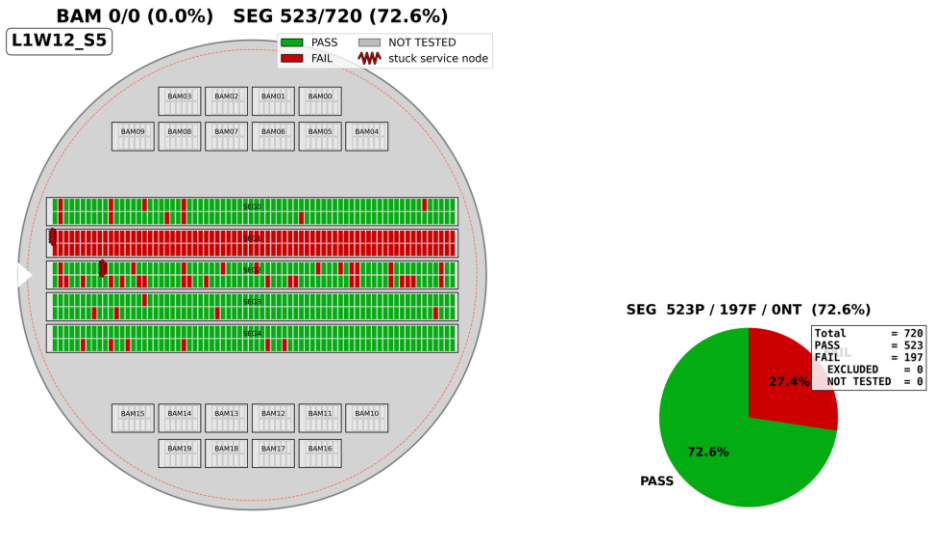
Testbeam - detection efficiency / fhr

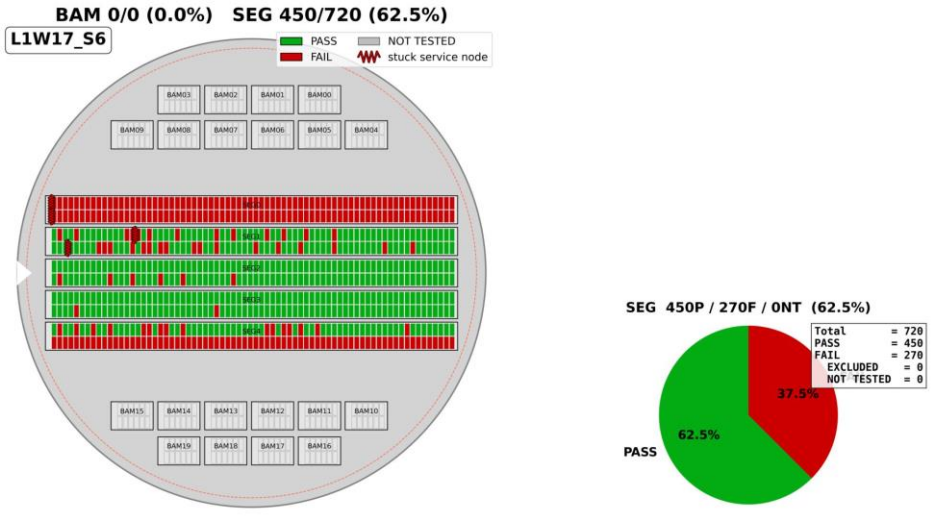


Yield – thinned layers example





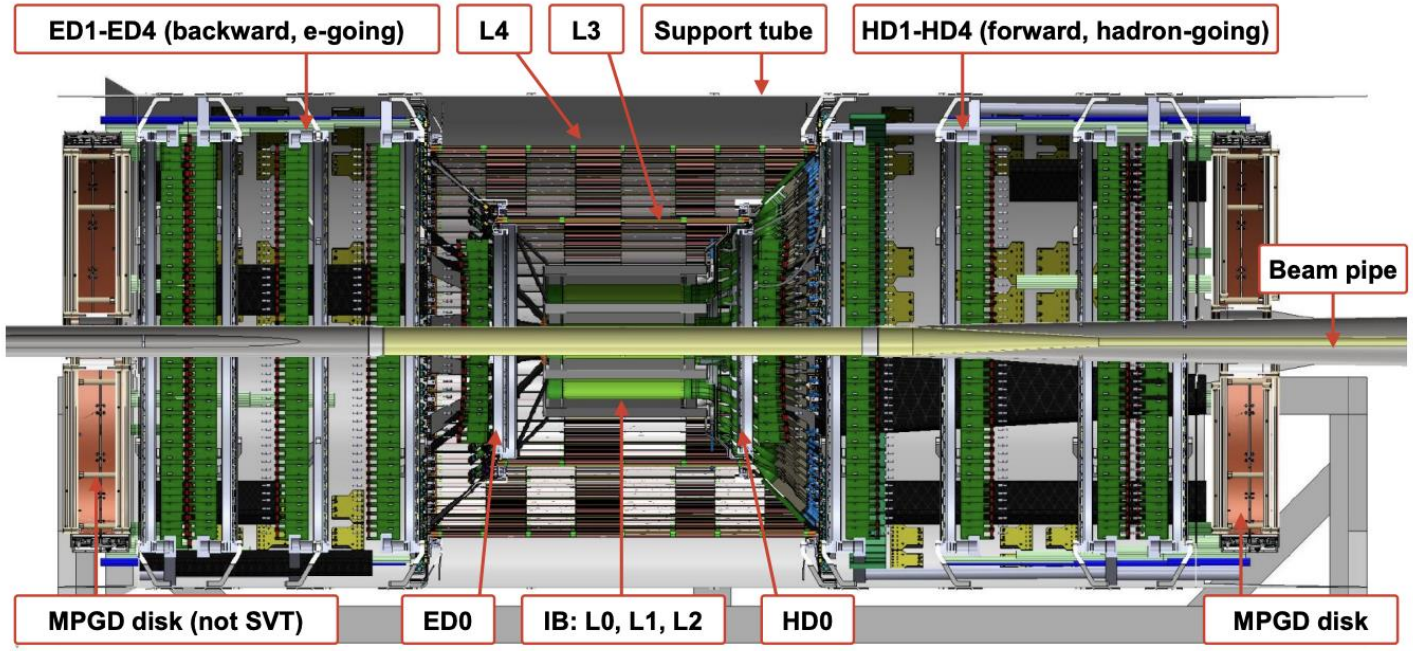




Thinned layers tile yield

- 1x L0: 99%
- 1x L1: 99%
- 2x L2: 73% / 63%

SVT



Overall
- -1.05 m < z < 1.2 m; r ≲ 0.43 m (active)
- ~8.5 m² of silicon – IB ~0.4 m², OB ~3 m², disks ~5 m²

Sensors
- MAPS in TPSCo 65 nm, ALICE ITS3 lineage
- Pixel 20.8 × 22.8 μm²; integration time ≤ 2 μs
- ~40 mW/cm² on the sensitive area

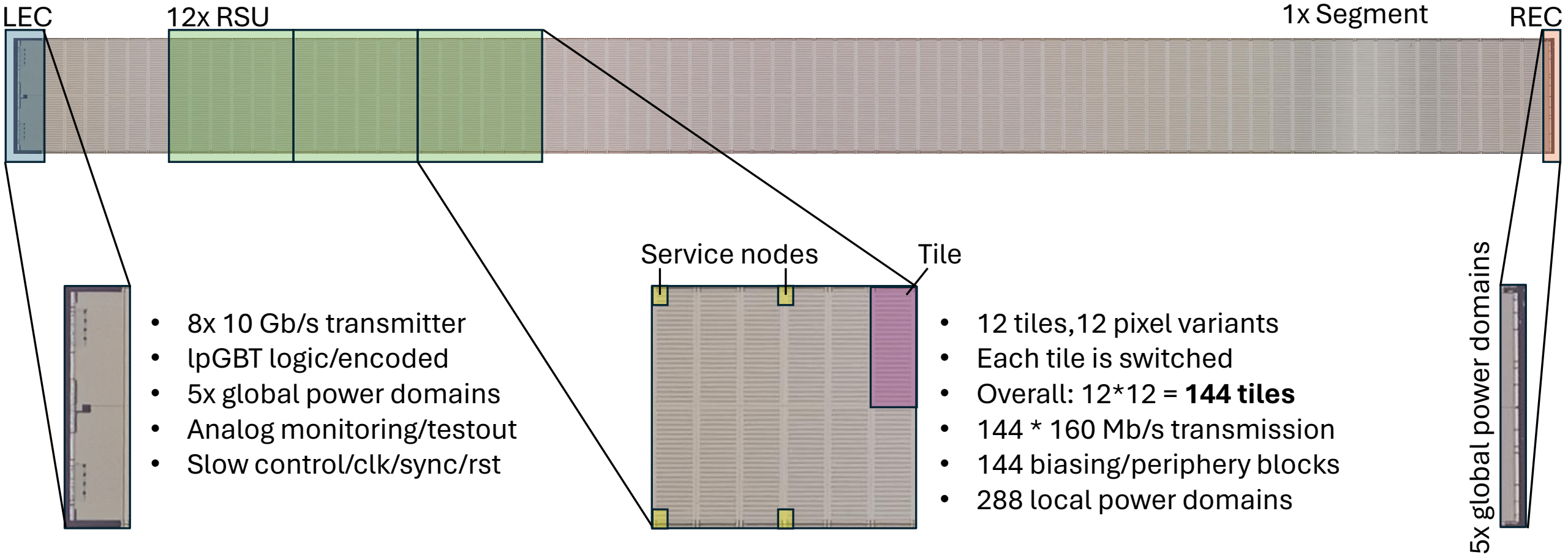
Mechanics, services, cooling
- Carbon foam / carbon-fiber composite supports
- Room temperature, air cooling
- Aluminum flexible printed circuits
- lpGBT, VTRx+; streaming readout

Inner Barrel (IB)
- L0, L1, L2 at r = 38, 50, 126 mm
- X/X_0 ≈ 0.07% per layer
- Bent, wafer-scale MOSAIX sensors
- Direct powering (ITS3 scheme)

Outer Barrel (OB)
- L3, L4 at r = 270, 420 mm
- X/X_0 ≈ 0.25% (L3), 0.55% (L4)
- Carbon-fiber staves; EIC-LAS sensors
- Serial powering via AncASIC

Endcap disks (ED, HD)
- Two arrays of five disks: ED0-4, HD0-4
- X/X_0 ≈ 0.25% per disk
- Corrugated carbon core; EIC-LAS sensors
- Serial powering via AncASIC

Mosaix anatomy



- 8x 10 Gb/s transmitter
- lpGBT logic/encoded
- 5x global power domains
- Analog monitoring/testout
- Slow control/clk/sync/rst

- 12 tiles,12 pixel variants
- Each tile is switched
- Overall: 12*12 = **144 tiles**
- 144 * 160 Mb/s transmission
- 144 biasing/periphery blocks
- 288 local power domains

One tile ~ one pixel sensor

Wafer prober upgrade

New platen, allowing for two probecards at once:

- Cantilever for REC powering (to be produced)
- Vertical for LEC (as is)
- Requires new microscope travel range

- Installation complete, incl. dark box (sources, laser)
- Taken into operation again

