

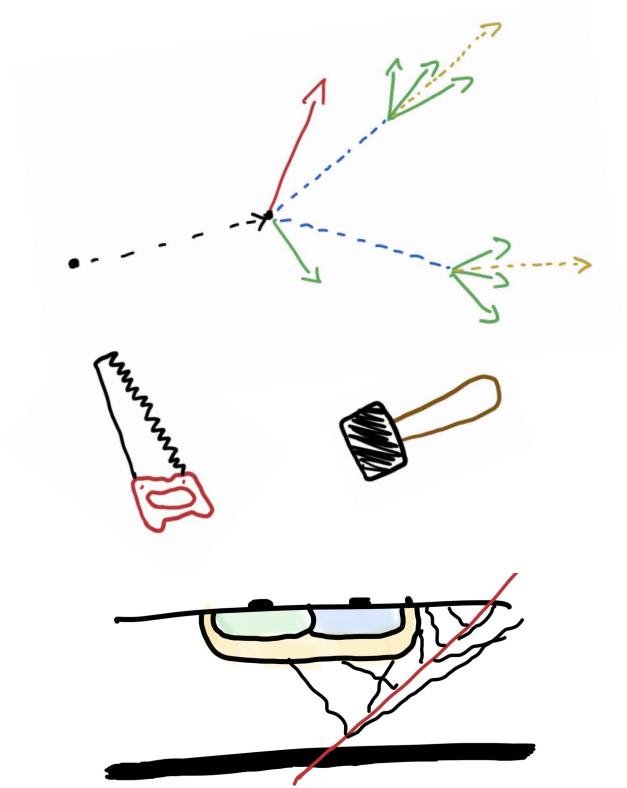
HV-MAPS Sensor Design and Simulations for FCC-ee

Doug Berry, Ron Lipton, Corrinne Mills, **Danush Shekar**

CPAD 2026 (October 21)



arxiv.org/abs/2610.28946



Outline

Vertexing at FCC-ee

MAPS R&D at FNAL

HV-MAPS design and performance

Conclusions and outlook

FCC e^+e^- goals and requirements

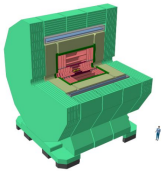
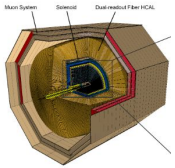
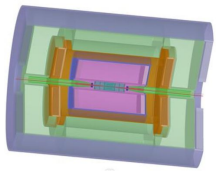
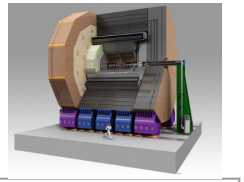
- Precision measurements of the Higgs boson, the W and Z bosons, and the top quark using collisions at center-of-mass energies ranging from 88 to 365 GeV.

- Vertex detector requirements:
  Excellent identification and lifetime measurement of long-lived particles such as heavy quarks and tau leptons

$$\sigma(d_0) = a \oplus \frac{b}{p \sin^{3/2}\theta}$$

Single-hit resolution ~3 μm
Trade-off between material budget, power consumption, and hit-rate capability
  - Low material budget < 0.2% X_0 per layer
  - Low power and air-cooled (<= 50 mW/cm^2)
  - Handle hit rates at O(100 MHz) during the Tera-Z program

FCC e^+e^- goals and requirements

Detector concept	CLD	IDEA	ALLEGRO	ILD
B-field [T]	2	2	2	2
Vertex inner radius [mm]	17.5	13.7	14	16
Vertex	**Si-pixel**	**Si-pixel**	**Si-pixel**	**Si-pixel**
Tracker	Si-pixel	Drift chamber, Si-strips	Si-pixel or Gas, Si-strips	TPC, Si-strips
Remaining subdetectors	Si-W ECAL, scintillator-steel HCAL, …	Crystal ECAL, scintillating fiber DR HCAL, …	Pb-LAr ECAL, scintillator-steel HCAL, …	Si-W ECAL, scintillator-steel HCAL

All detector concepts propose Silicon-pixel sensors for vertexing

D. Dannheim, FCC week 2026, arxiv.org/abs/1911.12230, arxiv.org/abs/2502.21223, indico/6214312/, arxiv.org/abs/1306.6329

Vertexing at FCC e^+e^-

Approximate performance (requirements) at other experiments

Experiment/ subdetector	Spatial resolution (um)	Material budget ($\%X_0$)	Rad. hardness (n_{eq}/cm^2)
ALICE ITS2	~ 5	0.36	~ 1.7×10^{12}
ALICE ITS3	< 5	0.05	< 10^{13}
Belle II VXD	10 - 15	~ 0.3	~ 10^{14}
ALICE 3 tracker	2.5	< 0.15	~ 10^{15}
FCCee VTX	3 - 5	< 0.3	~ 10^{13}

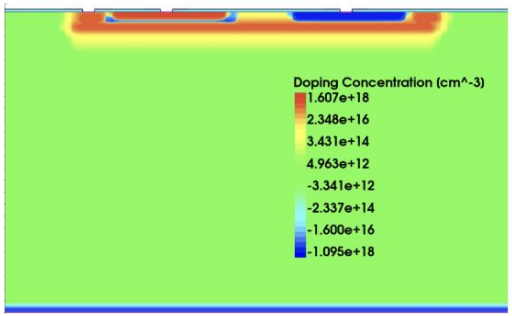
Successful demonstration of MAPS technology in other current or upcoming detectors with similar/worse experimental conditions. Future R&D needed for aspects like power, rate, etc.

Inspired from J. Baudot, FTCF workshop 2024

MAPS R&D at Fermilab

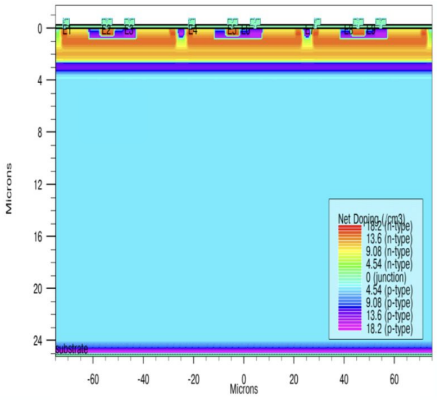
Investigations of multiple MAPS designs are underway.
Currently at simulation/design stage, but end-to-end pipeline (design to laboratory characterization) is envisioned.
Broad exploratory studies now; future work will narrow scope to specific detector requirements.

High-voltage MAPS (HV-MAPS)

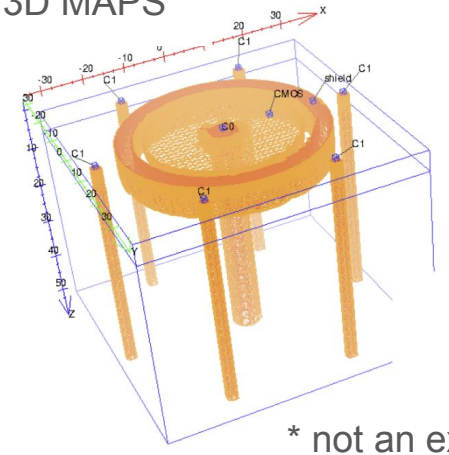


This talk

MAPS with gain layer



3D MAPS

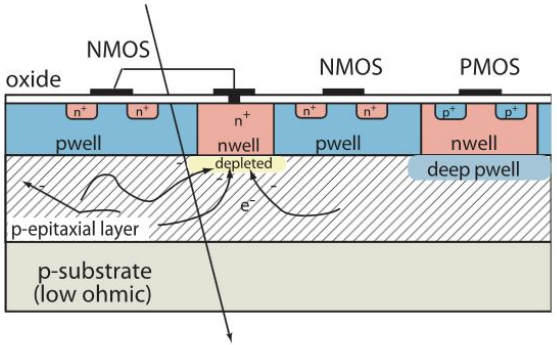


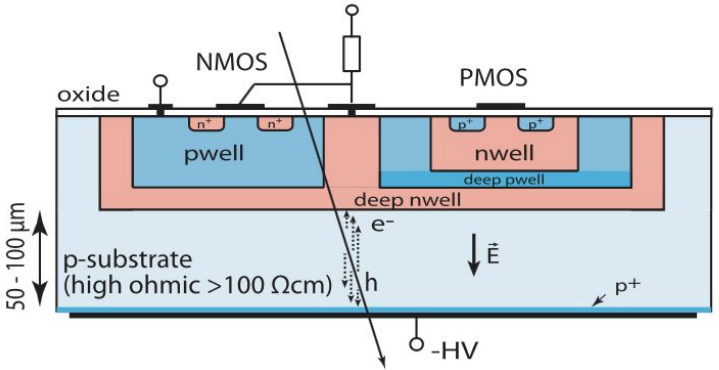
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* not an exhaustive list!

MAPS vs HV-MAPS

MAPS





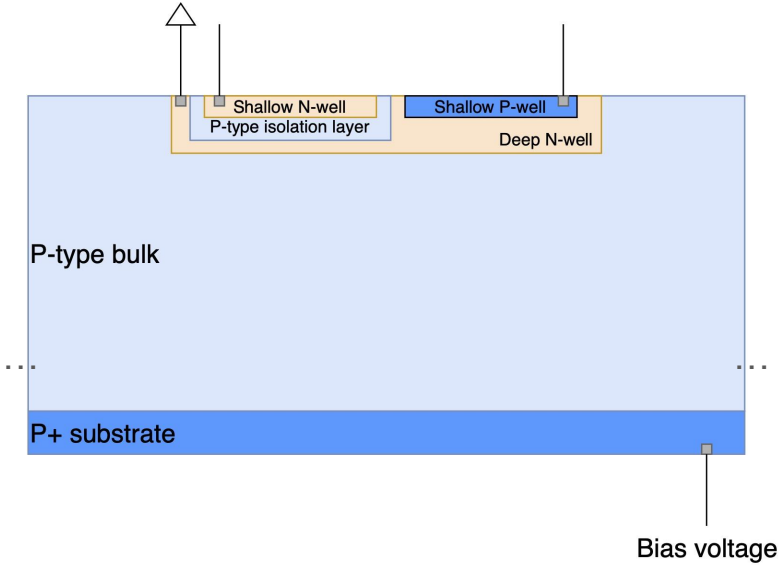
HV-MAPS

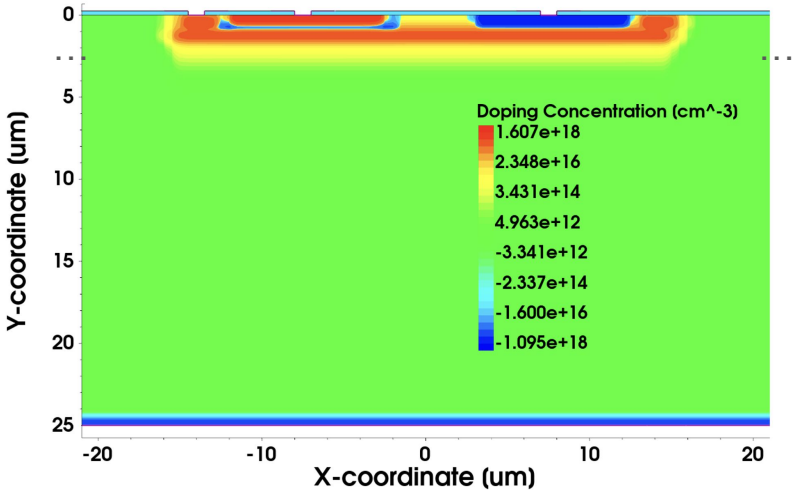
- Active volume/depletion zone
- Mechanism of charge collection
- Implant design and placements
- Capacitance, signal rise-time, radiation-hardness …

- High-bias voltage operation to withstand expected radiation environment at FCC-e^+e^-
- The effects of increased depletion width needs to be carefully evaluated across metrics like S/N, power, spatial resolution, etc.

Rep. Prog. Phys. 81 (2018) 066101

HV-MAPS design





- 2D process+device simulations (Sentaurus Synopsis) of 3-pixel HV-MAPS structure
- 25 µm thick sensor, pixel pitch of 50 µm, bulk resistivity of ~13 kΩ.cm
- Two shallow N-type (SNwell) and P-type (SPwell) implants as placeholder for CMOS circuitry
- Deep N-type well (DNwell) encapsulating the shallow well, with a P-type isolation layer separating the SNwell and DNwell

Outline of design optimization

The design parameters all the top-side implants were varied independently in a series of parameter scans to assess their individual effects on device performance.

Several metrics were used in this assessment:

1. **Maximum electric field in hotspots** within the silicon volume
   (ensures operation below the sensor breakdown threshold)
2. The electric **field magnitudes within the shallow implants**
   (avoid high electric fields in the sensitive circuitry that these implants will contain)
3. The **total sensor capacitance** and inter-implant capacitance
   (minimize to reduce noise when coupled to the readout chain)
4. The **signals induced at all contacts by MIPs**
   (maximize charge collection at the DNwell contact, minimize charge collection at the shallow-implant contacts)

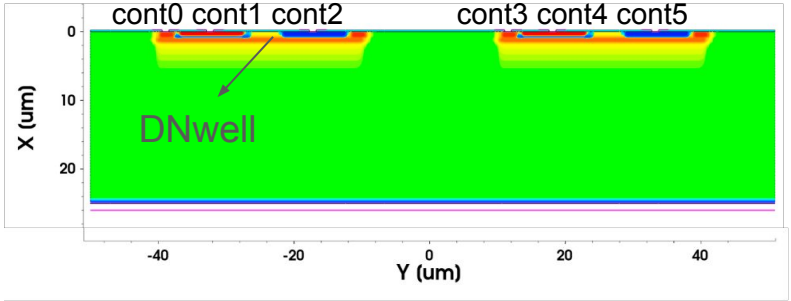
After optimizing all design parameters, the DNwell parameters were re-optimized to ensure closure.

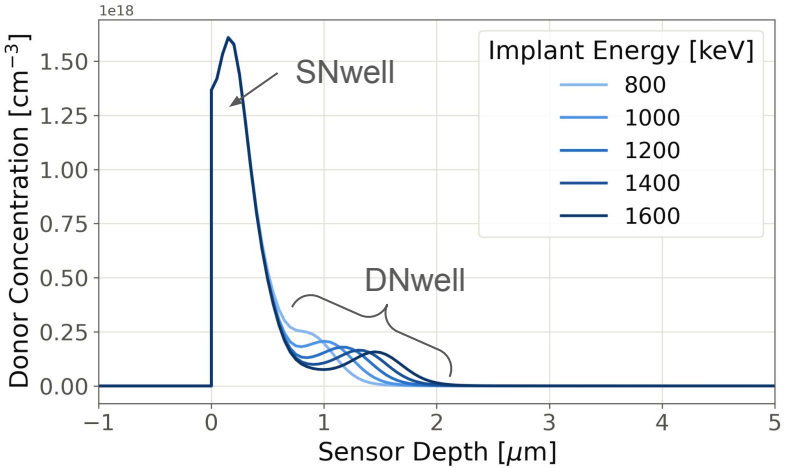
HV-MAPS design optimization

Results from DNwell implantation energy optimization will be discussed here - in the interest of time, but contains all key-takeaways.

The implantation energy of the DNwell (EDNwell) was varied to obtain different implant depths; following values were considered:

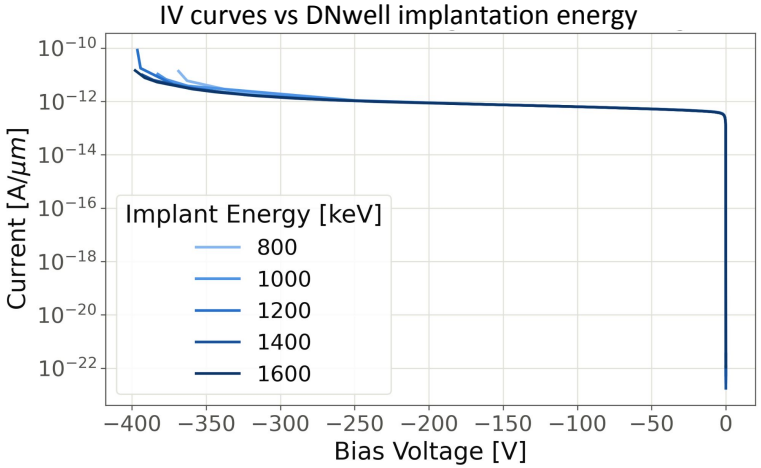
1.800 keV
2.1000 keV
3.1200 keV
4.1400 keV
5.1600 keV

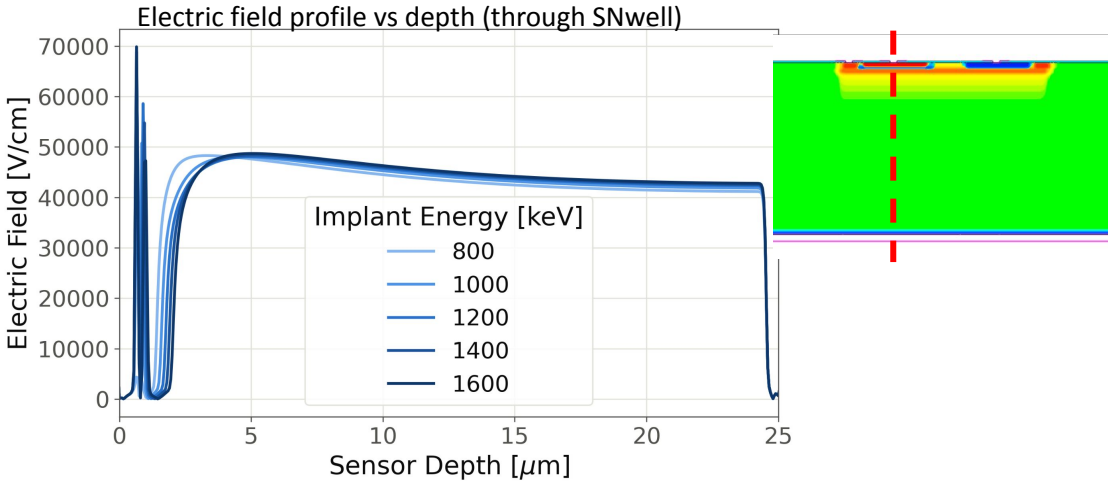




Additional 200 keV energy gets you roughly 0.15 µm of added depth

HV-MAPS design optimization

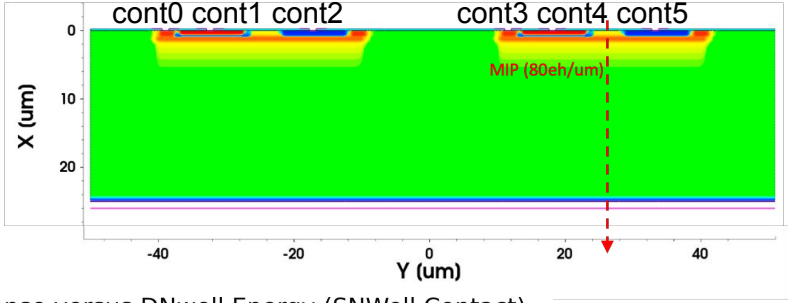


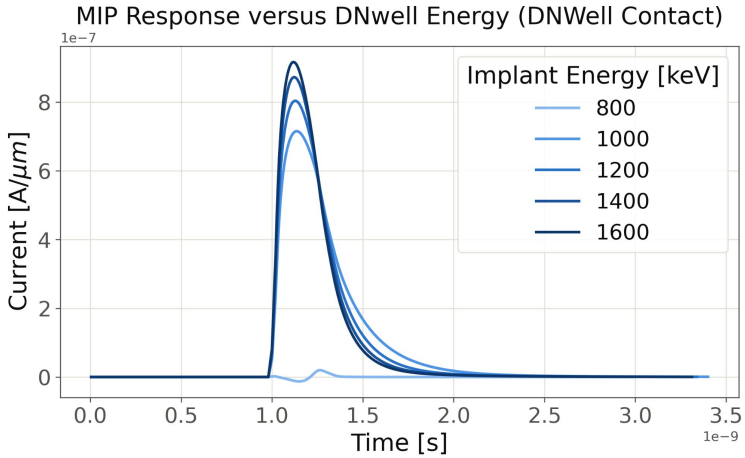


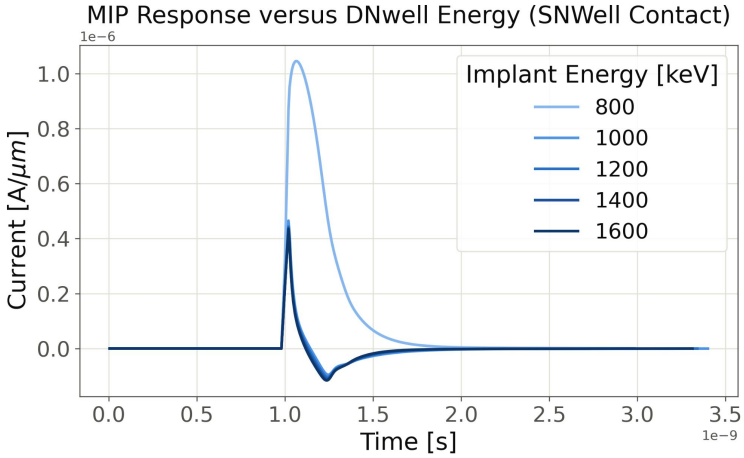
- Max operational voltage (because of the maximum electric field within silicon volume) increases with depth of the DNwell.
- Increasing depth of DNwell slightly increases electric field in the bulk, but however also increases the magnitude of electric field spikes near the transistor region.

HV-MAPS design optimization

Transient response for normally-incident MIPs (80 eh/μm) passing through the center of a pixel

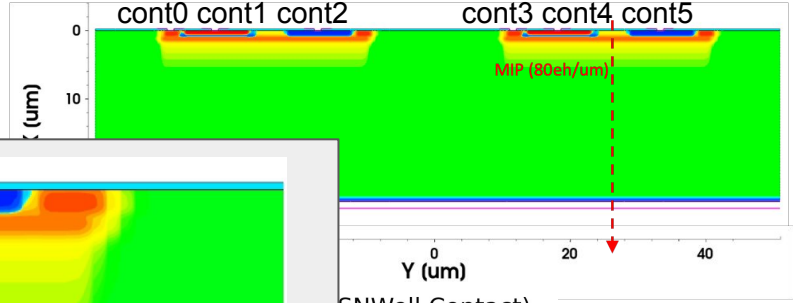






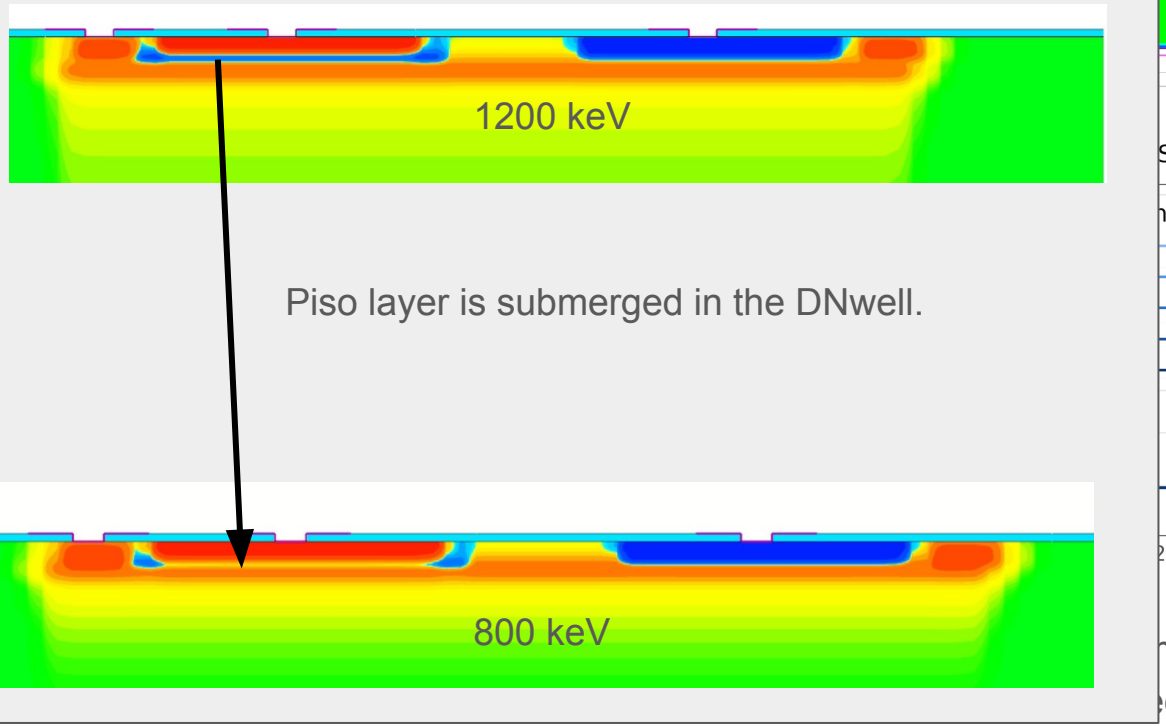
Increasing depth of DNwell increases amplitude of signal but total charge roughly remains the same. DNwell with implant energy = 800 keV is not optimal, a bulk of the signal gets induced on SNwell because the P-type isolation layer is “submerged” in the DNwell.

HV-MAPS design optimization



Transien

passing



MIP Re

SNWell Contact)

Increasing

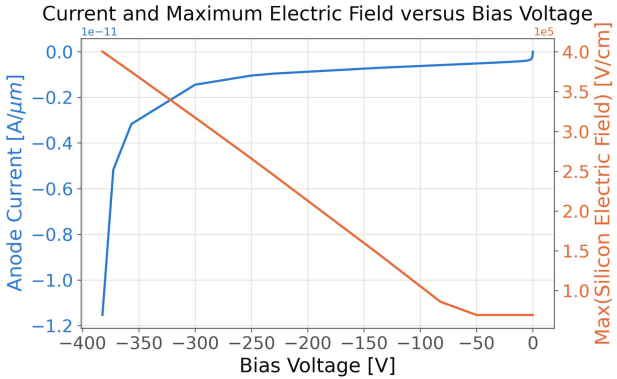
mains the same.

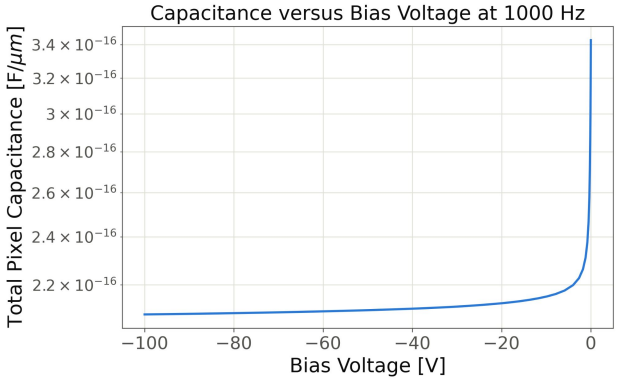
DNwell w

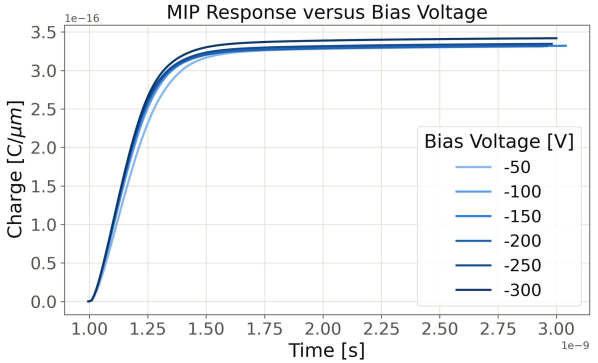
d on SNwell because the P-type isolation layer is “submerged” in the DNwell.

Optimized HV-MAPS properties

- Optimization of design parameters of all implants, including the closure test of DNwell implant parameters were completed.



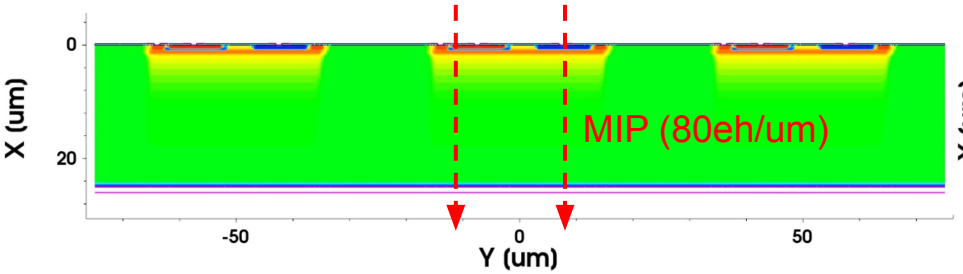




- Properties of final design: depletion voltage = ~3V, breakdown voltage = ~300 - 390V.
- No strong dependence of charge collected vs bias voltage for normally incident MIPs; reasonable bias of 100V was chosen to be operational bias voltage for further studies.

Simulated performance of optimized HV-MAPS

MIP response vs impact position

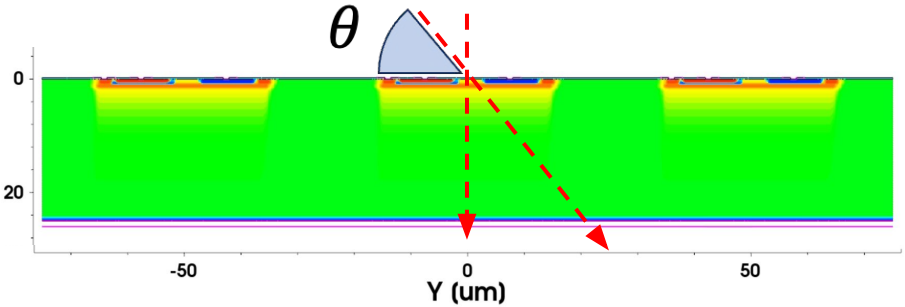


Considered values: 15, 10, 5, 0, -5, -10, -15, -20, -25 μm

Charge collection efficiency (CCE) definitions:

Leading-pixel CCE ("Leading DNwell CCE") =
charge collected by the leading DNwell electrode
total charge deposited by the MIP

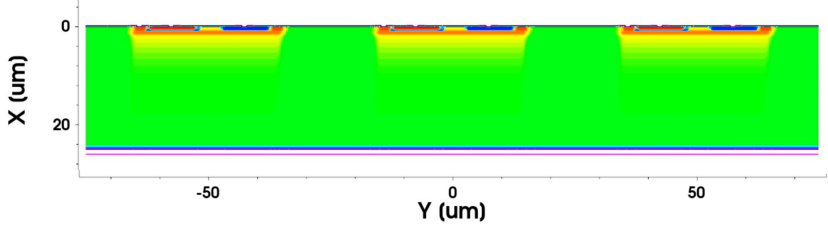
MIP response vs incident angle



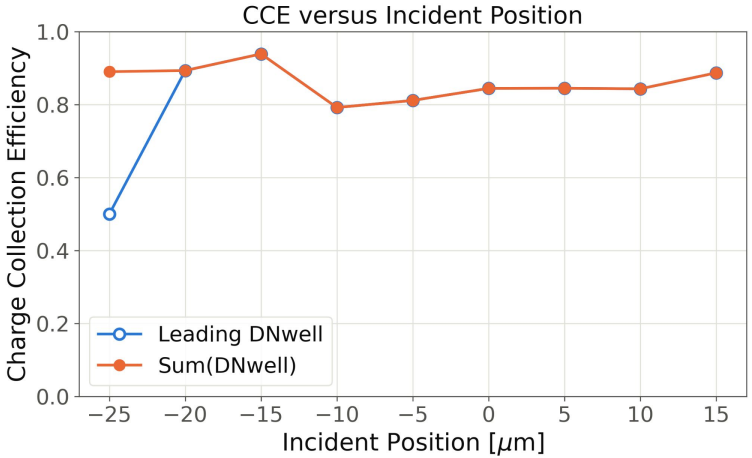
Considered values: 90, 75, 60, 45, -45, -60, and -75 deg

Summed CCE ("Sum(DNwell) CCE") =
charge collected by all DNwell electrodes
total charge deposited by the MIP

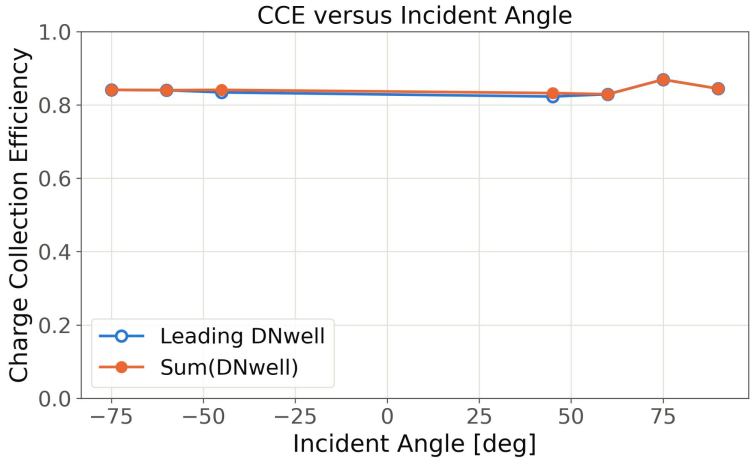
Simulated performance of optimized HV-MAPS



MIP response vs impact position



MIP response vs incident angle



- CCE vs impact position: 90% outside the well regions and 80% within them,
  CCE vs incident angle: roughly independent on the angle of incidence.
- For all incident positions and angles simulated: CCE >= 0.8, corresponds to >= 1600 electrons.

Summary and outlook

- Design of an HV-MAPS pixel structure for the vertex detectors of FCC e^+e^- experiments was presented
- Implant structures were optimized, and characteristic properties were studied.
- Charge collection efficiencies for MIPs at various incident positions and angles were quantified

- Update current implant structures with design files from foundry
- Study the effects of radiation-induced damage
- Perform three-dimensional simulations to obtain more precise estimates of spatial resolution and charge sharing
- Once the design is finalized, test structures will be fabricated at a foundry and characterized through laboratory and test-beam measurements.

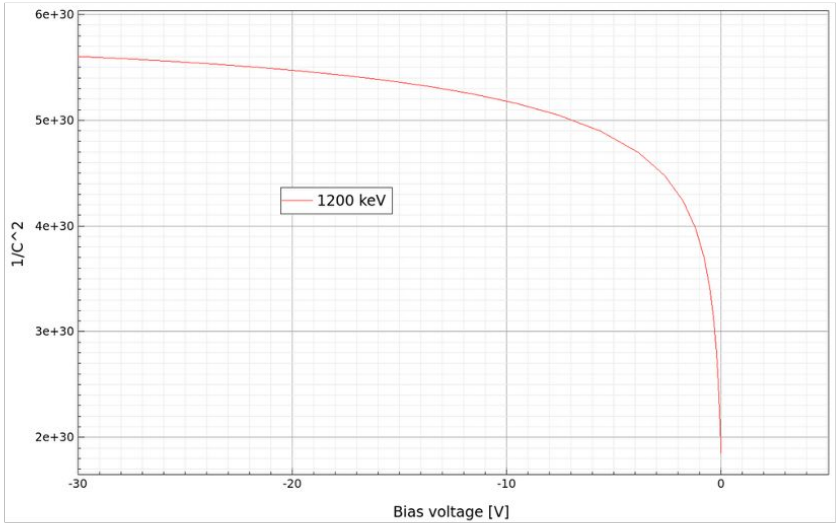
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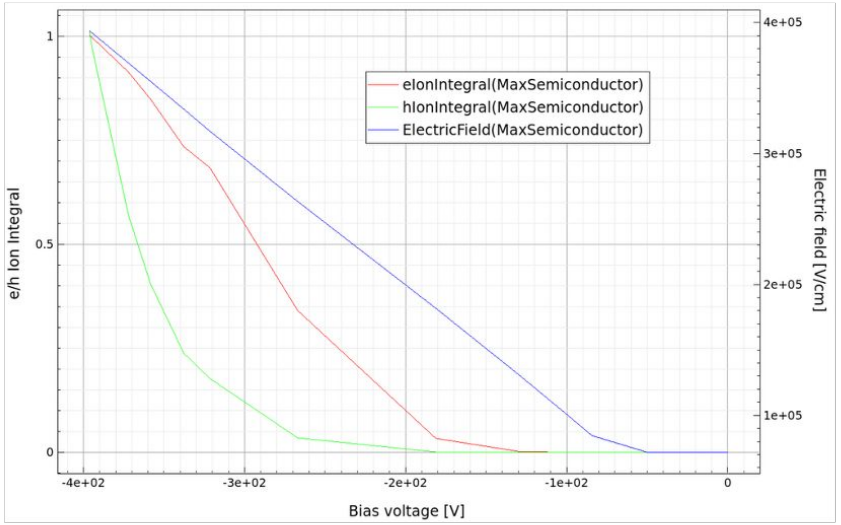
arxiv.org/abs/2610.28946

Backup

Operating voltage range

1/C² vs. bias voltage (1 kHz frequency) for 1200 keV EDNwell





Depletion voltage = ~3 V

Theoretical expectation ~ 0.5 V

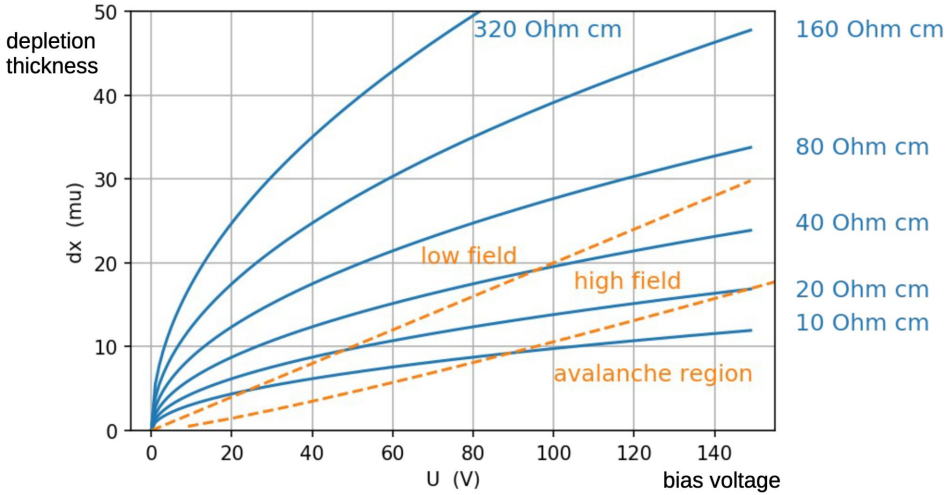
$$V_{\mathrm{dep}} = \frac{q\,|N_{\mathrm{eff}}|\,d^2}{2\,\varepsilon_{\mathrm{Si}}}$$

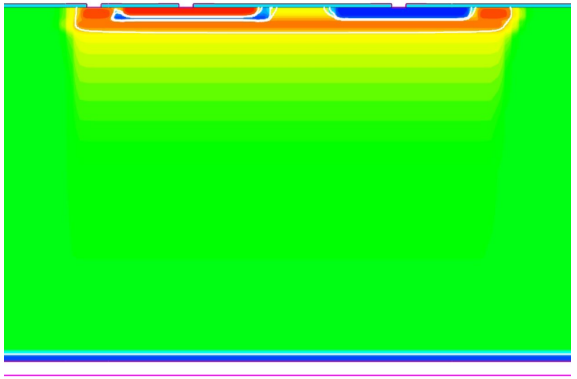
Breakdown appears to be around 300-400V range

Assuming avalanche effects start at ~3x10^5 V/cm

From ion integral curves

Operating voltage range





Junction line at 100V bias

A. Schöning, NuFact workshop 2021