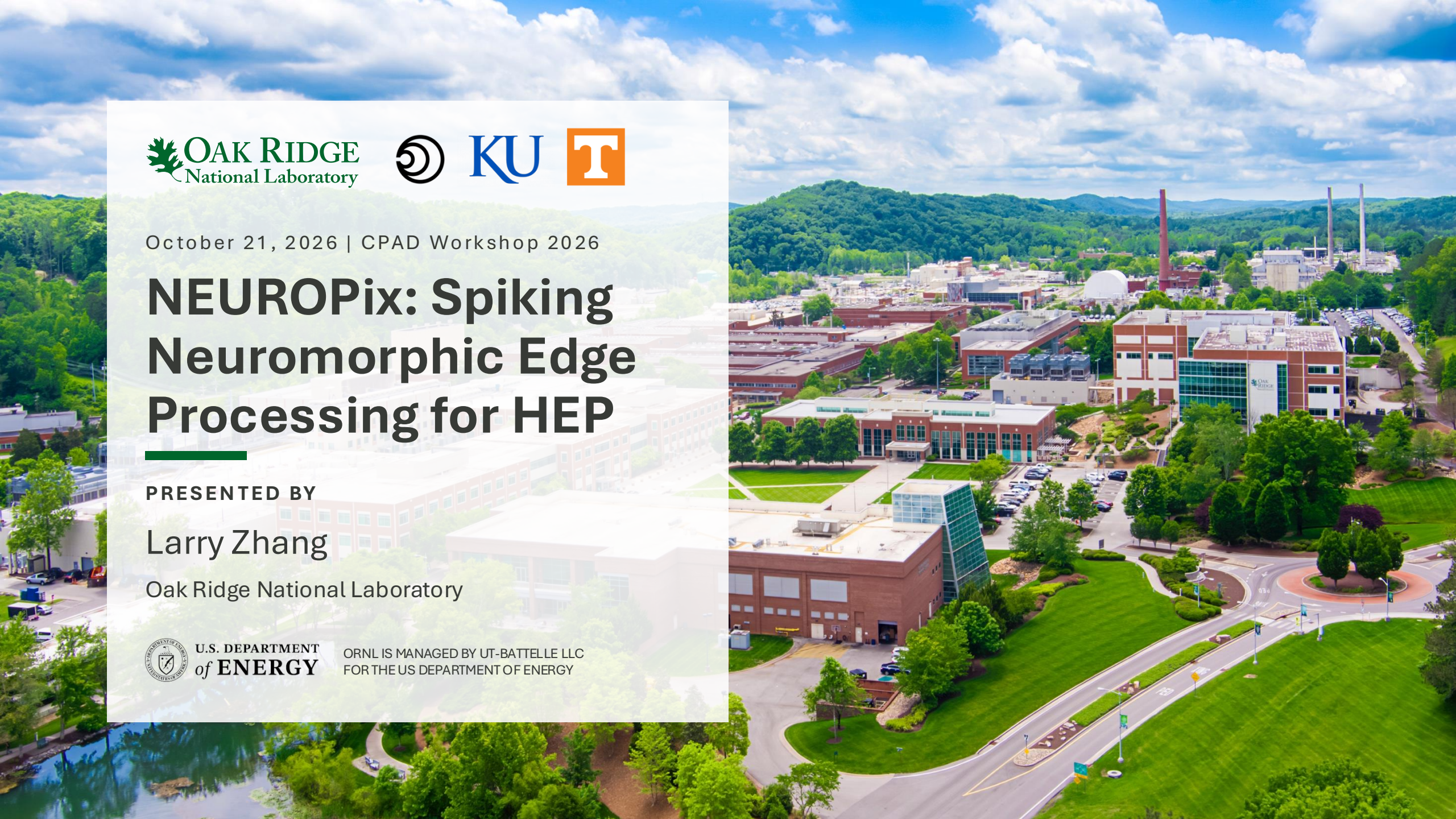


October 21, 2026 | CPAD Workshop 2026

NEUROPix: Spiking Neuromorphic Edge Processing for HEP

PRESENTED BY

Larry Zhang

Oak Ridge National Laboratory

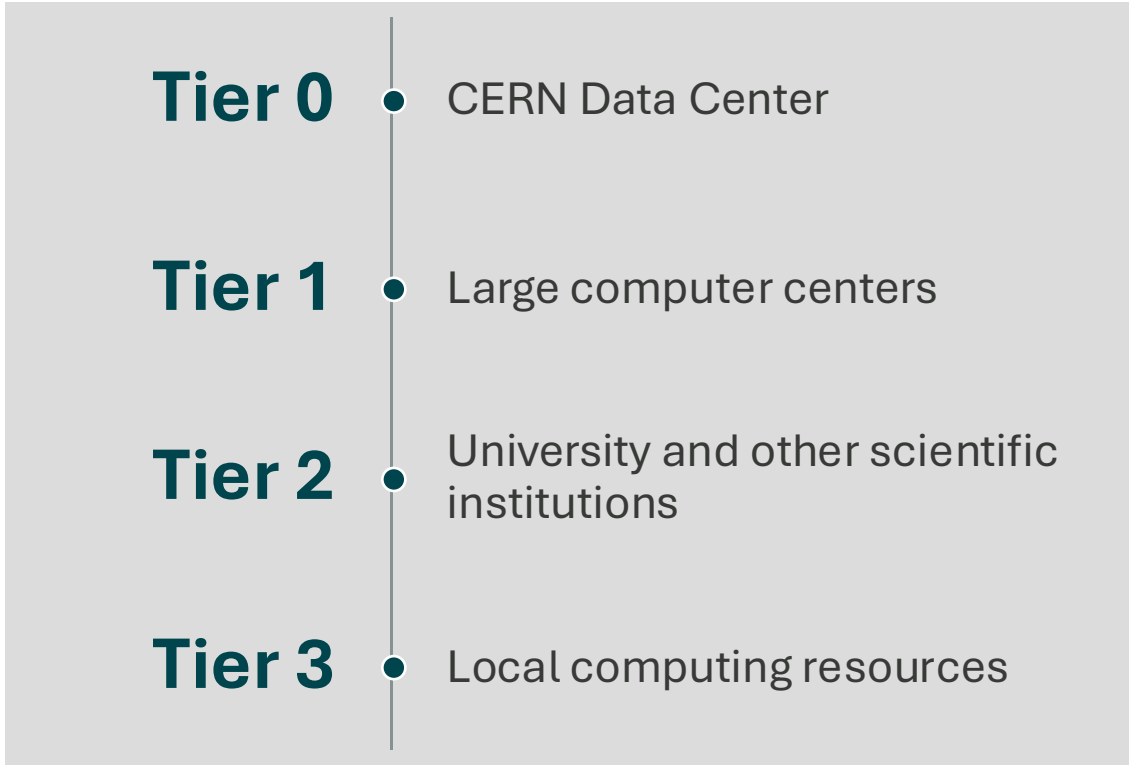
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Challenges faced by the current LHC computing model.

- The Worldwide LHC Computing Grid (WLCG) distributes research computing capacity across 4 “tiers”.
- This model did not anticipate current state of hardware and HEP funding.
- We are currently in Long Shutdown 3 in the transition to High-Luminosity LHC.
- This is when the next computing model will be decided.

The WLCG Model:



Hardware Challenges in 2026:

3–5×

Increase in DRAM prices since August 2025 [1]

2–4×

Increase in enterprise storage costs over last 2 years [2]

~50%

DRAM and NAND material cost contributions for a new server [2]

NEUROPix is tasked with finding edge computing solutions for HEP with spiking neuromorphic algorithms.

Overall Goal: Embed an SNN onto an FPGA to process pixel detector data streams on the edge for HEP applications.

Task 1

- Improve realism of interactions in Allpix^2 [3].

Task 2

- Add GPU acceleration to Allpix^2 simulations.

Task 3

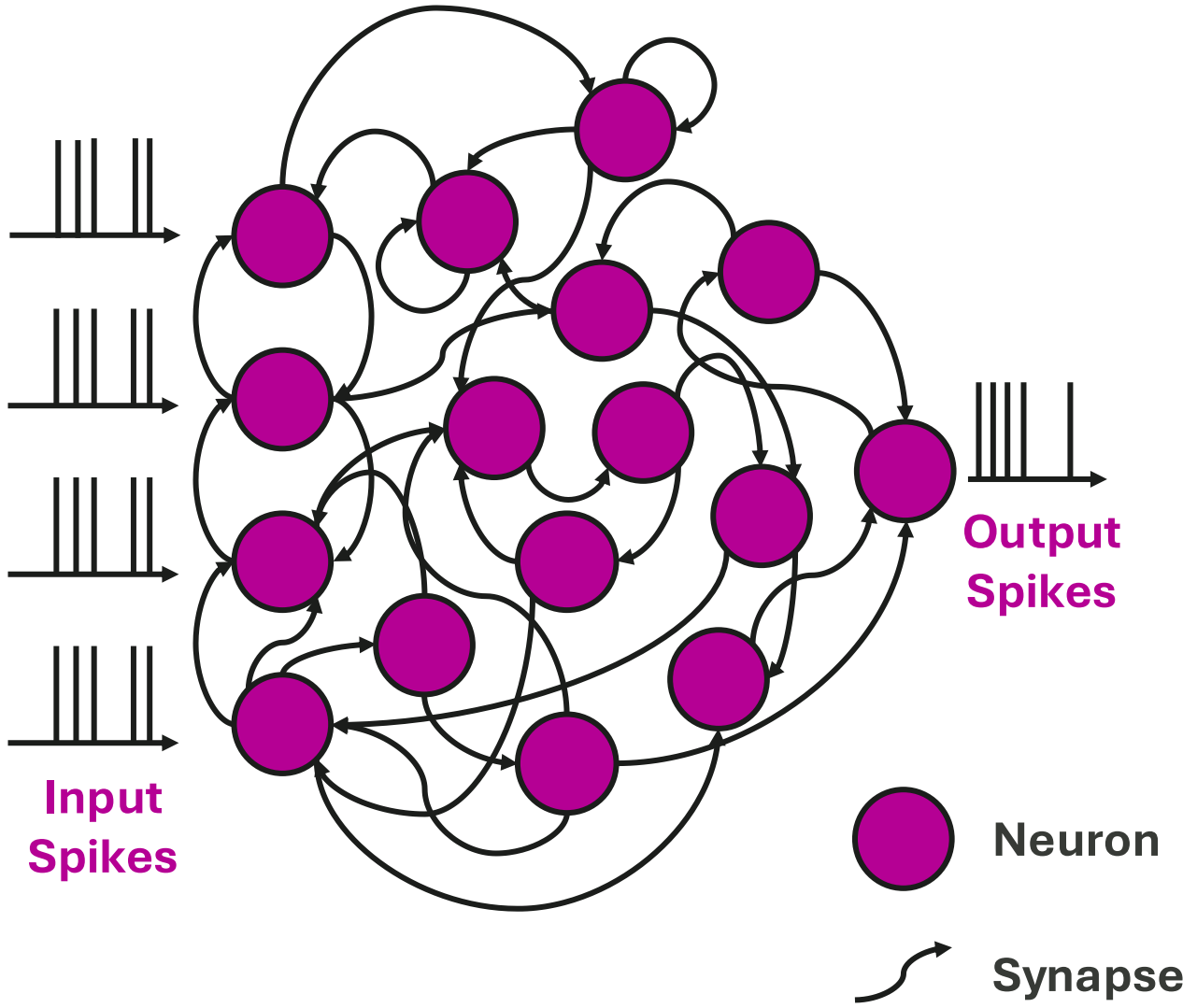
- Train Spiking Neural Network (SNN) on simulated data.

What are Spiking Neural Networks?

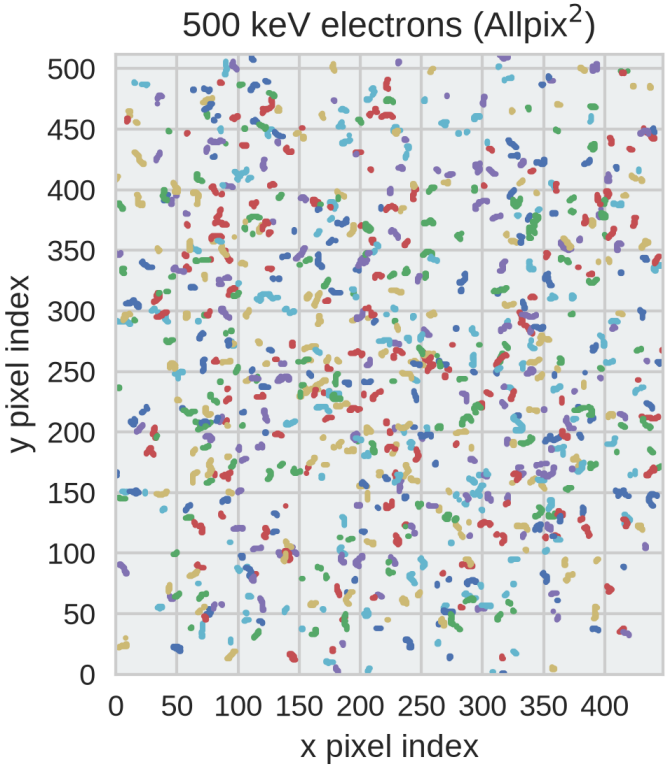
Properties of ORNL SNNs:

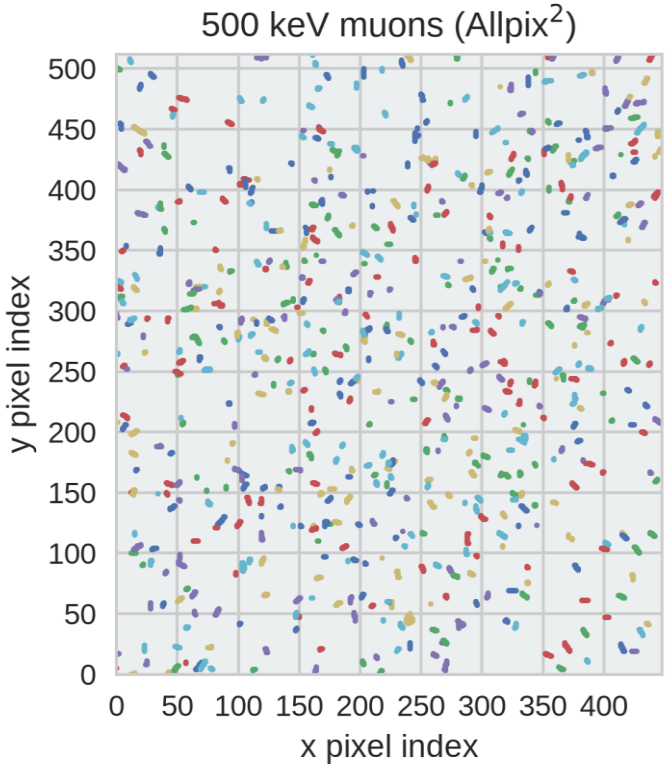
- Inspired by biological neurons
- Event-based
- Enforce sparsity
- Highly recurrent
- Extremely low latency
- Extremely low power

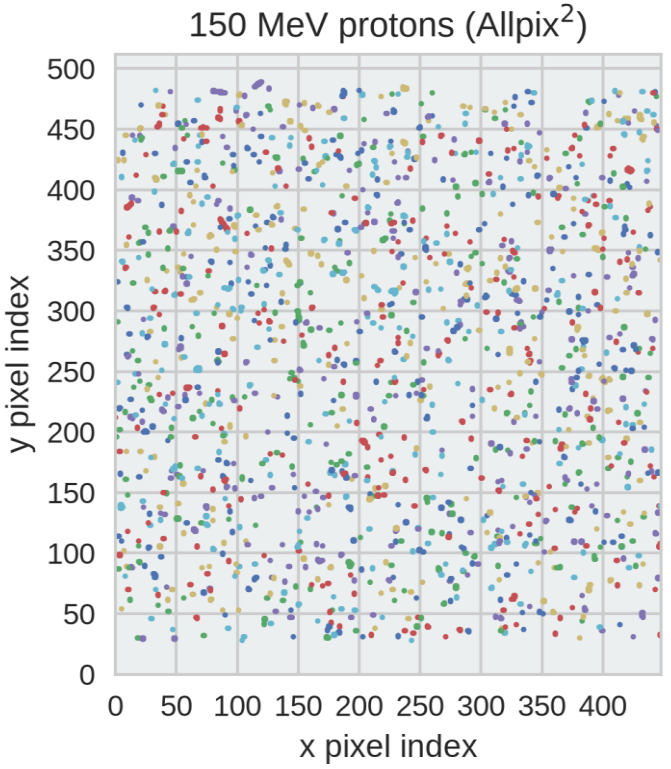
Spiking Neural Network generated with TENNLab genetic algorithm (illustration).



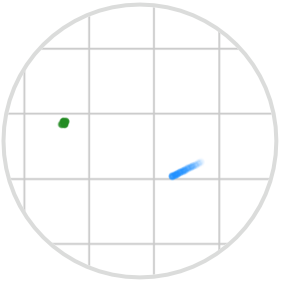
Generating data with Allpix^2, as well as an interim approach.







- Simulate response of Timepix4 chip [4].
- Worked on generating runs of various monoenergetic particles.
- Begun data-mixing process, to create realistic training data.
- Training on simpler case with fewer clusters in the interim (right).



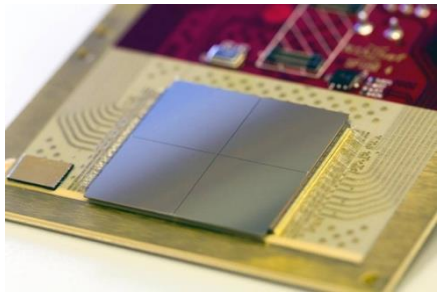
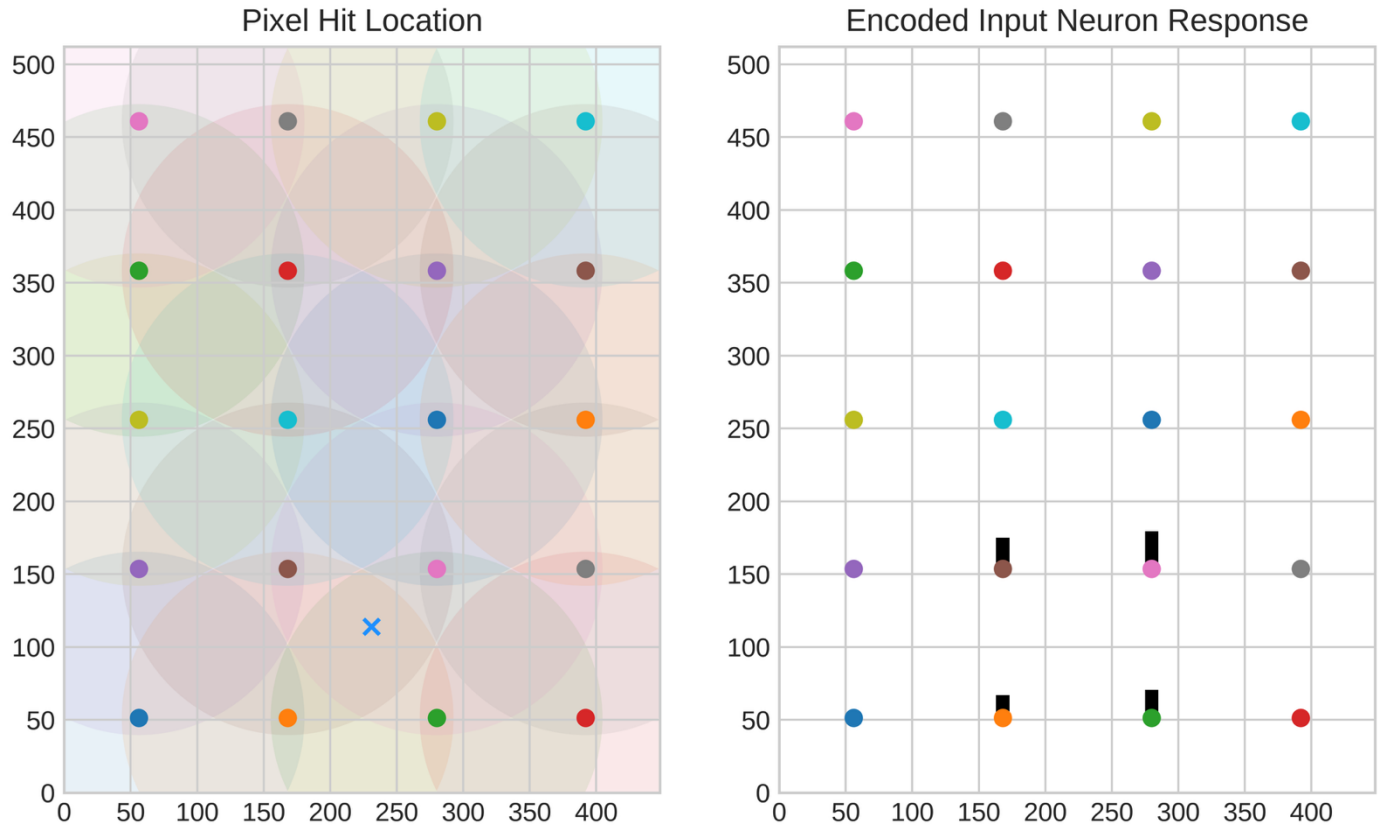


Image credit:
CERN document server

Encoding pixel hit events as spiking inputs.

- With highly recurrent model, input neurons are expensive, and compact networks are preferred.
- Timepix4 resolution is 448 × 512.
- Require methods to convert pixel detector data stream to input spikes, with few input neurons.
- Several “encoding” schemes are explored, with one example on the right.



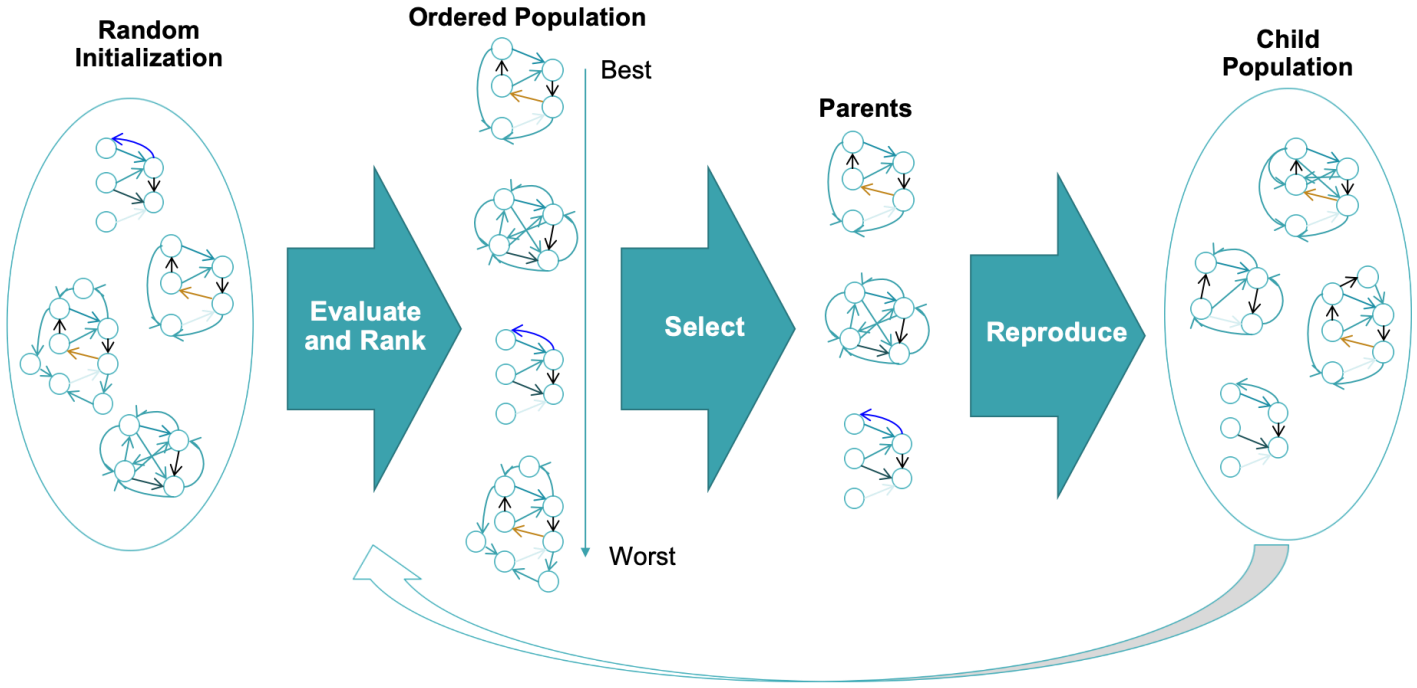
Steps for “Distance-Based” Encoding:

1. Assign input neurons to locations on detector grid.
2. Give each input neuron a circular region to monitor.
3. Set neuron firing strength proportional to distance of each incoming pixel hit to center of neural region.

Training a population of SNNs with an evolutionary approach.

- We use the LEMONS (Leveraging Evolutionary Multiobjective Optimization for Neuromorphic Systems) training algorithm developed by UTK.
- Allows for multi-objective optimization.
- Current fitness functions:
    - Accuracy
    - Dynamic Time Warping (DTW) distance

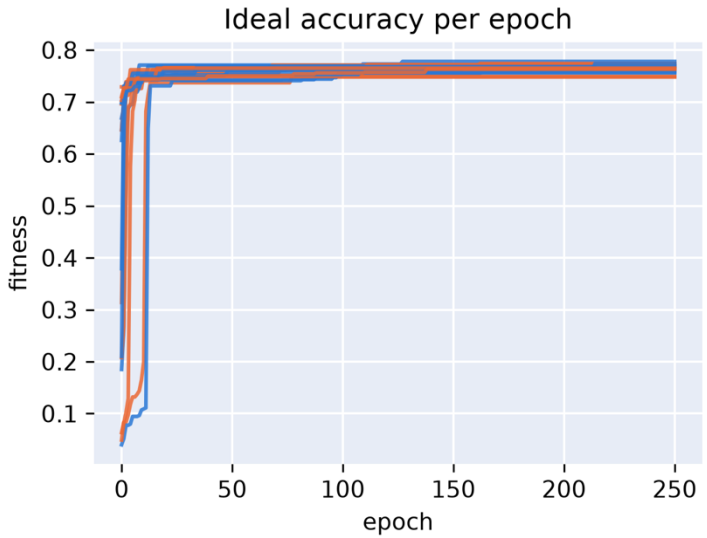
Genetic Evolution Training Schematic for SNNs

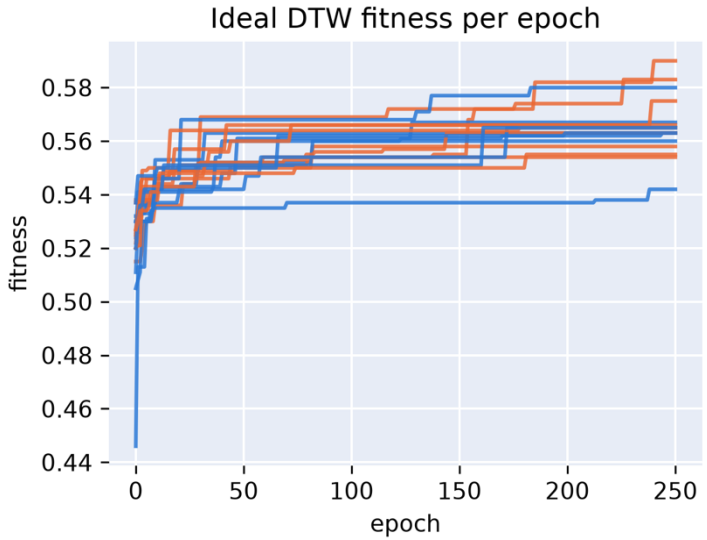


Schuman, Catherine D., et al. "An evolutionary optimization framework for neural networks and neuromorphic architectures." *2016 International Joint Conference on Neural Networks (IJCNN)*. IEEE, 2016.

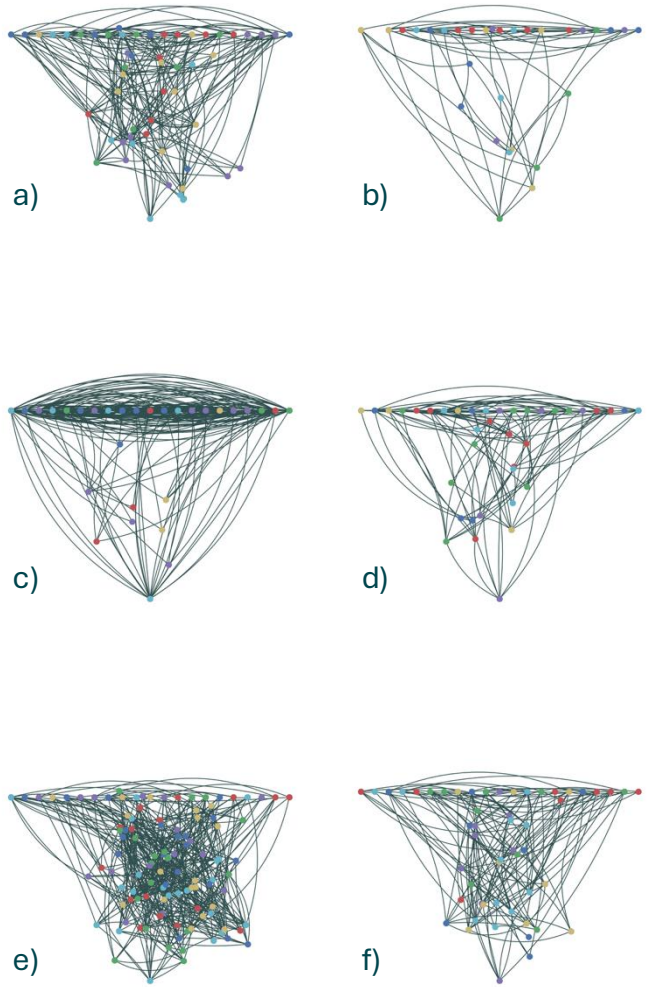
Current training results.

- DTW fitness needs tuning, as a normalization routine has “squeezed” the outputs too much.
- Nevertheless, training is quite successful, with an optimal network f1 score of ~0.8.
- We are still in early stages of training, with many hyperparameters left untouched.



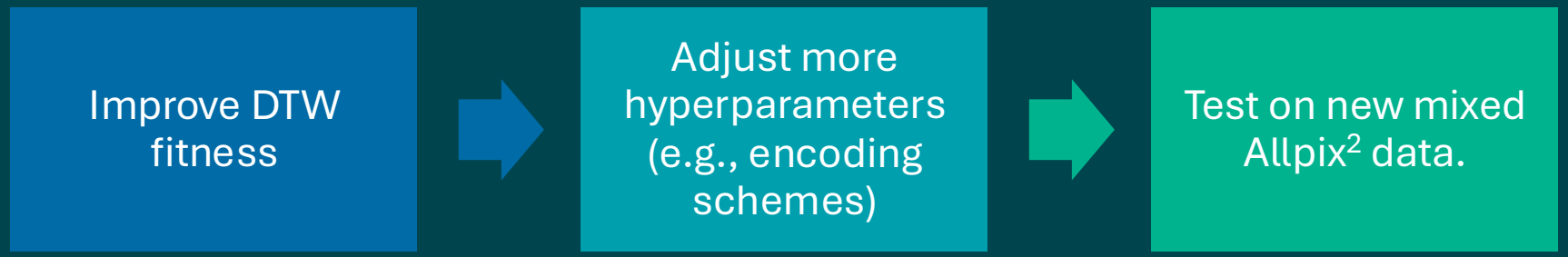


Sample networks from populations



Next steps for algorithm improvement and testing.

Short term:



Long term:



Thank you

NEUROPix Team

PI: **Mathieu Benoit**[1] (benoitm@ornl.gov)

Larry Zhang[1] (zhanglz@ornl.gov), Aaron Young[1], Amanda Steinhebel[1], Sebastian Hortua[2], Alice Bean[2], Jesse Harris[3], Pranay Damuka[3], Stefan Spanier[3], George Evans[3], Katie Schuman[3], Shruti Kulkarni[1], Seth Johnson[1], Kailyn Mack[3], Andrew Nicholson[1], John Sparger[1], Ramashish Gaurav[1]

[1]ORNL, [2]KU, [3]UTK

Citations

[1] “Memory Prices Climb 500% in 12 Months, up to 10x the Lowest Ever Tracked Prices — 128GB of DDR5 Now $3,399.” Tom’s Hardware, August 17, 2026. https://www.tomshardware.com/pc-components/ram/memory-prices-climb-500-percent-in-12-months-up-to-10x-the-lowest-ever-tracked-prices-128gb-of-ddr5-now-usd3-399.

[2] PCSP. “Server Price Increases 2026: Lead Times and What to Do.” Accessed October 20, 2026. https://pcserverandparts.com/news/server-price-increases-lead-times-2026/.

[3] “Allpix Squared v3.2.0 User Manual.” Accessed October 30, 2025. https://allpix-squared.docs.cern.ch/docs/.

[4] Llopart, X., J. Alozy, R. Ballabriga, et al. “Timepix4, a Large Area Pixel Detector Readout Chip Which Can Be Tiled on 4 Sides Providing Sub-200 Ps Timestamp Binning.” *Journal of Instrumentation* 17, no. 01 (2022): C01044. https://doi.org/10.1088/1748-0221/17/01/C01044.