Design and construction of the Inner Tracker for the CMS Upgrade at HL-LHC

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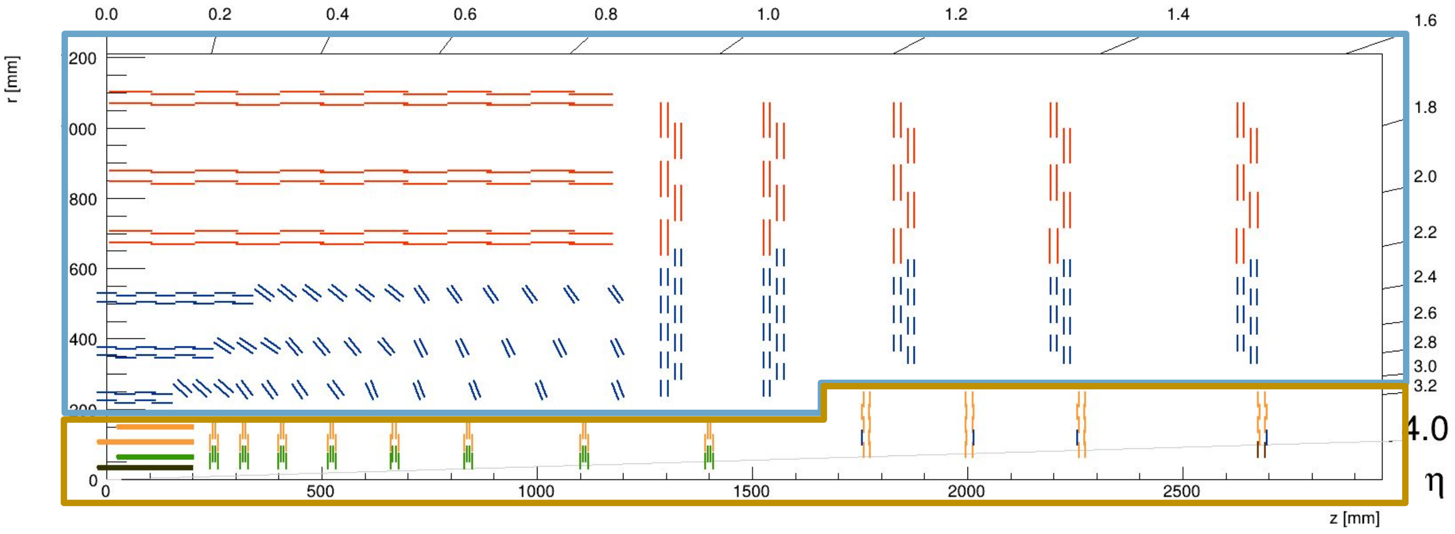
Phase II upgrade of CMS Tracker (focus on IT)

Complete new tracker that will replace the current detector during HL-LHC:

- Extended geometrical coverage
- Participation in the L1 trigger (Only Outer Tracker)
- Reduction of passive material
- Larger r-o bandwidth to cope with increased limit of triggers
- Higher granularity → *in IT 25x100 μm² pitch ensure occupancy below 0.1%*
- Radiation hardness (after Run 4 up to ~ 2× 10^{16} n_{eq}/cm^2 and up to 1 Grad in the innermost IT Layer) → *in IT thin planar sensor and 3D sensors, 65 nm CMOS based ROC*

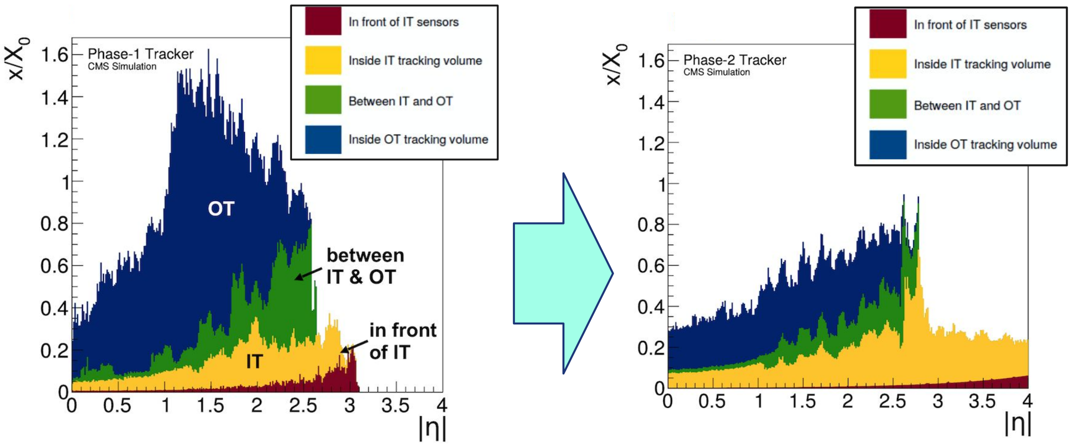


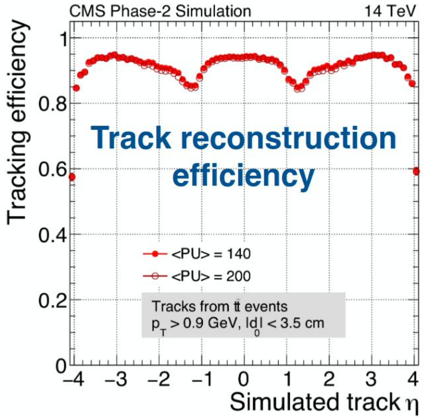
Outer Tracker (OT): more in [Inna's contribution]

Inner Tracker (IT)

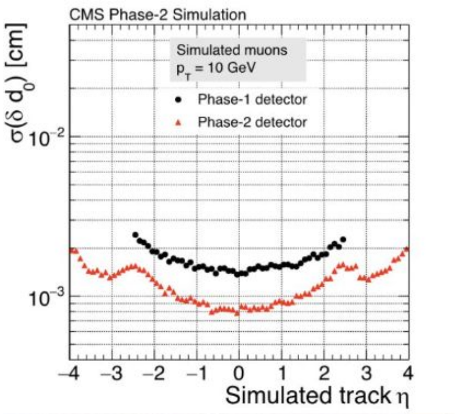
Expected Tracking performance

- Serial powering chain and lightweight mechanics allow to maintain low the IT material budget, despite the increased granularity and power consumption
- Tracking performance is unchanged despite the denser environment of HL-LHC
    - Track reconstruction efficiency unaltered even at pile-up 200





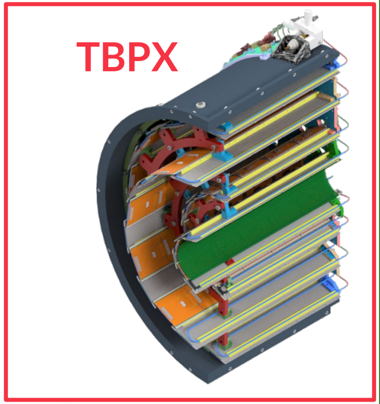
Tracking efficiency

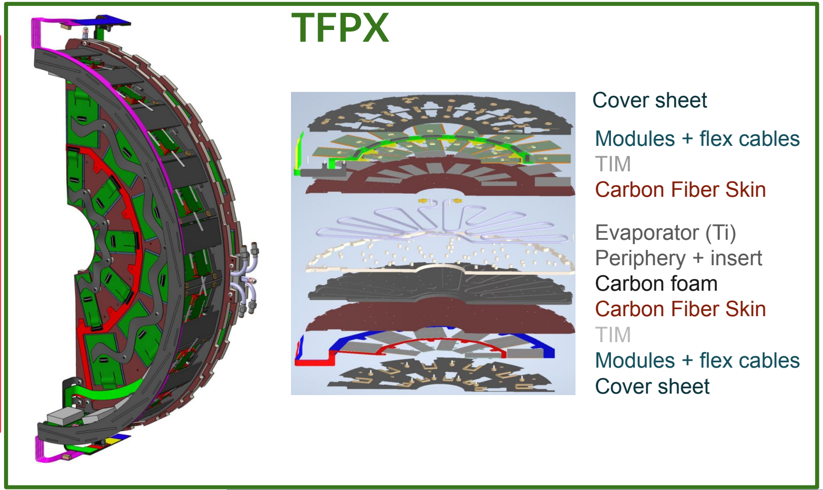


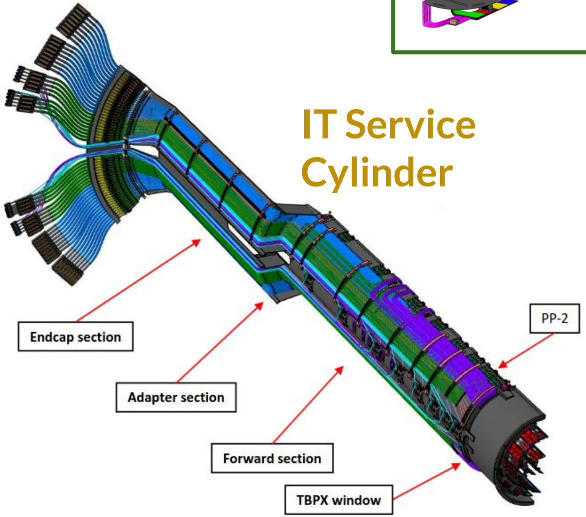
Impact parameter resolution

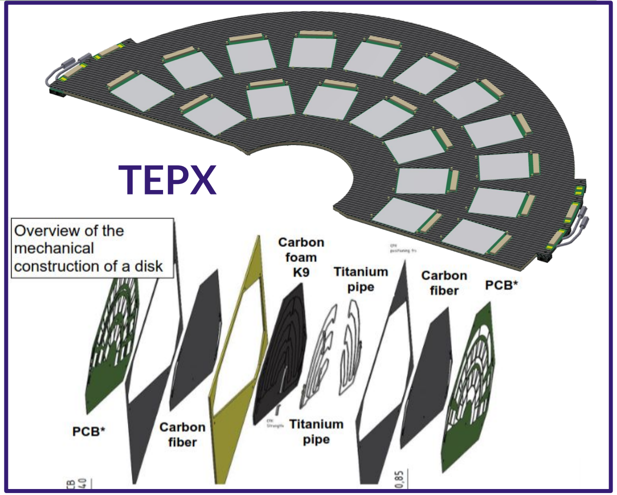
CMS IT - Mechanical concept

- Lightweight carbon fiber mechanical structure hosts the modules and the cooling pipes for bi-phase CO_2 cooling at -35 °C
    - Modules T @ -20 °C
- TBPX quarter and TFPX disks and their services are hosted in the service cylinder
    - TEPX has independent services
- Quarter assembled together, aligned and fixated in z around the beam pipe
- Full accessibility of the IT for maintenance → possibility to replace L1 in LS4

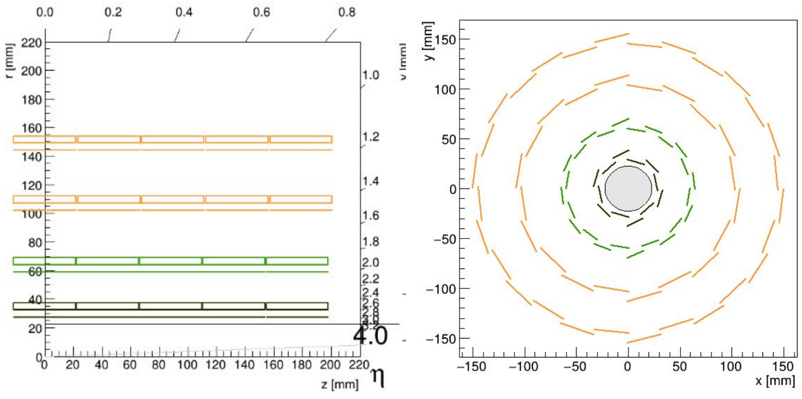




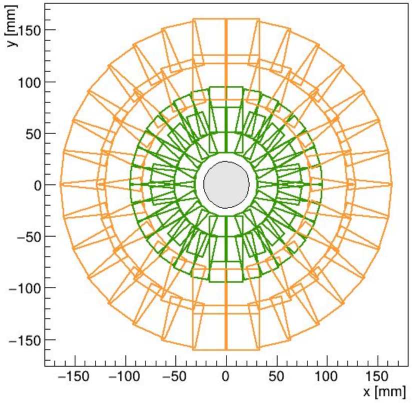




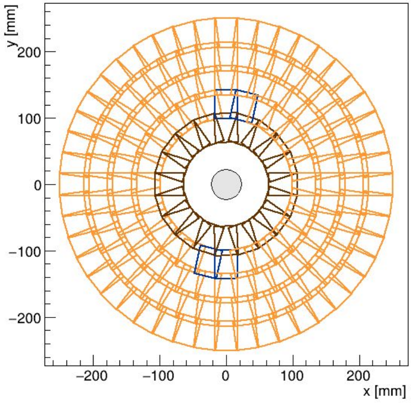
CMS IT - Construction layout



TBPX

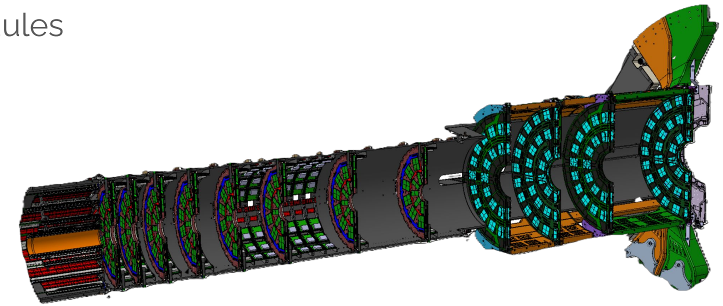


TFPX



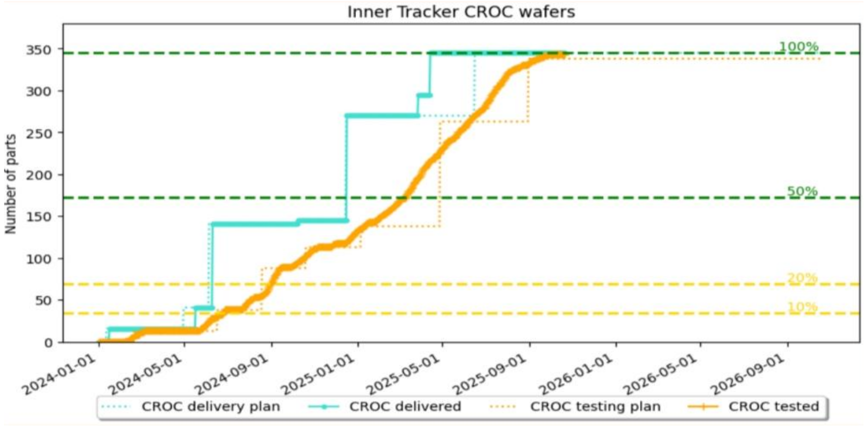
TEPX

- 2x2 modules with planar sensor, 1x2 with planar sensor and 1x2 with 3D sensors, total of 3892 modules
- TBPX → Barrel with 4 layers: L1 1x2 3D, L2 1x2 planar, L3 - L4 2x2 modules
- TFPX → Forward with 8+8 small disks: R1 and R2 with 1x2 planar, R3 and R4 2x2 modules
- TEPX → Extension with 4+4 large disks: 2x2 modules, modules in TEPX are used as luminosity monitor

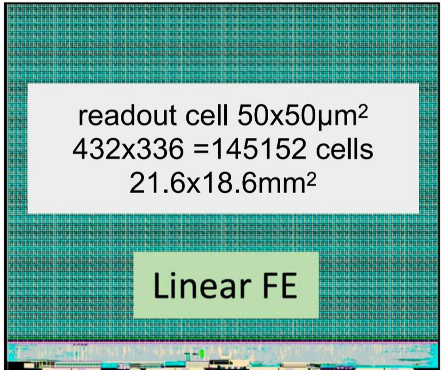


CROC

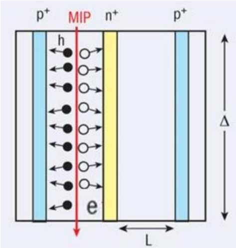
- CMS Read-out Chip starting from the common RD53 R&D, with 336x432 channels matrix
    - Low threshold (1000 e-), low noise (100 e-) ROC, 4 bit TOT per channel
    - Powered in current thanks to the shuntLDO IP block → sustain the serial powering operation
    - 50x50 μm^2 channel pitch
- All the CROC wafers have been produced and thoroughly tested at wafer level
- CROC production in stock, delivered to hybridization companies according to need

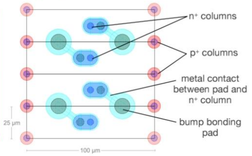


Production CROC Wafer tested [1]



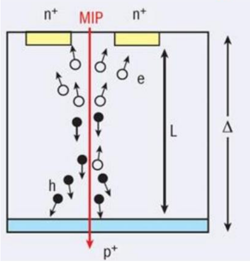
Sensors

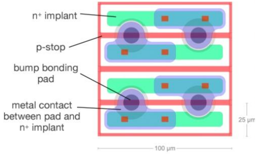




- 3D sensors chosen to equip L1 of the barrel given the lower bias voltage to be depleted
- Fully validated down to the fluence expected during HL-LHC (dedicated irradiation campaign and test beams)
  - Efficiency and resolution after irradiation are satisfying CMS requirements
- Dedicated metallization to pass from 25x100 µm² pitch to the readout pitch
- Sensors production in stock

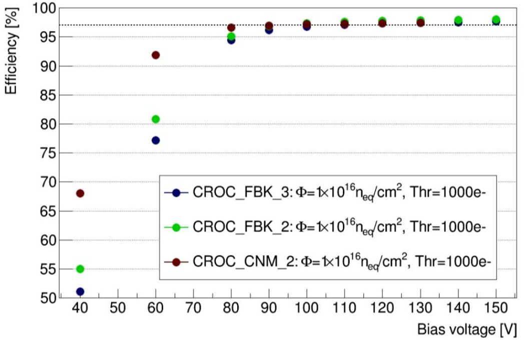
- Thin planar sensors with 150 µm thickness

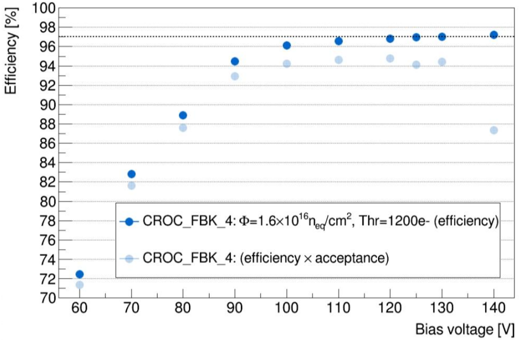




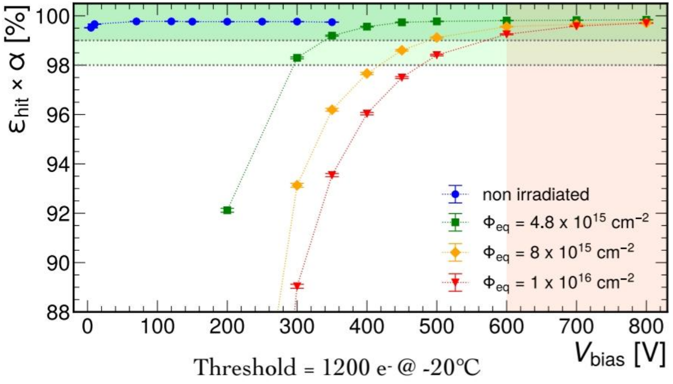
$$\epsilon_{hit} = \frac{N_{hit}}{N_{tracks}}$$

$$\alpha = 1 - \frac{N_{masked\ pixels}}{N_{total\ pixels}}$$





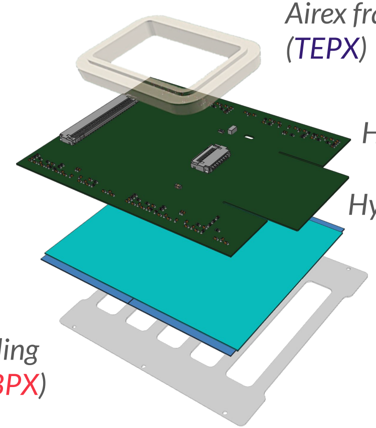
[Results for irradiated 3D sensor with normal incidence](#) [2]



[Efficiency times acceptance for irradiated planar](#) [3]

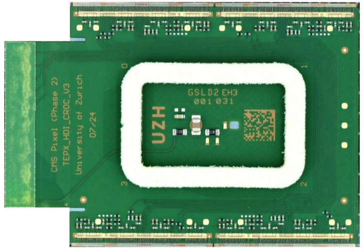
CMS IT modules

- Flip Chip and hybridization is done at three different companies
- Modules foresee a passive high density interface (HDI) for holding and data/power connections
  - The HDI is connected with the CROC through wire bonding



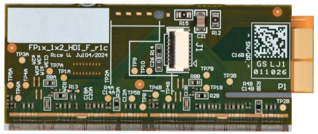
- Different design for different subdetectors for cooling and mechanical fixation reason
  - Also according to the different layer or z+/z-side position
- All the modules undergo parylene coating at SCS to prevent sparking between HV and LV

TEPX

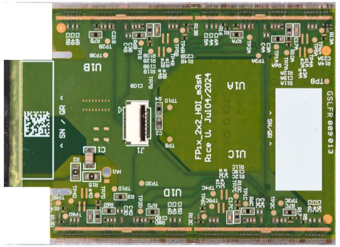


2x2

TFPX

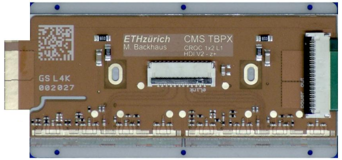


R1/R2 1x2

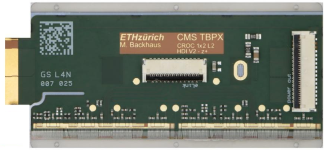


R3/R4 2x2

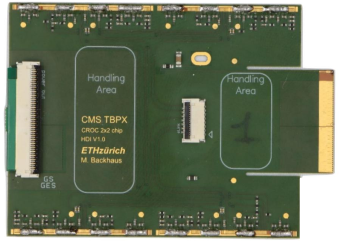
TBPX



L1 2x1



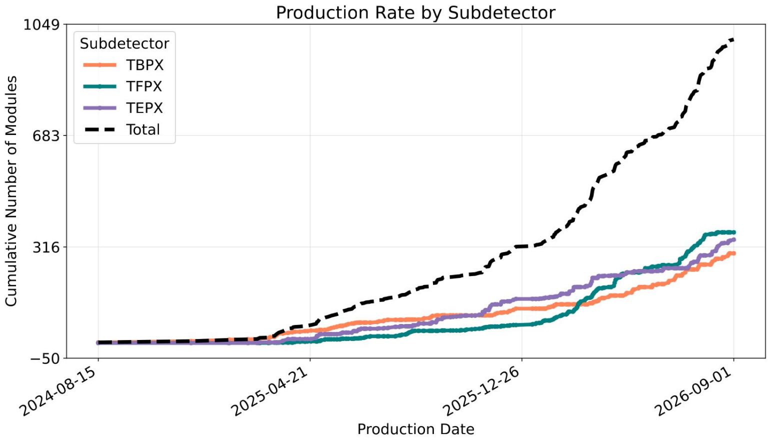
L2 2x1



L4 2x2

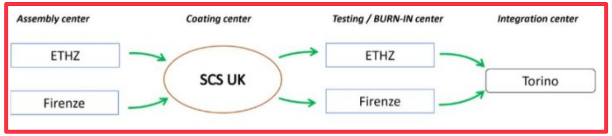
Module production and logistic workflow

- Modules production started; common workflow production across subdetectors
  - Fast testing of modules after assembly to verify IV, shunt LDO VI, and number of open bumps
  - Extensive testing of the modules after parylene coating and thermal cycling (burn-in) to assess module performance at cold

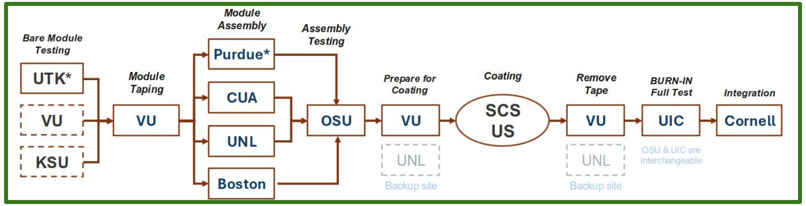


- 40% (1846 modules with a total of 5738) extra modules will be produced to account for yield loss while having spares
  - Compensate for the arising challenges during module production (core column issue, large region with missing bumps)

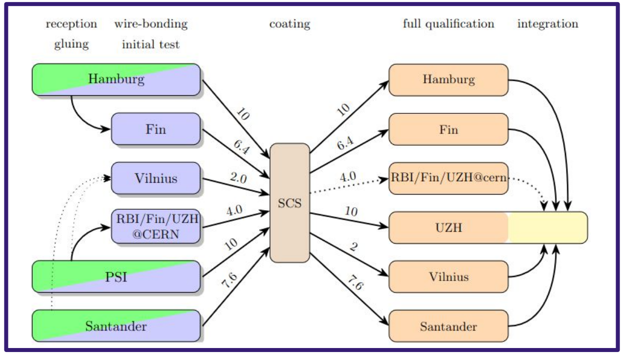
TBPX



TFPX



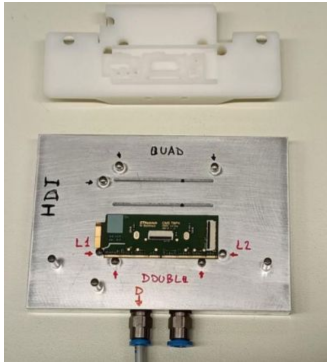
TEPX

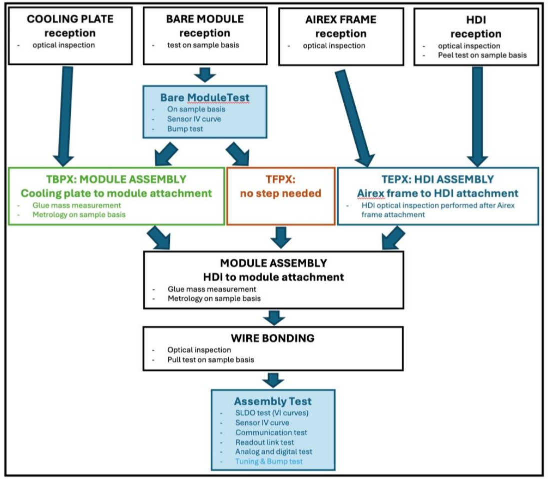


Module assembly

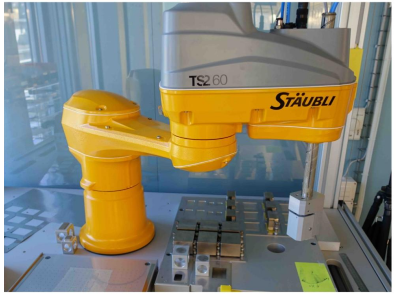
- Each subdetector has small variation with the same key points during assembly
  - E.g. bare module testing for TFPX, IV curve of bare module only for TBPX 3D
- Different automation level in assembly between subdetectors
  - TBPX modules by manual assembly with jigs and template, with stencil for glue deposition
  - TFPX modules by assembly with jigs and templates, with gantry correcting the position for reference markers
  - TEPX modules assembled by a robotic arm, with parts disposed in a tray with precise order and glue applied by stamp
- Expected throughput is obtained either by parallelization of assembly stations or batch assembly with the robot

TBPX *module assembly station*

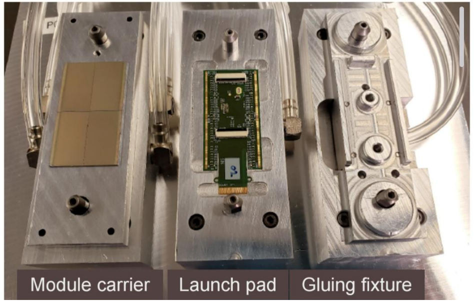




TEPX *robotic arm*

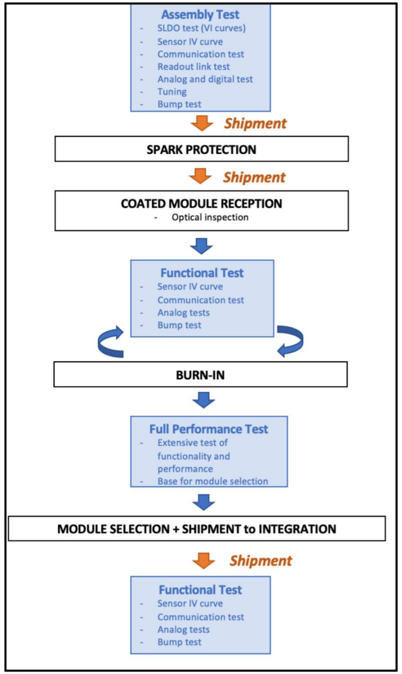


TFPX *module assembly sequence*

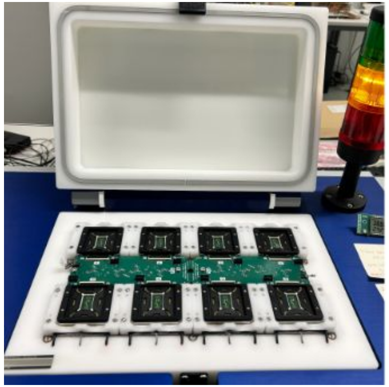


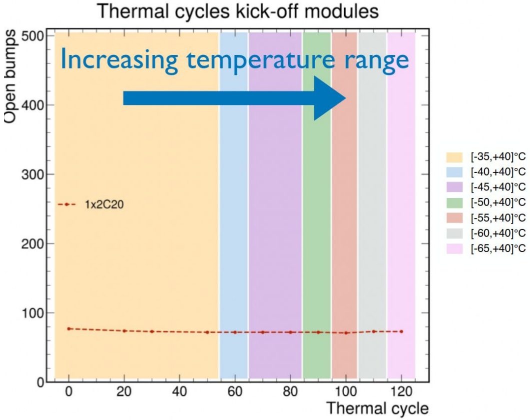
Module testing workflow

- Testing after module assembly and coating are performed in a 8-slots peltier box where temperature could range between -35 ˚C and 40 ˚C
  - Up to 8 modules together can be tested to achieve parallelization during testing
- Common acquisition software, grading software and construction database are established
  - Software developed to ensure unattended testing automation and results uploading
- On sample basis, extensive tests, e.g. thermal cycling with increasing temperature range to prove stability of bump bondings
- QC criteria finalizationwith increased statistics



8-peltier cold box

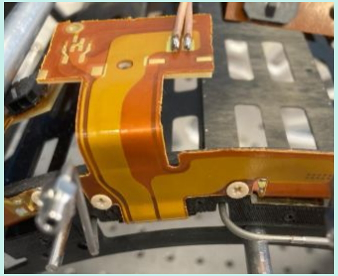




Module QC details: more in [Christina's contribution]

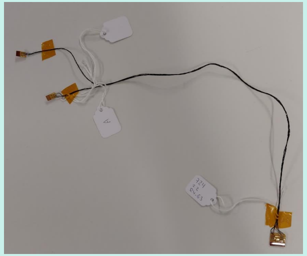
[Results of extensive thermal cycling used to validate bump stability during hybridization pre-production] [4]

Powering and DAQ chain - frontend

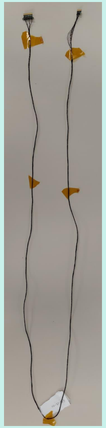


Flexes to distribute power to serial chain and HV in TFPX/TBPX, a PCB covering the disks for TEPX

Production TBPX flex



Production TFPX e-link harness

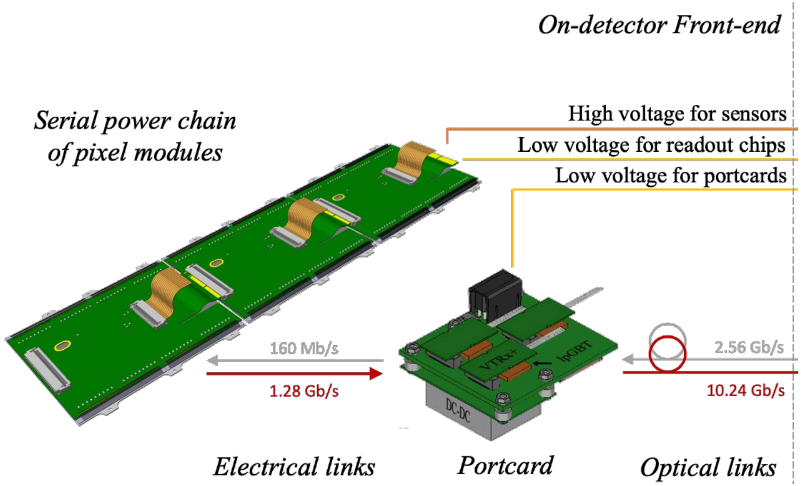


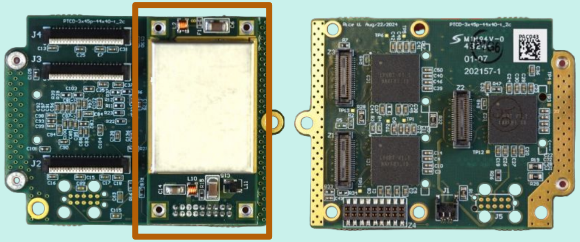
Pre production TBPX e-link harness

Up to 6x 1.28 Gb/s lane for lpGBT, 1x 160 Mb/s lane per module

Twisted pairs for TBPX/TFPX (max 1.6m)

Flat cable for TEPX

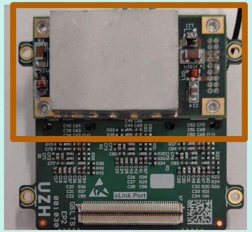




TFPX/TBPX Portcard pre-production board

680 portcards, each with 3x LpGBT + 3x VTRx+ ensure optical conversion

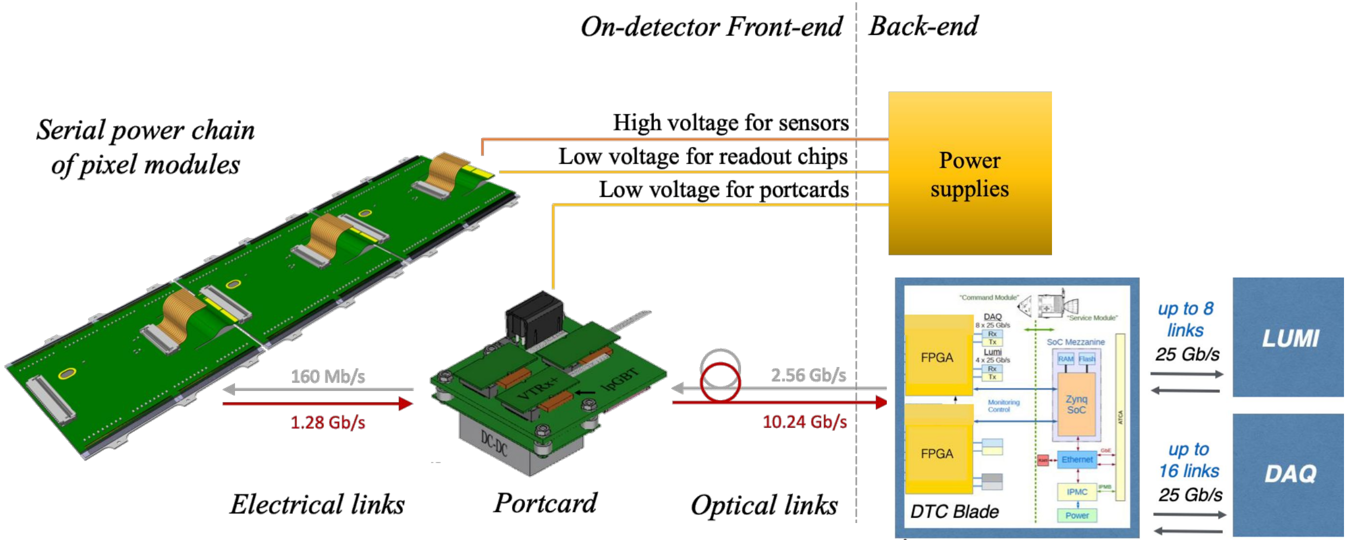
Finalizing QC criteria for portcard selection



TEPX pre-production portcard

On portcard mezzanine DC-DC converter based on bPOL → can be replaced later

Powering and DAQ chain - backend



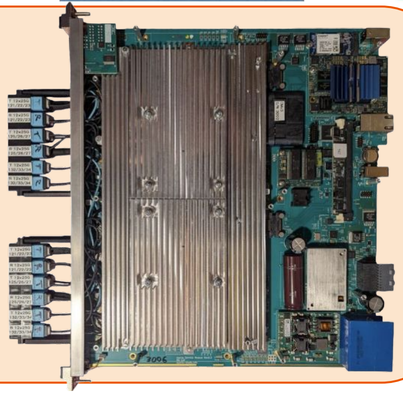
IT power supply prototype

60 kW power system, with 500 serial power lines

HV is in parallel per serial chain

Apollo board used for IT Data Trigger Control system (DTC)

36 boards in total

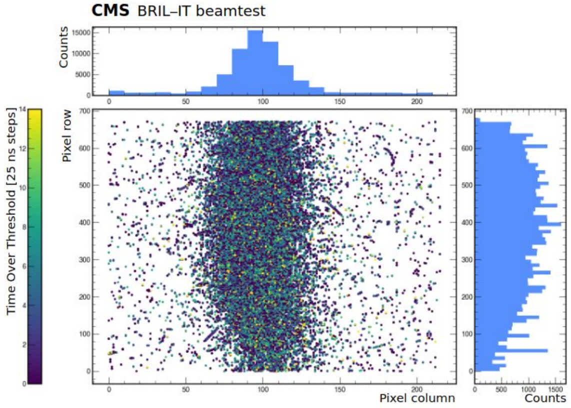


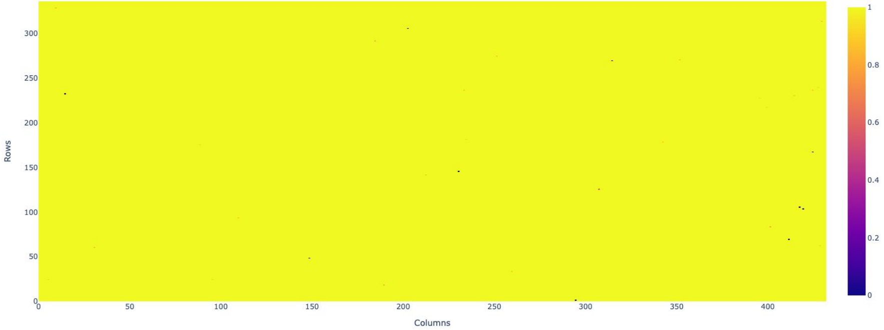
Apollo pre production board

IT back-end for integration

- While module on structure will still be tested with μTCA-based DAQ, when subdetectors will be integrated final DTC software based on ATCA backend will be used
    - Data taking with ATCA backend during BRIL/IT test beams (online decoding, clustering, ROC configuration)
- DTC software has been developed as common effort between IT and OT
    - Library in the common [ShepHerd's RunControl framework](#) .[5]
    - First calibrations based on pixel injection have been already deployed

[*Cluster map in the silicon pixel module, in unit of time over threshold*](#) [6]



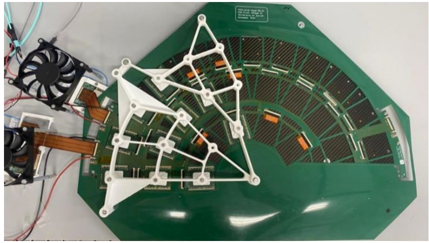


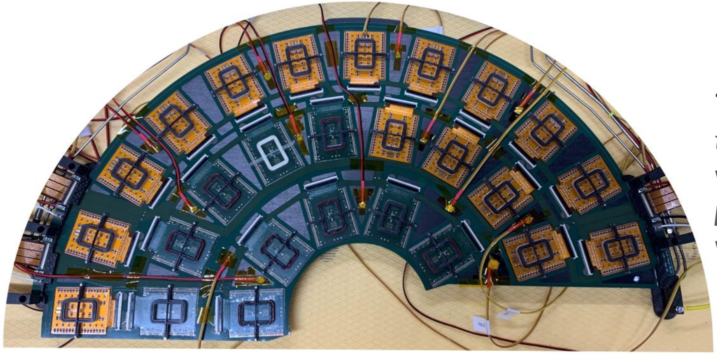
Efficiency map obtained by injecting each channel with large signal performed with final DAQ software

System tests

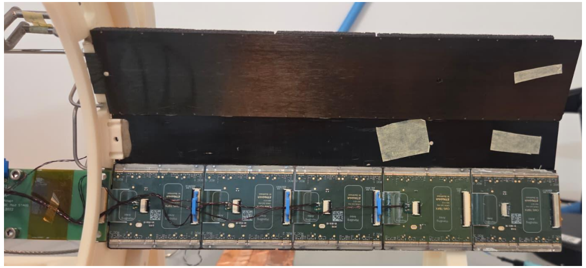
- Several system tests have been realized by all subdetectors, equipped with final read-out, final powering and final mechanics
- Thermal, powering and read-out validation for realistic system bench featuring final modules
- Expertise for the integration center

TEPX disk for DTC software development

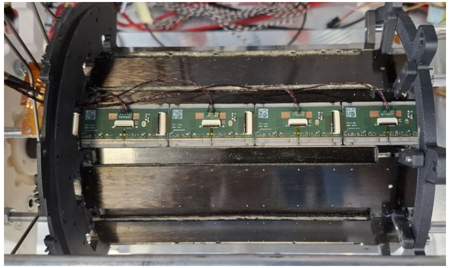




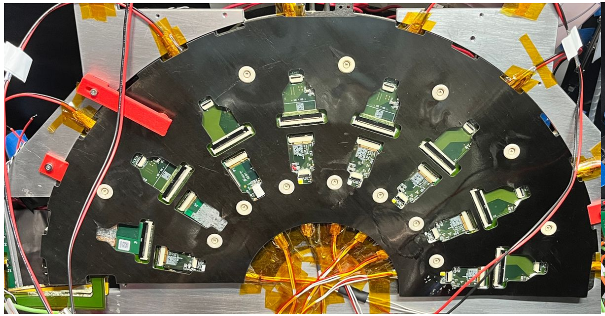
TEPX disk system tests for thermal validation and powering validation

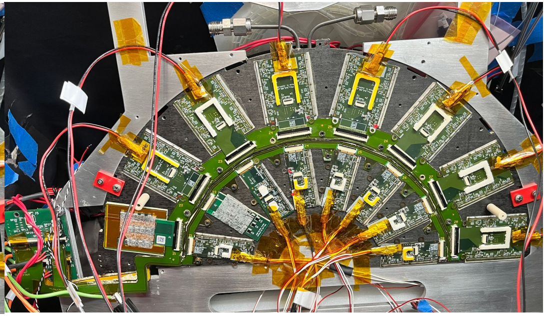


TBPX L3 for read-out validation and thermal validation of irradiated module



TBPX L2 first for thermal validation, now for powering, read-out and grounding studies



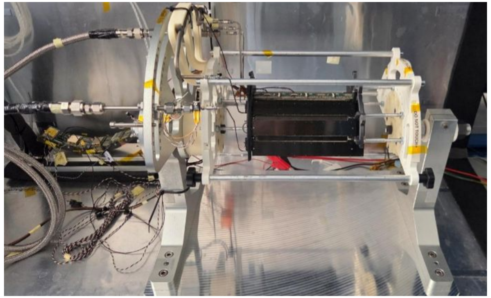


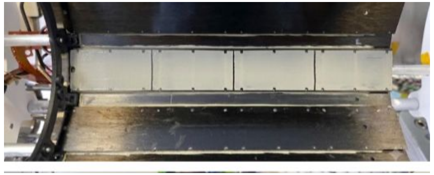
Fully equipped TFPX disk for thermal and read-out validation

Towards integration: modules on structure

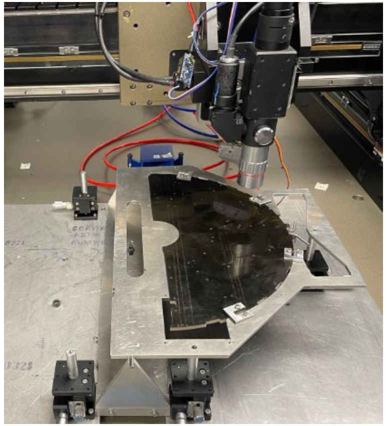
- Readiness of integration center towards structure equipment in terms of tooling, resources, procedure and testing strategy
  - **TBPX**: Modules glued with handling tools, proceeding module by module, layer by layer
  - **TFPX**: "dee" gantry for TIM deposition, module and power flexes mounting and position measurements
  - **TEPX** will use gantry for TIM application in a dedicated box, dedicated handling tools for module placement

- Auxiliary parts production is ongoing or complete, e.g.,
  - Thermal validation of TBPX L4-L3-L2 completed
  - All TFPX e-links have been produced
  - Huge improvement in TEPX disk thermal interfaces

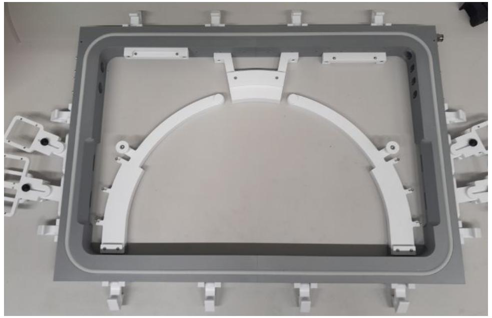




TBPX cradle to host layers, with TIM deposition



TFPX "dee" gantry at Cornell



TEPX disk box at UZH

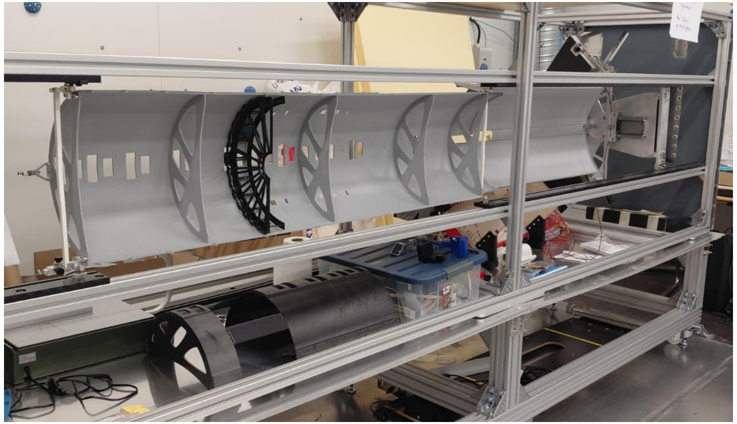
Towards integration: Subdetector integration

- TBPX and TFPX disks will be joined and integrated together in the ITST by quarter at CERN → first time there will be the r/o, power and cooling capability to sustain a TFPX+TBPX quarter

- Integration of TEPX disks and services will happen in UZH first and then the "octant" will be attached to the ITST

- Logistic is finalized, ongoing tooling and testing plan finalization after mechanical integration → subset of module QC tests to verify detector performance and exercise the DAQ + continuous monitoring

- Schedule well defined to cope with final installation at the end of LS3, with contingency for parts replacement (e.g. DC DC converters for portcards) or to cope with possible compression

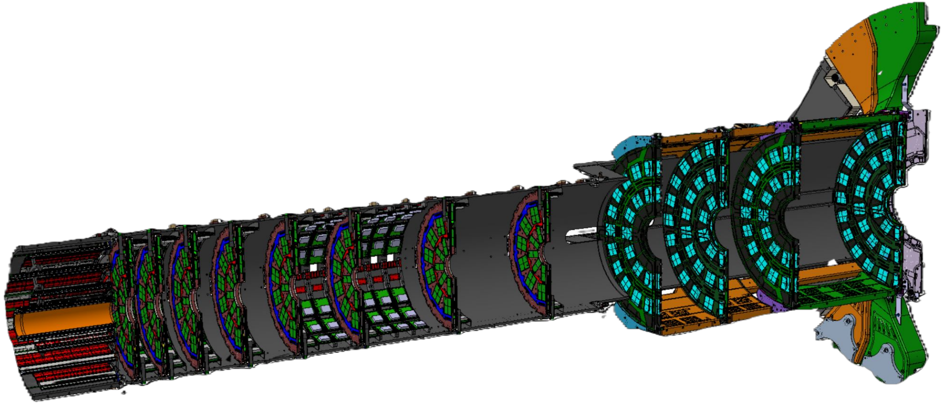


*IT service cylinder mock-up in a cassette, where **TBPX** and **TFPX** will be joined*

*Mock-up of **TEPX** "octant", Disks + TEPX services in the dedicated box for integration*

Summary

- CMS IT is a challenging and ambitious project that will be able to guarantee unaltered tracking performance during HL-LHC
- The detector exhibits new and exciting technological developments never adopted in such a large scale in a detector
- Production is ongoing with module integration starting in the following weeks
  - Module availability represents the bigger challenge
  - First quarter is expected to be delivered next year, paving the way to large scale detector integration
  - Readiness has been demonstrated, with contingency to cope with the scaling complexity of the system
- Last detector to enter CMS, profiting for the full LS3 for module production and integration



Thank you for the attention !

*14th **International***
Conference on Position Sensitive Detectors,
04/09/2026

Back up Material

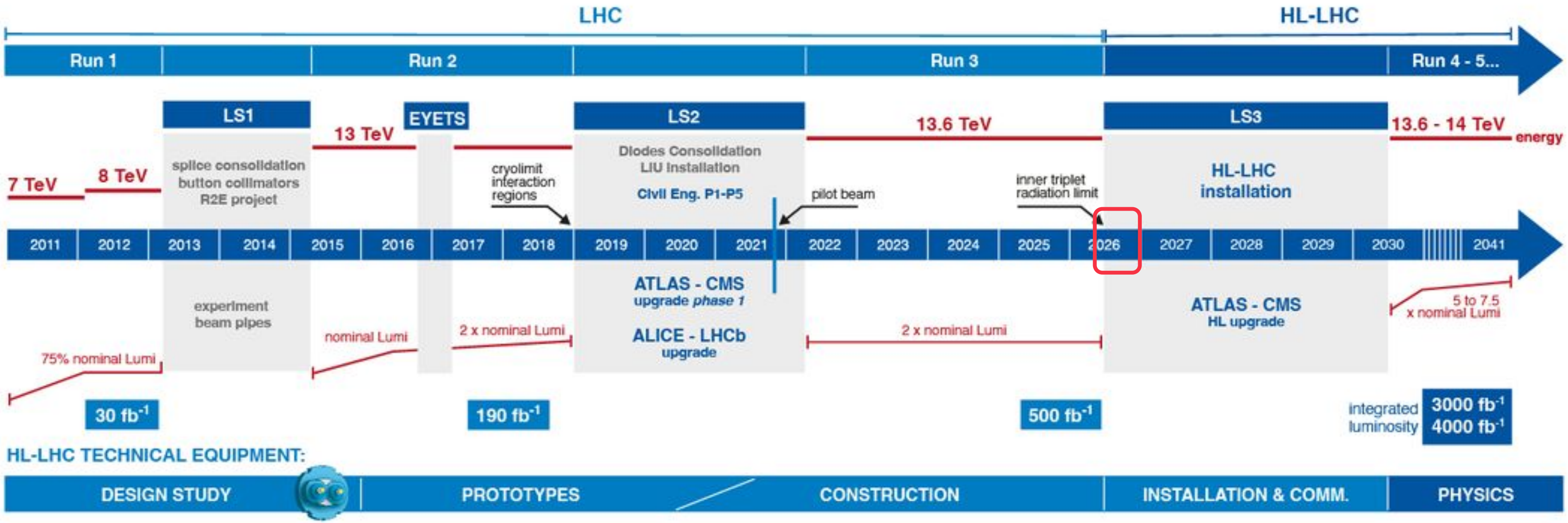
*14th **International***
Conference on Position Sensitive Detectors,
04/09/2026

References

- [1] M. Grippo, on behalf of the CMS Tracker Group, *"The CMS pixel tracker upgrade for High-Luminosity LHC: from sensors to the full detector"*, 21 "Trento" Workshop on Advanced Silicon Radiation Detectors, https://indico.cern.ch/event/1586892/contributions/6846276/
- [2] CMS Tracker Group, *"Evaluation of 3D pixel silicon sensors for the CMS Phase-2 Inner Tracker"*, NIM A 1088, 2026, https://doi.org/10.1016/j.nima.2026.171359
- [3] M. Antonello, on behalf of the CMS Tracker Group, *"Performance of irradiated planar pixel modules for the Phase-2 Upgrade of the CMS Inner Tracker"*, 2025 IEEE NSS MIC RTSD, https://www.eventclass.org/contxt_ieee2025/scientific/online-program/session?s=NSS-34#e1508
- [4] G, Bonomelli, on behalf of the CMS Tracker Group, *"Comprehensive design validation of serially powered CMS Phase-2 Pixel"*, 2025 IEEE NSS MIC RTSD, https://www.eventclass.org/contxt_ieee2025/scientific/online-program/session?s=NSS-27#e1481
- [6] T. Williams, on behalf of the CMS Collaboration, *" System design and prototyping of the CMS Level-1 Trigger at the High-Luminosity LHC "*, Journal of Instrumentation 19 03, https://doi.org/10.1088/1748-0221/19/03/C03016
- [6] M.Pari, on behalf of the CMS Tracker and BRIL Group, *" Test beam experiences with Phase 2 CMS BRIL and Inner Tracker: detectors, front-end, back-end, and infrastructure "*, 14th Beam and Telescopes and Test Beams Workshop, https://indico.cern.ch/event/1594436/contributions/6989150/

The HL-LHC upgrade

Instantaneous Luminosity:	$\leq 2.5 \times 10^{34}$ cm^{-2}s^{-1}	→	$5 - 7.5 \times 10^{34}$ cm^{-2}s^{-1}
Average Pile-up:	≤ 60	→	~ 140 - 200
LHC Integrated luminosity:	548 fb $^{-1}$	→	3000 - 4000 fb $^{-1}$



- Massive upgrade of CMS detector to cope with HL-LHC environment: Radiation hardness, trigger strategies, reduction of passive material

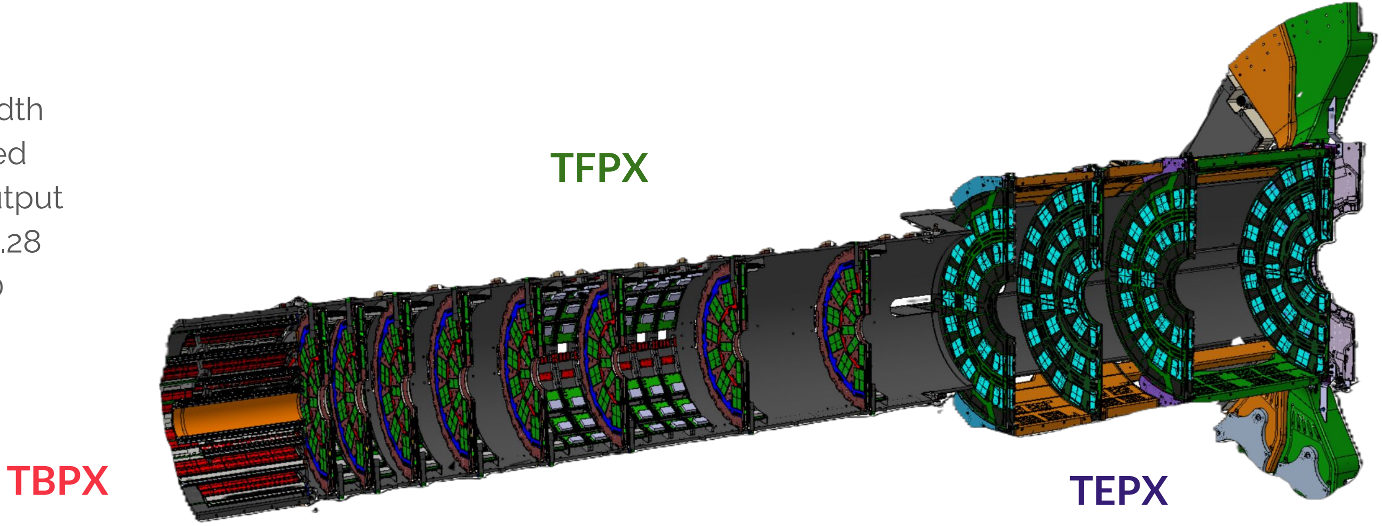
CMS IT - Requirements

- Maximum fluence of 2×10^{16} n_{eq}/cm^2 and up to 1 Grad in the innermost Layer (L1) at LS4 → thin planar sensor and 3D sensor in the innermost barrel layer, with ROC designed with 65 nm technology

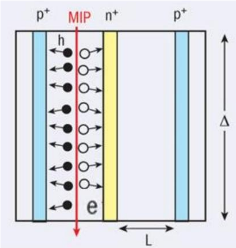
- Reduced passive material to preserve tracking performance in HL-LHC → Serial power chain for module powering and lightweight mechanics to host the CO_2 cooling pipe @ -35 ˚C

- Occupancy below 0.1 % in the IT to cope with the high pile-up → sensor pitch is 25x100 µm^2

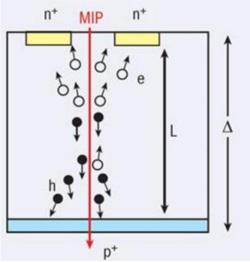
- Large read-out bandwidth to cope with the updated limit of the trigger → output bandwidth is up to 4 x 1.28 Gbps, trigger rate is 750 KHz



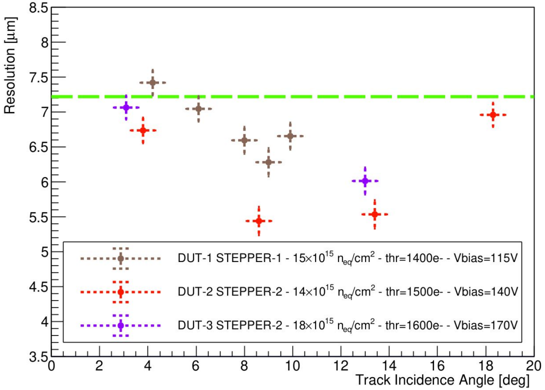
Resolution for Sensors

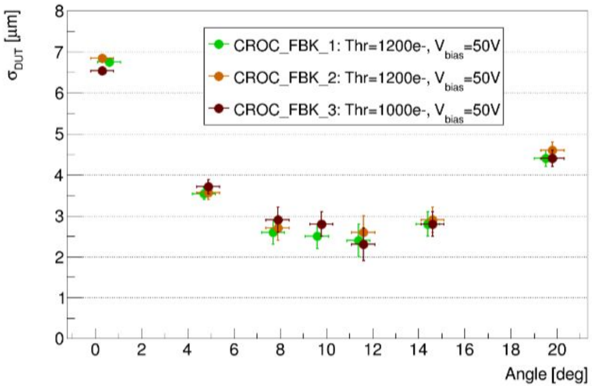


- 3D sensors chosen to equip L1 of the barrel given the lower bias voltage to be depleted
- Thin planar sensors with 150 µm thickness

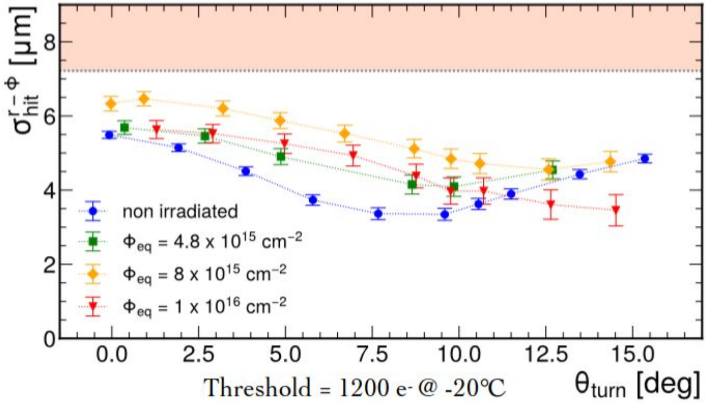


- Resolution computed for fresh and irradiated modules mostly at DESY test beam (bigger uncertainty due to passive cooling material downstream)
- Planar geometry, non irradiated max cluster size is expected at ~ 9.5˚
- Resolution of the telescope is subtracted from total residual to quote the DUT resolution only





[Resolution for irradiated 3D (RD53A) and fresh 3D sensor (CROC) as a function of the incidence angle](#) [2]

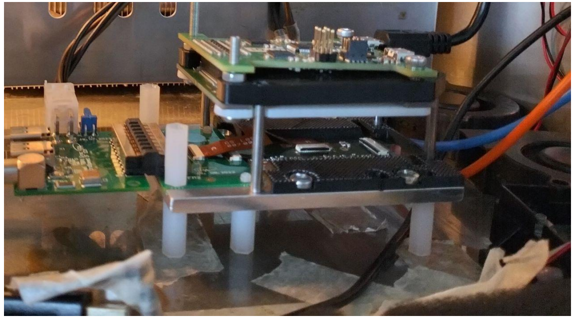


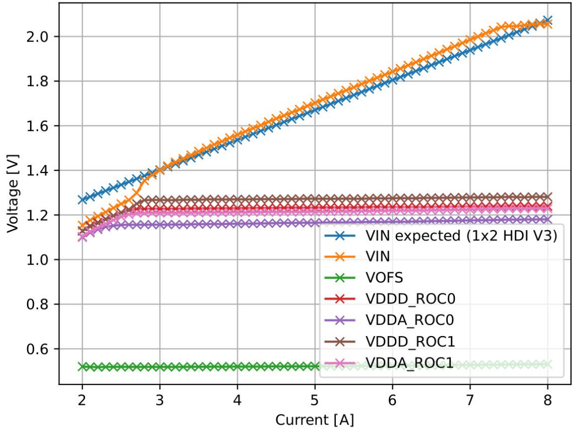
[Resolution as a function of the incidence angle](#) [3]

Powering modules - QC tests

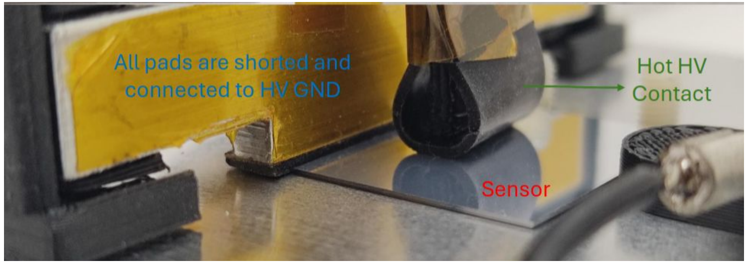
Module QC tests: more in [Christina's contribution]

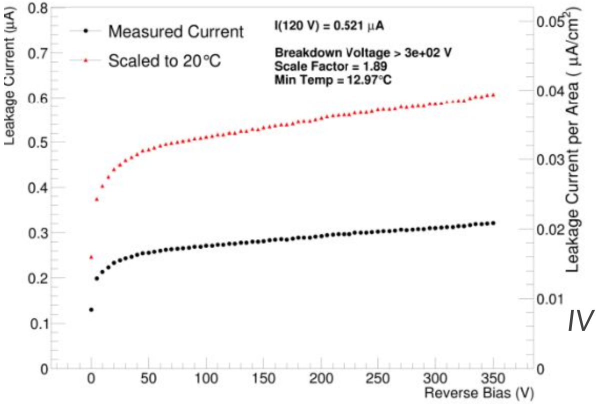
- SLDO VI curve probed both with external needle card (only pre-coating) and with monitored internal voltages
  - Selection cuts on the VI slope and offset
- Sensor IV down to High Voltage to assess sensor quality, and scaled to module T
  - In QC workflow also test at voltages expected during irradiation
- Bare module IV testing to avoid parts wasting for 3D assembly
  - Consistent results with manufacturer before and dicing





Expected SLDO VI for a double module



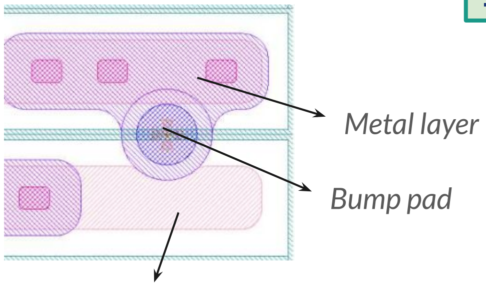


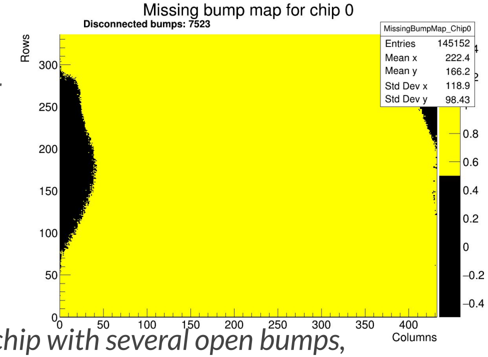
IV of a sensor scaled for module T

Selected module QC tests

Module QC tests: more in [Christina's contribution]

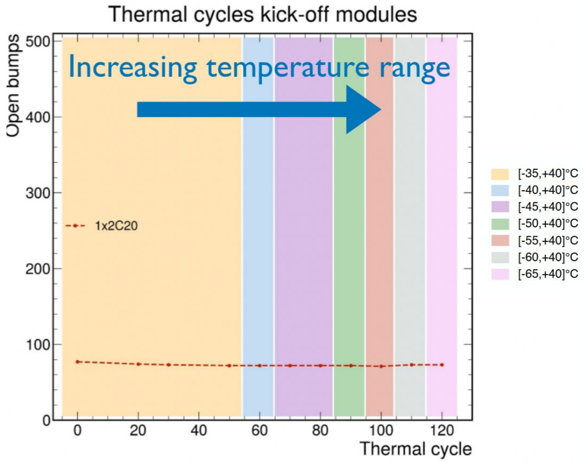
- Bump connectivity is verified exploiting the natural cross-talk between adjacent pixels
  - Fast method, well benchmarked with sources
  - Paramount to provide feedback during pre-production to hybridization companies



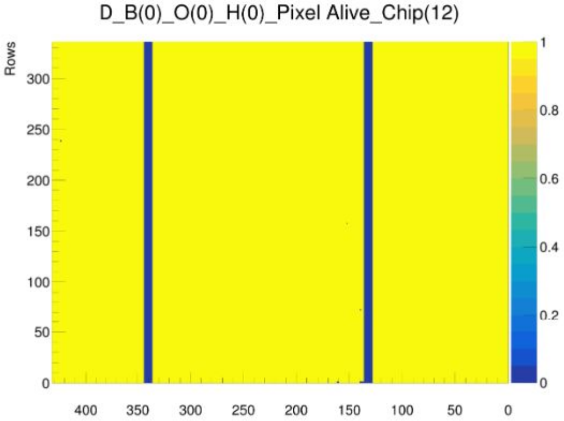


Flip chip with several open bumps, cross-checked also with X-ray measurements

- To emulate thermal stress, after coating, 10x thermal cycles between -35 ˚C to +40 ˚C are performed as part of the QC
  - Extensive test with increasing temperature range on sample basis
    - Also used to assess bump connection stability during pre-production modules

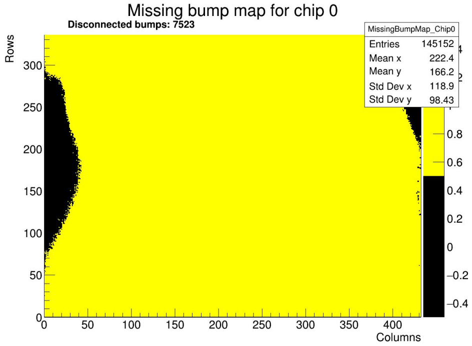


Challenges of Modules Production



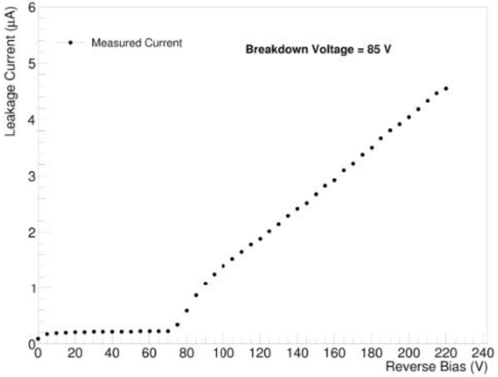
Core column defects

- Coating has to be exercised between different modules type
- Core column issue → Mitigated by having laser pre-grooving before dicing at the company
  - Mask pattern looking for pixel to reduce core column impact



Flip chip with several open bumps, cross-checked also with X-ray measurements

- Open Bumps continuously improved by weights and vacuum optimization at the hybridization company



- Early IV breakdown for planar sensor (no sensor bias scheme → difficult to probe all the sensors in the wafer)
  - Small impact constantly monitored during production