ATLAS EXPERIMENT

UNIVERSITÉ DE GENÈVE
FACULTY OF SCIENCE

Lessons learned from the ATLAS Pixel Detector Operation at the LHC in Phase-1

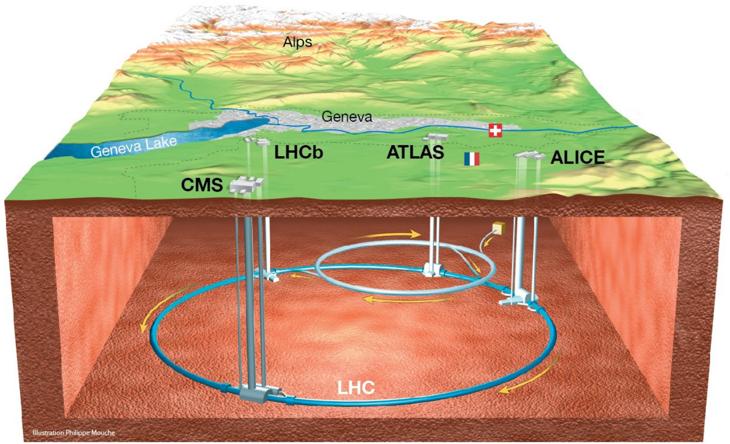
1 September, 2026

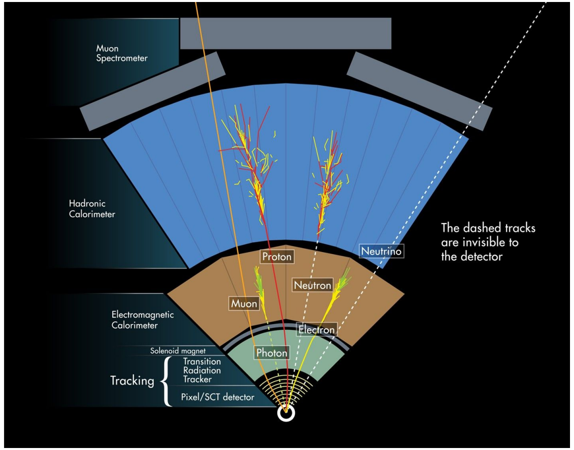
14th International Conference on Position Sensitive Detectors
Queen Mary University of London

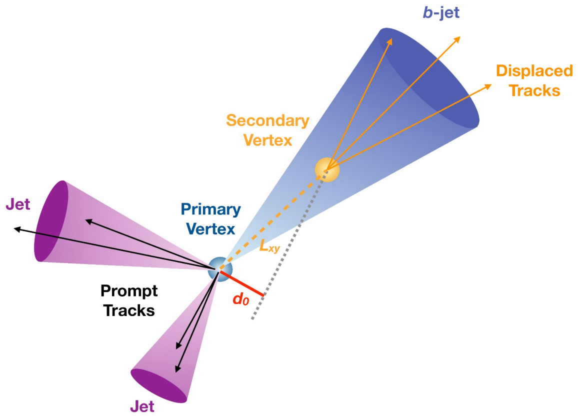
Chris Scheulen *(on behalf of the ATLAS Collaboration)*

Tracking Detectors at the Large Hadron Collider

A very brief Introduction







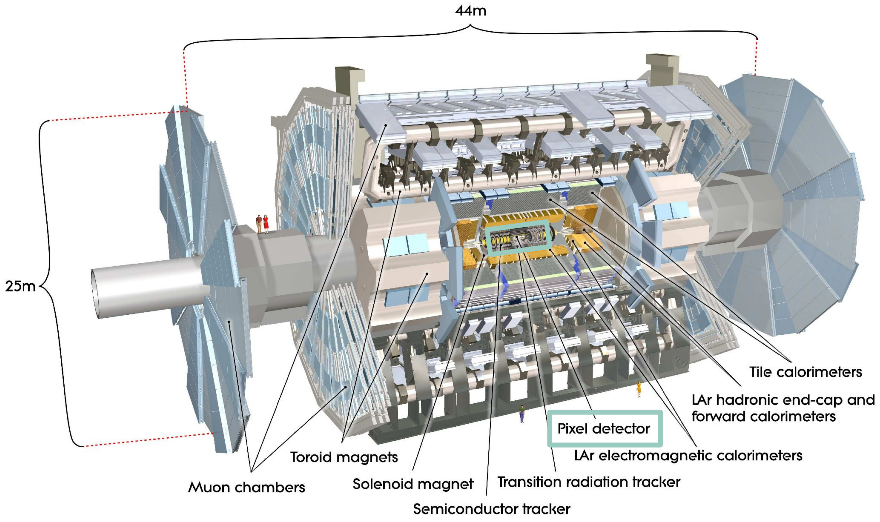
- LHC: world's largest particle accelerator
  - Led to Higgs boson discovery by ATLAS & CMS in 2012

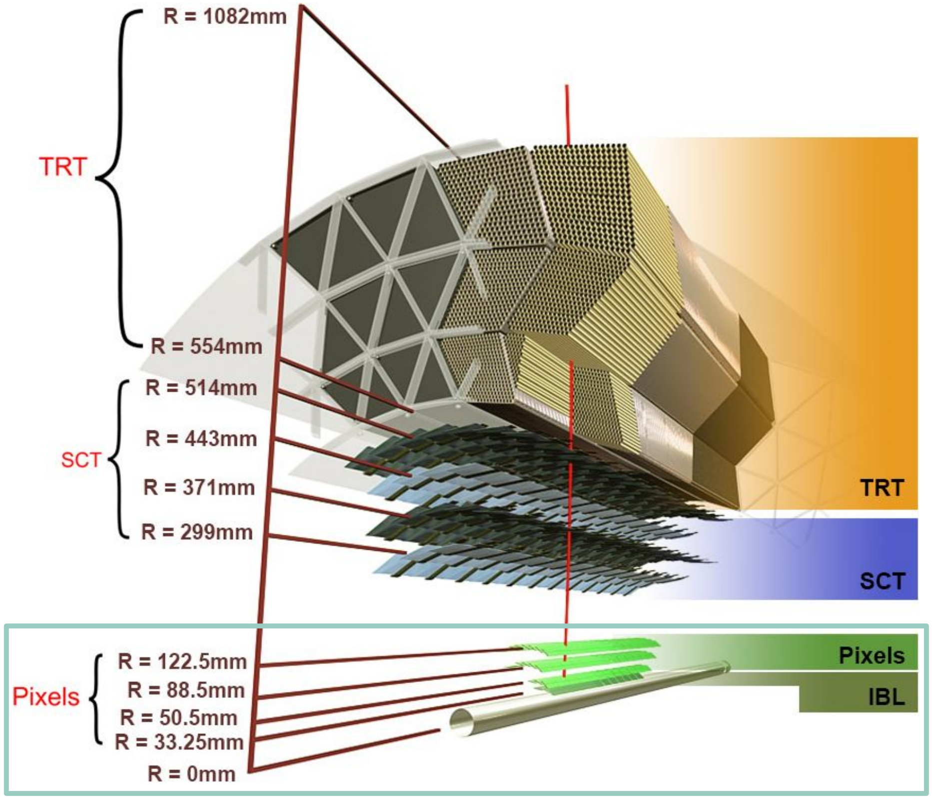
- Tracking detectors enable in the LHC experiments enable
  - Vertex & trajectory reconstruction
  - (Transverse) momentum measurement
  - Particle identification via impact parameters & secondary vertices

- Full introduction to position sensitive detectors in particle physics: Francesca's talk at 11:00 on Thursday

The ATLAS Pixel Detector

An Overview





- Innermost part of ATLAS since start of operations
  - Since 2010: 3 layers & 2 × 3 end-cap disks covering $|\eta| < 2.5$
  - Since 2015: augmented by Insertable B-Layer (IBL)
- Immersed in 2 T solenoidal field
- 92 million channels (12 million of which in IBL)

The ATLAS Pixel Detector

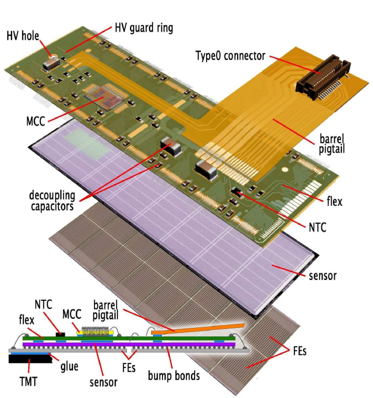
Modules

Pixel

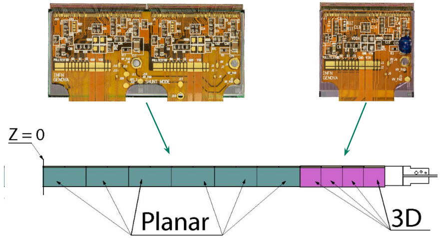
- Detector:
  - 1.7 m^2 of silicon
  - Layers at 5 cm (B-Layer) up to 12 cm
  - C_3F_8 evaporative cooling
- Modules:
  - Hybrid planar n-in-n sensor, 400 µm × 50 µm pixel matrix, 250 µm thickness
  - 250 nm CMOS front-end (FE) chip
  - 16 FEs with single controller (MCC) per module
  - Radiation hard up to $1 \times 10^{15}\ n_{eq}\ cm^{-2}$

IBL

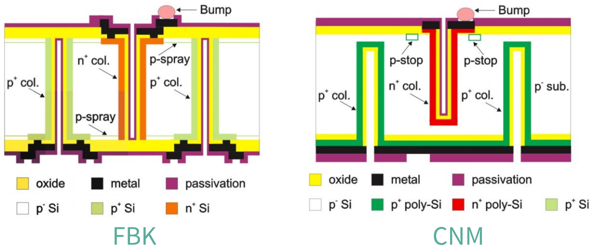
- Detector:
  - 0.2 m^2 of silicon at 3.3 cm radius
  - CO_2 evaporative cooling
- Modules:
  - Central Region: Planar n-in-n sensor of 200 µm thickness
  - Forward Region: 3D n-in-p sensor of 230 µm thickness
  - 250 µm × 50 µm pixel matrix
  - 130 nm CMOS FE
  - Radiation hard up to $5 \times 10^{15}\ n_{eq}\ cm^{-2}$



Pixel module schematic



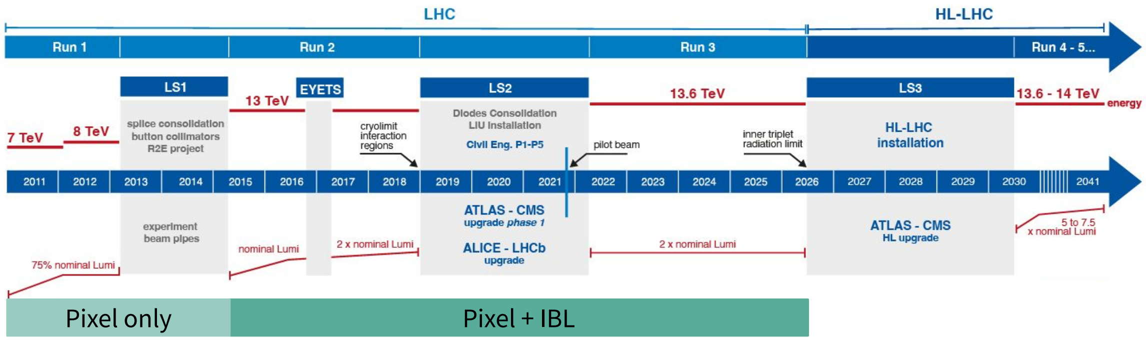
IBL half-stave

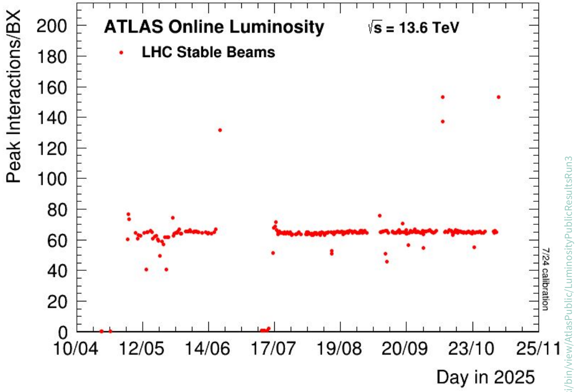


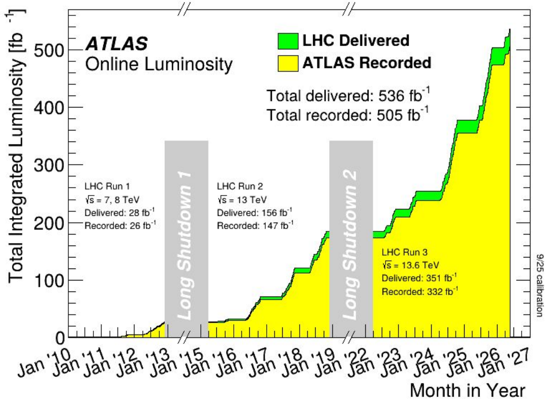
3D sensor design (2 vendors)

Data-Taking Conditions

- Detector sits in high-radiation environment close to beam-pipe
  - Total fluence in IBL up to **$3 \times 10^{15}\ n_{eq}\ \mathrm{cm}^{-2}$**
- In operation for **17 years** (IBL: 12 years)
  - About 5 years longer than foreseen by initial design
- Evolution of operational parameters beyond LHC design values
  - Number of interactions/bunch crossing **$\langle\mu\rangle = 64$** during levelling near end of Run 3
  - Far beyond design spec for Pixel!
- Total luminosity of **505 fb^{-1}** recorded by Pixel (IBL: 479 fb^{-1})







Taken from ATLAS public luminosity results page: https://twiki.cern.ch/twiki/bin/view/AtlasPublic/LuminosityPublicResultsRun3

Modules

- On-detector components inaccessible
  - Failing modules not replaceable
- Common failure modes:
  - No configuration possible
  - No configuration & dead on-module NTC (connection issues suspected)
  - Open high voltage
  - No low voltage
- **93%** of Pixel & **99%** of IBL still operational near end-of-life

Layer	2018		2026	
	Disabled/Total	[%]	Disabled/Total	[%]
B-Layer	18/286	6.2	26/286	9.1
Layer 1	29/494	5.8	20/494	4.0
Layer 2	33/676	4.8	59/676	8.7
Disks	15/288	5.2	20/288	6.9
Total Pixel	95/1744	5.4	125/1744	7.2
IBL planar FEs	1/336	0.3	2/336	0.6
IBL 3D FEs	2/112	1.8	4/112	3.6
Total IBL FEs	3/448	0.7	6/448	1.3
Total	**98/2192**	**4.5**	**110/2192**	**6.0**

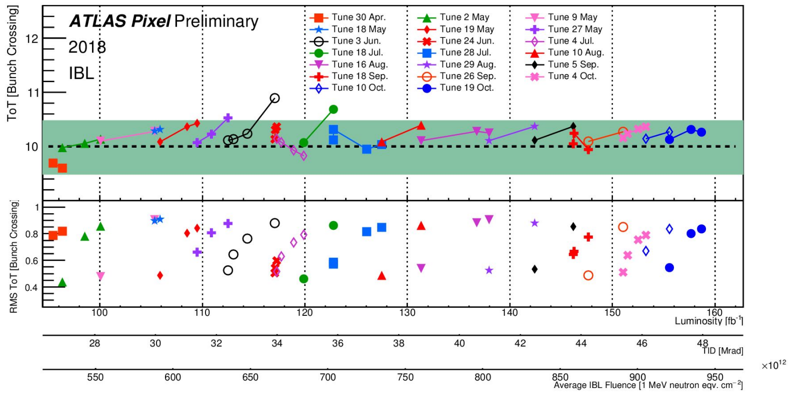
Disabled module statistics

Front-Ends

- IBL FE has some improvements over Pixel FE:
  - Updated read-out architecture
  - No controller chip required
  - Higher read-out rate
  - On-chip voltage regulators

- Good performance from both chips overall, some smaller issues:
  - Pixel FE (FEI3):
    - Digital voltage raise needed to prevent FE desync. at high luminosity
    - Preamplifier circuitry problematic at high total integrated dose (TID), operational issue without impact on data-taking
  - IBL FE (FEI4):
    - Frequent retuning required due to TID
    - On-chip regulators only switch on at room temperature for several FEs at high TID

Taken from: https://atlas.web.cern.ch/Atlas/GROUPS/PHYSICS/PLOTS/PIX-2018-009



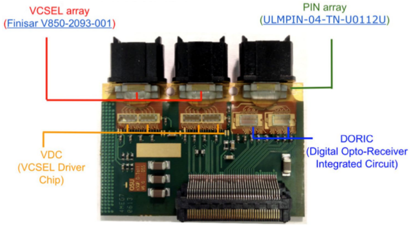
IBL retunings in 2018

➤ Good performance of both FEI3 and FEI4 front-ends, adequate capabilities for frequent monitoring & retuning critical

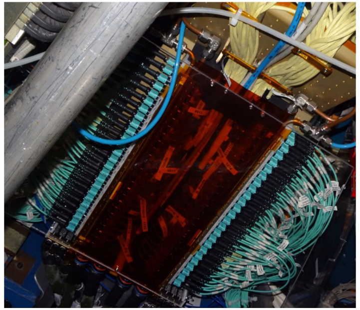
Optical Components

- Electrical signals on module side converted to optical pulses via custom optoboards
- Several optoboard failures during Run 1
  - Initially at inaccessible locations, moved out of inner detector volume after Run 1
- Further VCSEL failures during Run 2
  - Replaced before Run 3, flushed with dry air, sealed
  - No additional failures during Run 3
- Similarly, high failure rate of custom TX & RX plugins (optical converters on off-detector side)
  - TX replaced by humidity-resistant alternative
  - RX exchanged with spares since no suitable alternative model

➤ Custom optical components were source of many issues,
use off-the-shelf if possible and make components as accessible as possible



Optoboard



Sealed Optobox

RX Plugins

Read-Out Firmware & Software

Module Desynchronisation Mitigation

Modifying off-detector software & firmware only way to retain detector performance with inaccessible on-detector components
Two examples dealing with major issues during Run 3:

- Buffers for 16 triggers in Pixel modules
  - Additional trigger requests lead to desynchronisation of up to 5 seconds
  - Mitigation mechanism to skip triggers on Pixel & IBL FEs found to be buggy

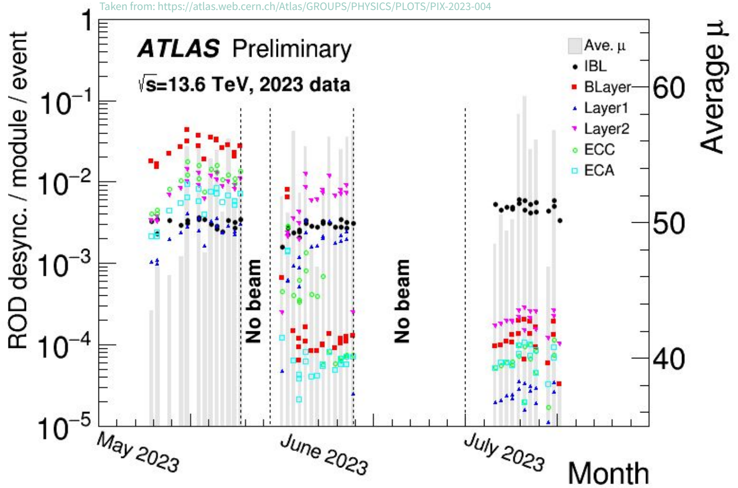
- Alternative off-detector firmware developed during Run 3 for mitigation:

"Smart Firmware"

- Working principle:
  - Keeps track of outstanding triggers for each module
  - Skips triggers over limit & inserts empty event fragment instead
  - Affected modules flagged for reconstruction

- Reduction in desynchronisation by two orders of magnitude

Taken from: https://atlas.web.cern.ch/Atlas/GROUPS/PHYSICS/PLOTS/PIX-2023-004



Desynchronisation during smart FW rollout

Read-Out Firmware & Software

Single Event Upsets

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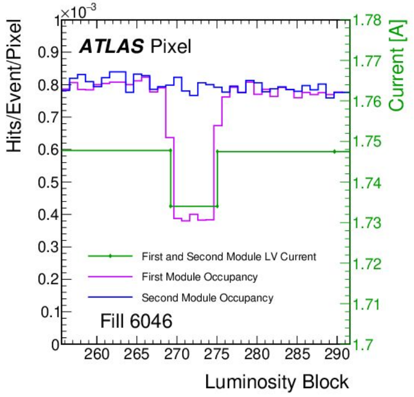
- Impact of SEUs observed despite hardened global FE registers:
  - Current changes and other FE-wide issues for global registers
  - Quiet & noisy pixels for non-hardened single-pixel registers

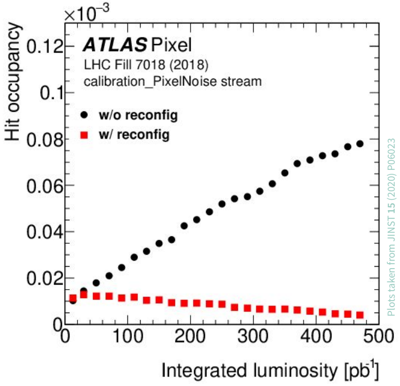
- Multiple reconfiguration mechanisms developed:
  - Fast O(0.1 s) reconfiguration during module timeout or busy
  - Global register reconfiguration during 2 ms ATLAS-wide re-synchronisation period every 5 s
  - IBL single-pixel registers reconfigure during same trigger gap on rolling basis

- Results in full reconfiguration every
  - 5 s for global IBL FE registers (every 80 s for Pixel)
  - 11 min for single-pixel IBL registers



Effect of global FE register SEU

> ➤ Continuous improvements in Firmware & Software crucial to meet emerging operational challenges



Plots taken from JINST 15 (2020) P06023

Occupancy development

Detector Condition & Data Quality Monitoring

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- Detector condition & online data quality (DQ) monitored by shift crew in control room
- Additional offline DQ monitoring performed
- Large amount of online histograms available for expert debugging of issues
  - Decision what is monitored by shifters needed
- Common issues for detector condition & DQ monitoring:
  - Relevant alerts buried in noise
  - References not appropriate since out of date or because of special fills
- Identifying symptoms of failure modes and matching to DQ metrics worked well
  - E.g. check for hits-on-track via push notification introduced after mistiming issue in Run 3

➢ Need reasonable amount of DQ metrics and detector condition alerts while covering possible failure modes

Cooling Systems

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- Common C_3F_8 cooling system in place for Pixel & SCT detectors
  - Initially using 7 compressors
  - Upgraded to thermosiphon before Run 3 (with compressor backup)
- Several issues in Pixel return line heater system during operation:
  - Failures of initial heaters led to replacements
  - Issues in heater temperature & power supply racks led to detector interlocks
  - Temperature sensor failures required repairs in inner detector volume
  - Heater efficiency dependent on line geometry
- Separate CO_2 cooling system installed for IBL
  - Redundant identical plant on standby in case of issues
  - Extremely reliable system
- Critical components even during shutdowns due to need to prevent annealing of irradiated modules

Layer	2026 Setpoint [°C]
B-Layer	-32
Layer 1	-26
Layer 2	-28/-29
Disks	-20
IBL	-20

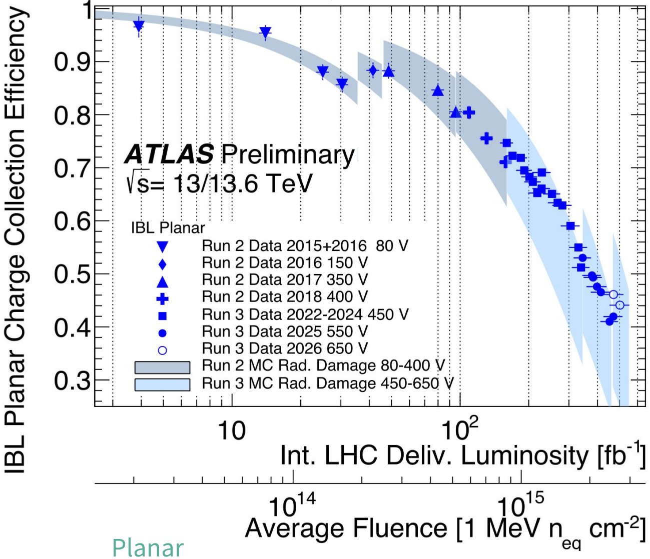
➢ Critical component for detector operation and prevention of annealing, IBL plant extremely reliable thanks to full redundancy of critical components

Radiation Damage

Charge Collection Efficiency

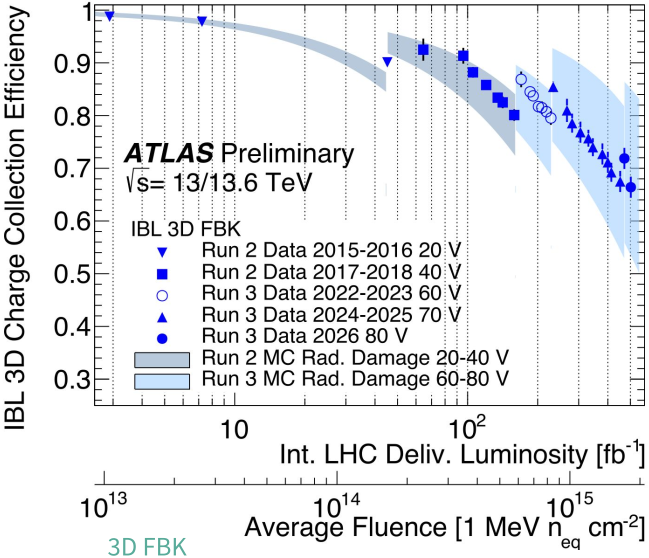
- Up to **3×10^{15} n_{eq} cm^{-2}** total fluence in IBL at end of Run 3 (IBL design limit: 5×10^{15} n_{eq} cm^{-2})
- Radiation damage in sensor bulk leads to charge collection efficiency (CCE) reduction **up to 60%**
  - Effect on CCE smaller in IBL 3D than IBL planar modules at same fluence
  - Loss in intrinsic hit efficiency limited to **1-2%** despite CCE reduction
- Effects of radiation damage on CCE included in ATLAS simulations via dedicated radiation damage digitiser for IBL planar and IBL 3D FBK modules
- Full details in JINST **21** (2026) P07048 (IBL planar) and JINST **19** (2024) P10008 (IBL 3D)

Taken from ATLAS note ATL-INDET-INT-2026-003 (update to JINST **21** (2026) P07048)



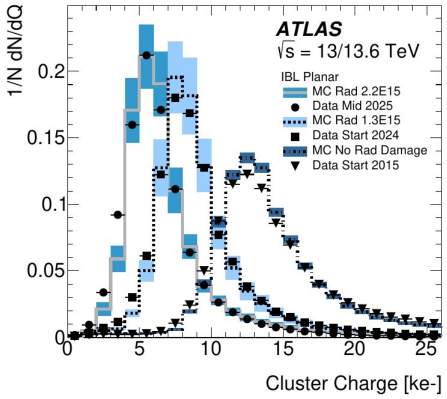
Planar

Taken from ATLAS note ATL-INDET-INT-2026-004 (update to JINST **19** (2024) P10008)



3D FBK

Taken from: JINST **21** (2026) P07048



Comparison of data and simulation

Radiation Damage

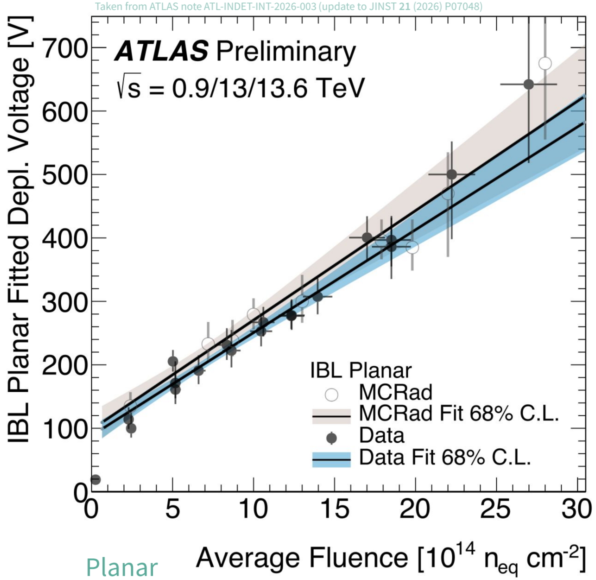
Depletion Voltage

- Depletion voltage determined via sweeping high voltage during collisions multiple times per year
  - Operational bias voltage determined in accordance with evolution
  - High voltage scans critical for retaining detector performance
- 8/28 IBL 3D high voltage channels cannot reach nominal bias voltage at end of Run 3
- Voltage limits at 1000 V for IBL planar, 600 V for Pixel
  - End-of-life test conducted up to 1000 V limit with IBL planar modules
  - A few HV channels permanently lost above 900 V in the process

Layer	2026 Bias Voltage [V]
B-Layer	600
Layer 1	400
Layer 2	400
Disks	400
IBL planar	650
IBL 3D	80

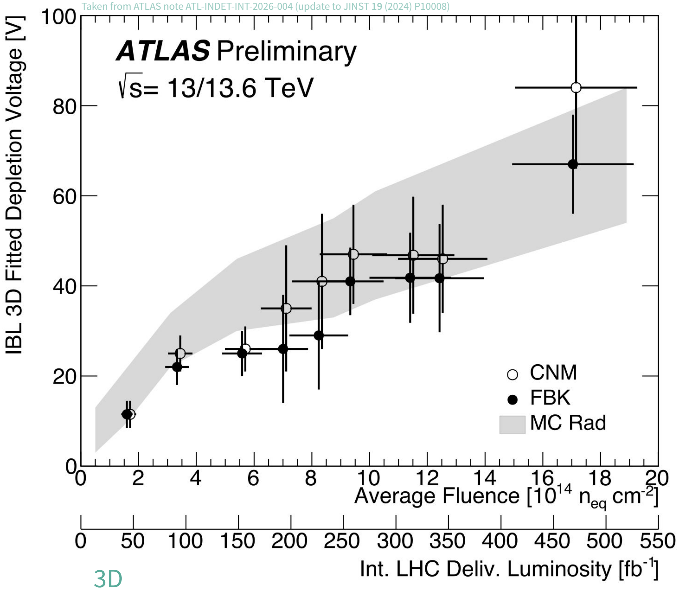
➤ High voltage scans needed to define operational strategy, even if some loss of physics data

Taken from ATLAS note ATL-INDET-INT-2026-003 (update to JINST **21** (2026) P07048)



Planar

Taken from ATLAS note ATL-INDET-INT-2026-004 (update to JINST **19** (2024) P10008)



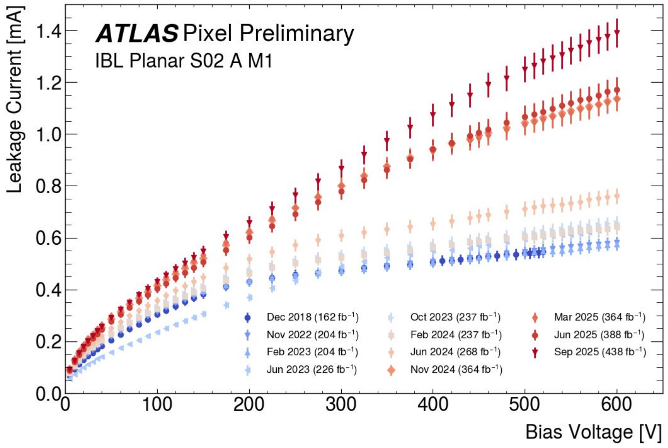
3D

Radiation Damage

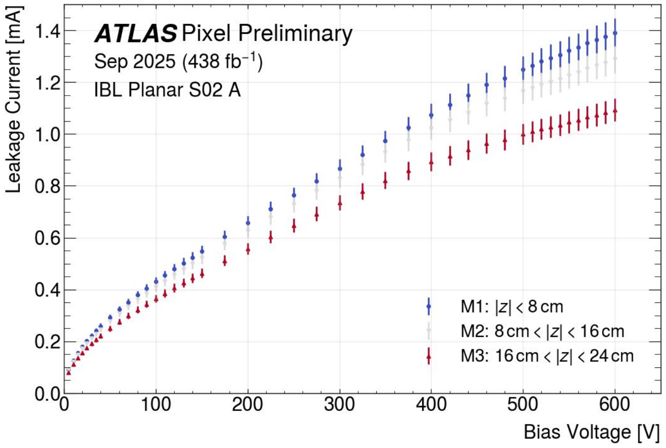
Leakage Current

- Conversion factor from luminosity to fluence provided by leakage current
- Evolution of leakage current monitored for detector safety
  - Dedicated I-V scans performed to inform yearly increases in bias voltage
  - No breakdown behaviour observed
- Leakage current remained low also thanks to limited annealing in cold detector condition

Plots taken from: https://atlas.web.cern.ch/Atlas/GROUPS/PHYSICS/PLOTS/PIXE-2025-02



I-V scan evolution (uncorrected for temperature effects)



Effect of module position

➢ Leakage current was no limiting factor, detector fully depleted for full lifetime

Conclusion

- ATLAS Pixel detector performed with minimal performance degradation for almost two decades
  - Despite high amount of received radiation damage & evolution of operational parameters beyond spec

- Many lessons learned about detector design and operational principles
  - Usage of off-the-shelf components in accessible positions where possible
  - Continuous development of off-detector data acquisition system critical to retain performance

- Collected valuable radiation damage data from highly irradiated detector and developed corresponding simulation model

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➤ Have a nice pattern ready for final threshold scan

Backup

Wirebond Oscillation Protection

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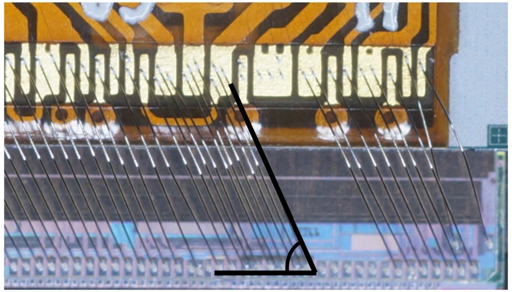
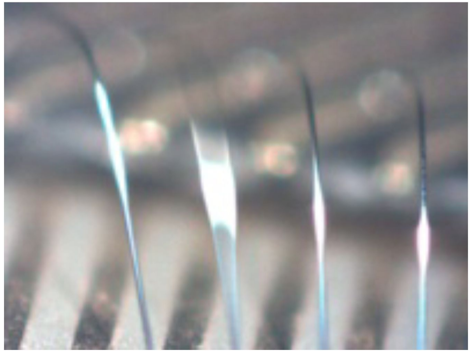
- No wirebond coating applied to IBL
  - Oscillation & wirebond failure observed in lab tests at fixed frequencies of 9 kHz - 25 kHz (depending on bond length)
- Fixed frequency trigger veto (FFTV) mechanism developed as operational safety precaution
- Problem mostly present during LHC fills with few colliding bunches
  - Simulations required to find permissible trigger rate limits
- Approval of Pixel & trigger experts required to release in operations
  - Lost physics data from trigger holds
  - Common issues from trigger noise spikes





➤ Initial prevention of operational safety issues preferable to later mitigation

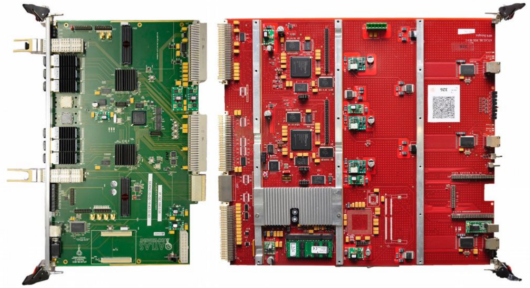
Off-Detector Read-Out Electronics

- Original Pixel read-out driver (ROD) & back-of-crate (BOC) developed together with ATLAS SCT strip detector

- Pixel ROD/BOC gradually replaced by IBL-developed hardware during LHC Run 2
  - Higher link bandwidth to cope with increased pile-up
  - Switch to calibration data transfer via ethernet
  - PowerPC included for control
  - Common code development possible to some extent

- Xilkernel on PowerPC replaced by Linux kernel before Run 3
  - Improved debugging capabilities & fewer software issues

- Separate test system set up as full detector slice for continuous development of software & firmware
  - Set up with automated tests of basic functionalities of new code versions



IBL-type ROD/BOC

➤ Opportunity to modernise hardware due to IBL addition,
separate test systems enable continued development & validation

Radiation Damage

Depletion Voltage

- IBL planar gradually loses distinction between non-depleted and depleted regime with increasing fluence

Plots taken from: JINST **21** (2026) P07048