ÖAW Österreichische Akademie der Wissenschaften

MARIETTA-BLAU-INSTITUT FÜR TEILCHENPHYSIK

# OCTOPUS: A MAPS demonstrator for future Lepton Collider Vertex detectors

**Thomas Bergauer** (MBI Vienna)
on behalf of the OCTOPUS DRD3 project

PSD14 Workshop September 2026
Queen Mary London

# Outline

- Vertex-detector R&D target: **FCC-ee**
- **65 nm MAPS** technology evaluation
- Simulation-based **sensor optimization**
- OCTOPUS **design** status
- **Test chips** and submission plans
- Conclusions

# FCC-ee as result of ESPPU process

## European Strategy for Particle Physics Update (ESPPU) 2026

**Input:**

- 268 input proposals submitted here
- Physics Briefing Book ( published in Sept. 2025 in arxiv and CERN Yellow report)
- Project assessment (ESG WG 2a report)
- Input by national HEP communities (ESG WG1 report)

**Results:**

- **The electron–positron Future Circular Collider (FCC-ee) is recommended as the preferred option for the next flagship collider at CERN.**
  - A descoped FCC-ee is the preferred alternative option for the next flagship collider at CERN

Comparison of all proposed large accelerator proposals:

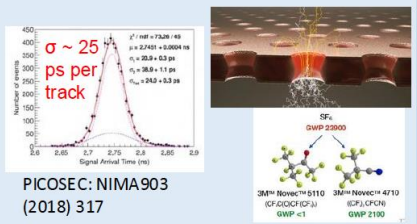
| Machine | Precision Physics | BSM physics | Physics vs CEPC | Technical readiness | Constr. cost (BCHF) | Time scale | Path to ≥10 TeV |
|---|---|---|---|---|---|---|---|
| FCC-ee | 22 | 23 | | | 15.3 | 2046-2060 | |
| Descoped FCC-ee | 15 | 17 | | | 12.9 | 2046-2055 | |
| LCF550 | 15 | 17 | | | 14.8 | 2045-2065 | |
| CLIC1500 | 14 | 18 | | | 14.6 | 2045-2066 | |
| LCF250 | 10 | 16 | | | 9.4 | 2045-2053 | |
| CLIC380 | 10 | 16 | | | 7.5 | 2045-2054 | |
| LEP3 | 15 | 17 | | | 4.1 | 2047-2062 | |
| LHeC | 8 | 7 | | | 2.1 | 2044-2051 | |

# ESPPU Recommendations on Detectors

i. *For the **DRD collaborations** to address the requirements of future flagship projects, they **must receive adequate funding**. New R&D topics and initiatives should be integrated in the DRD scheme. The General Strategic Recommendations in the roadmap must be fully addressed by dedicated initiatives coordinated across the DRD collaborations.*

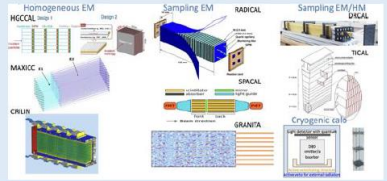
ii. *A coherent, strategic approach and sufficient resources to support **close cooperation with industry are required to address the rising costs and growing complexity in engineering, particularly in microelectronics.***

**DRD1: Gaseous Detectors**
Large · Fast · eco-friendly gases · MPGD, e.g. GEMs

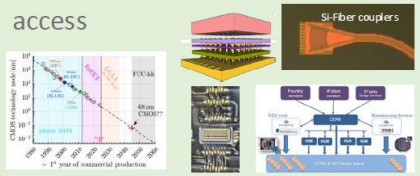



**DRD3: Semiconductor Det.**
Monolithic CMOS · LGADs · radiation hardness · interconns.

**DRD6: Calorimetry**
Energy resolution · High granularity · dual readout · particle flow · sandwich · optical

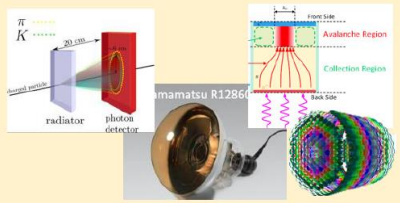


**DRD7: Electronics**
ADC/TDC IP Blocks · Opto-electronics · packaging · power · extreme environments · COTS · intelligence on detector · foundry access

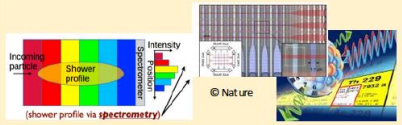



**DRD2: Liquid Detectors**
for Neutrinos · Dark Matter · 0vbb

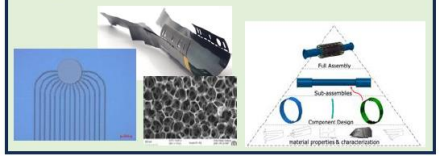

**DRD4: Photon detectors**
vacuum, solid-state (SiPM), hybrid single-photon and SciFi detectors · applications in PID and RICH




**DRD5: Quantum Sensors**
Quantum dots · superconduct. nanowires · bolometers · TES · MMC · nuclear clocks
Applications in LEPP, first projects in HEPP happening




**DRD8: Mechanics**
Ultra-thin beam pipes · CF foam and new materials · curved, retractable sensors · air & micro-channel cooling · eco-friendly ccoling fluids · robots · augmented reality

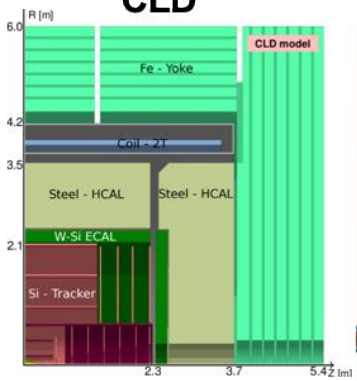


# All FCC-ee detector concepts plan for MAPS sensors as vertex detectors

V. Cairo FCC week 2026

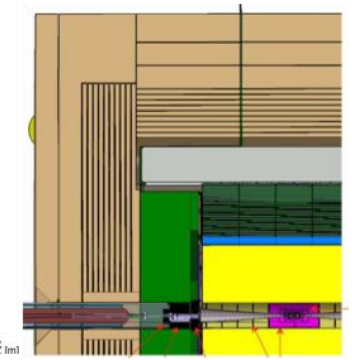
**Legend:** Inner Tracker, Outer Tracker, Wrappers

## CLD



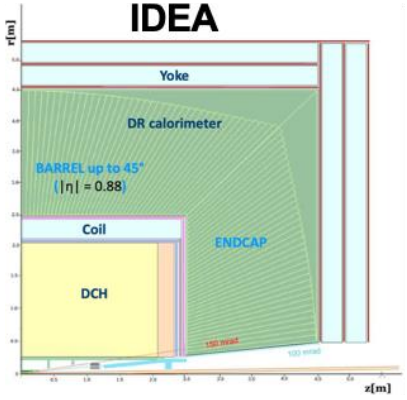

- Evolved from CLIC detector
- Silicon vertex with 25µm pixels
  - Geometry with ALICE ITS approximation → FCC-SEED
- Silicon tracker with 50µm strips
  - Sensors plus ASICs or monolithic structure or MAPS
- ARC (Array of RICH Cells) Lightweight with 20cm radial depth
  - Two radiators (gas + aerogel)

## ILD



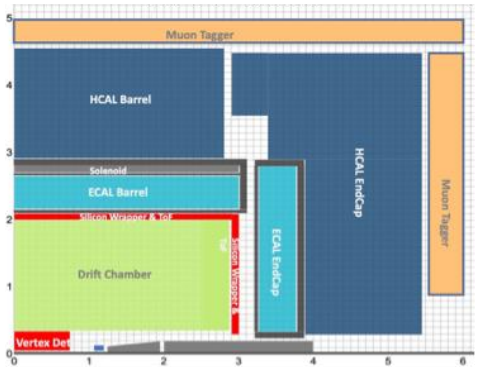
- Initial design for ILC
  - Significant changes for FCC-ee
- Silicon Vertex
  - Currently borrowed from CLD for simulations
- TPC as outer tracker
  - Studying different layouts varying the inner Radii
- Silicon External Tracker for ToF + momentum resolution

## IDEA



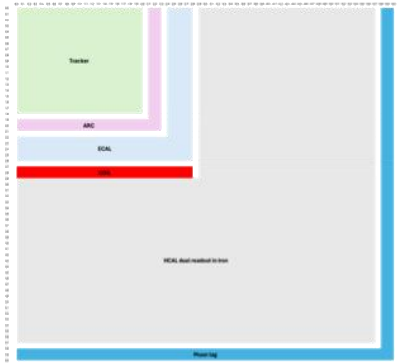

- Conceived for FCC-ee
- Silicon vertex tracker
  - Outer based on ATLASPix3 with 50x150µm² pixels
  - Inner ARCADIA based 25x25 µm² pixels
- Outer tracker based on low mass Drift Chamber
  - 112 layers
  - 4m Long
  - R = 35-200cm
- Silicon wrapper
  - either with MAPS with with ~$10^{11}$ channels!
  - or CMOS-LGADS ~40ps

## ALLEGRO




- Conceived for FCC-ee, started with a noble-liquid calorimeter
- Tracking system taken from IDEA
- Silicon Vertex with curved or straight sensors
- Outer tracker with
  - Extended Drift Chamber
  - Straw tubes
  - Scintillating Fiber Tracker (SciFi)
    - 5m Long
    - R = 35-200cm
- Silicon wrapper
  - Monolithic pixel or AC-LGADs

## ALFA



- Newly Conceived project for FCC-ee
- MAPS tracker following ALICE ITS3 developments
  - Vertex curved MAPS 65 nm CMOS TPSCo 10x10 µm² pixels
  - Outer tracker Reticle-size MAPS,
    - 25x32 mm² to 50x128 mm² module
- ARC (Array of RICH Cells) Lightweight with 20cm radial depth
  - Two radiators (gas + aerogel)

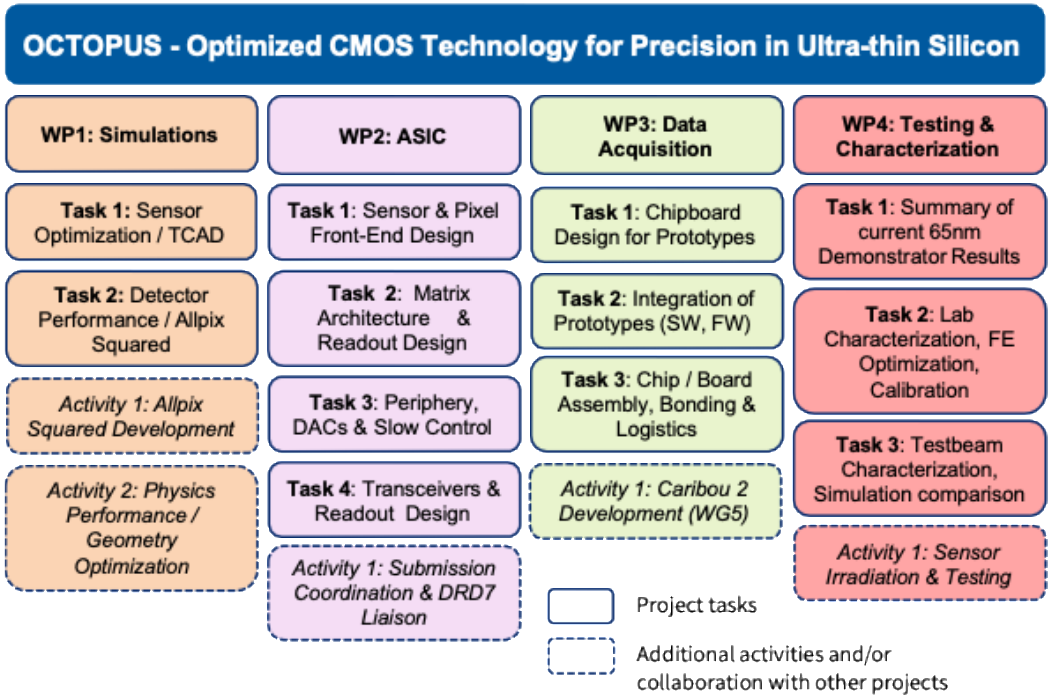
# OCTOPUS Project

**OCTOPUS: Optimized CMOS Technology fOr Precision in Ultra-thin Silicon**
(octopus.web.cern.ch)

DRD3 R&D project towards vertex detectors for Future Lepton Collider (FCC-ee)

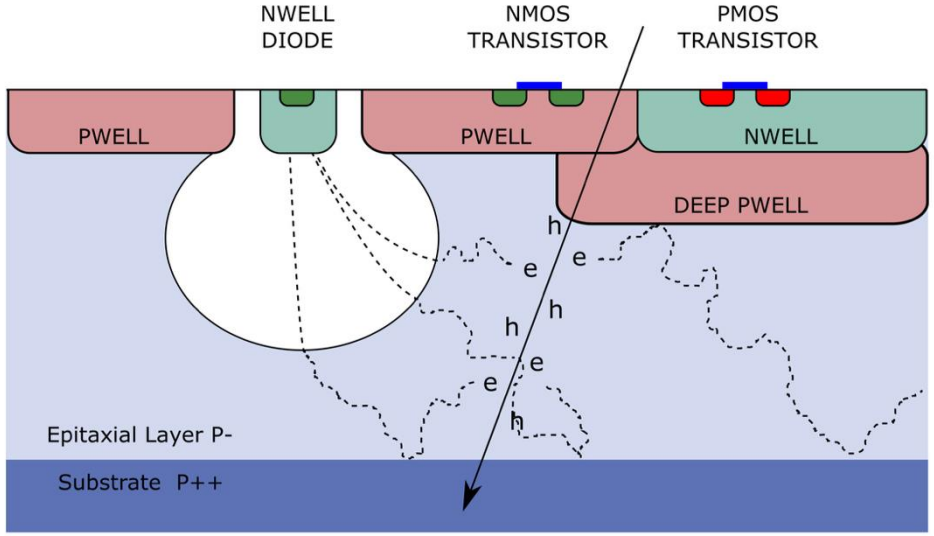
- Develop reticle-size CMOS MAPS sensors
- Intermediate target: sensors for new beam telescopes
- Current technology used: TPSCo 65 nm process

- Full R&D chain performed by 13 institutes across Europe
- Collaboration with MANTA project for outer tracker layers
  → Exploring synergies for frontend and readout design

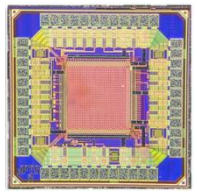


# 65 nm CMOS Imaging Process for MAPS

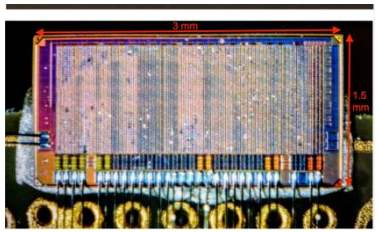
- Strongly driven by ALICE with ITS3 as the first application
- Candidate technology for ALICE3 (ALMIRA) and FCC-ee vertex developments
- Access through CERN EP R&D for DRD3/7, many institutes + other projects
- Encouraging results from common productions in 2021-22:
  - Process modifications working
  - Stitching to larger sensors than reticles
  - Fully efficient at small pitch, <100 ps sensor timing, radiation hardness $10^{15} n_{eq} cm^{-2}$, thinned to <20µm
- Several demonstrator chips exist



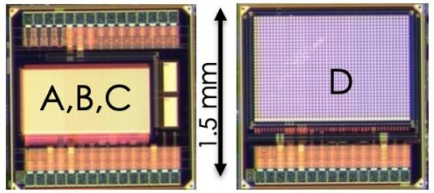

DPTS, 15 µm pitch, CERN



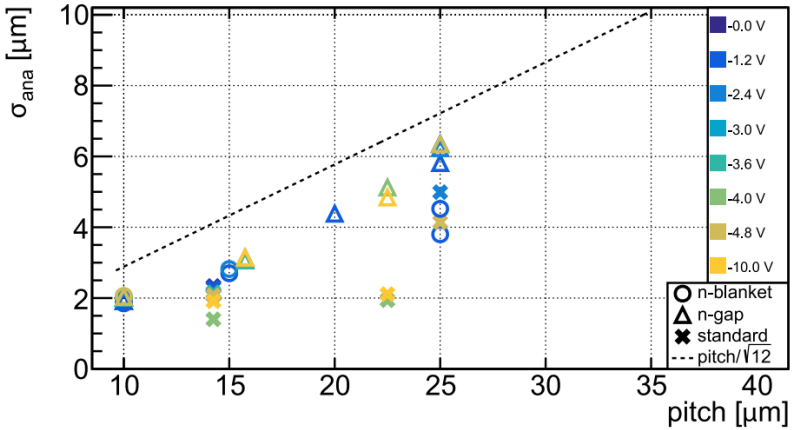
H2M, 35 µm pitch, DESY/CERN



CE-65, 15-25 µm pitch IPHC




Achieved TB position resolution vs. pitch (analog readout)




Comprehensive review of 65 nm results: *F. King et al.*, https://doi.org/10.1016/j.nima.2026.171672

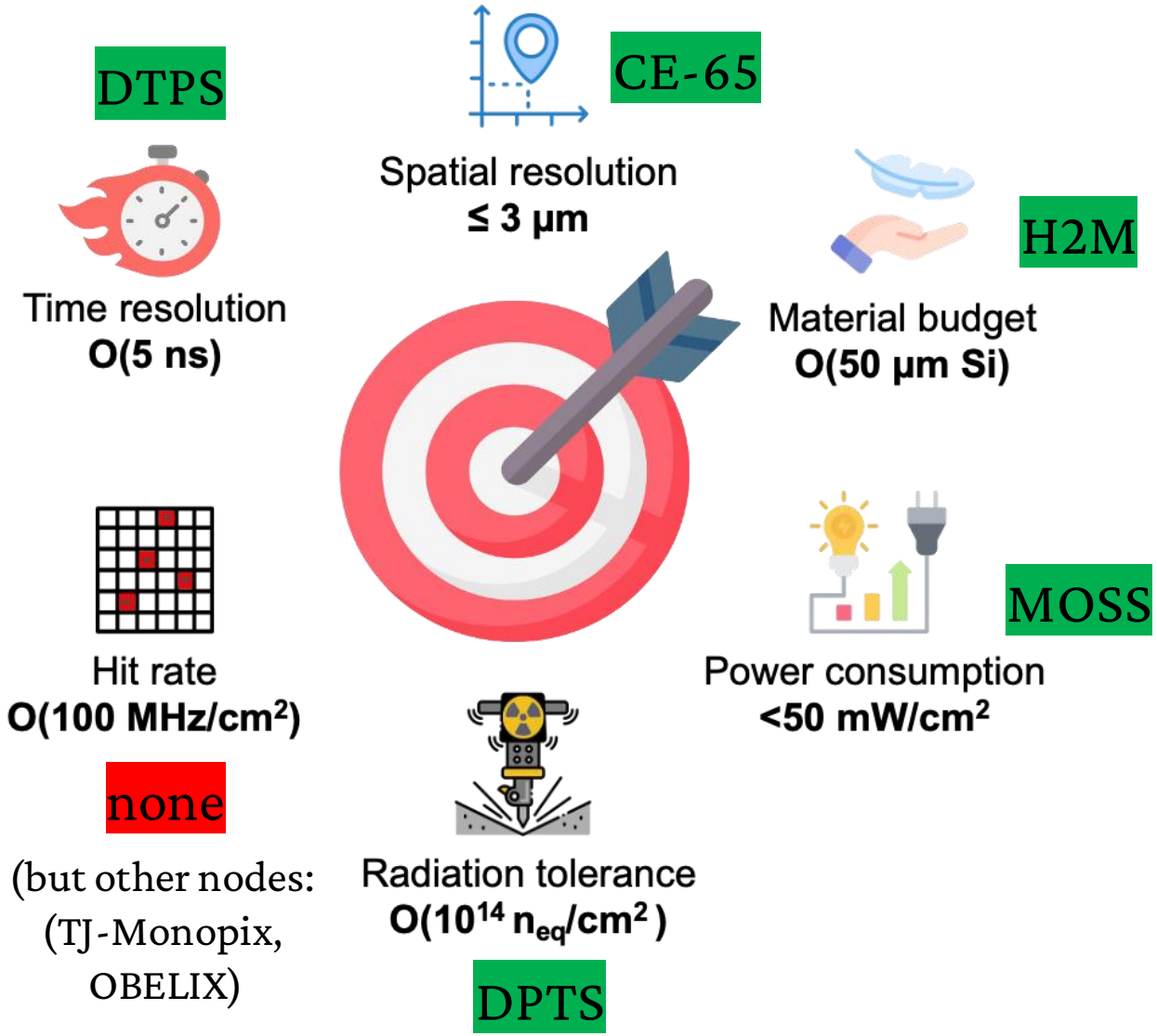
# Where do we stand?

FCC-ee as a lepton collider requires a re-thinking of requirements compared to hadron collider R&D:

- Moderate radiation hardness ~ $10^{14}$ $n_{eq}cm^{-2}$
- Spatial resolution < 3 µm
- Material budget/power consumption requirements are extremely low
- Hit rates 100 MHz/ $cm^2$ (for Z-pole running)

Most requirements are already achieved by the state of the art, but always at the cost of another performance parameter

- **The main project challenge is to achieve all targets in one chip**



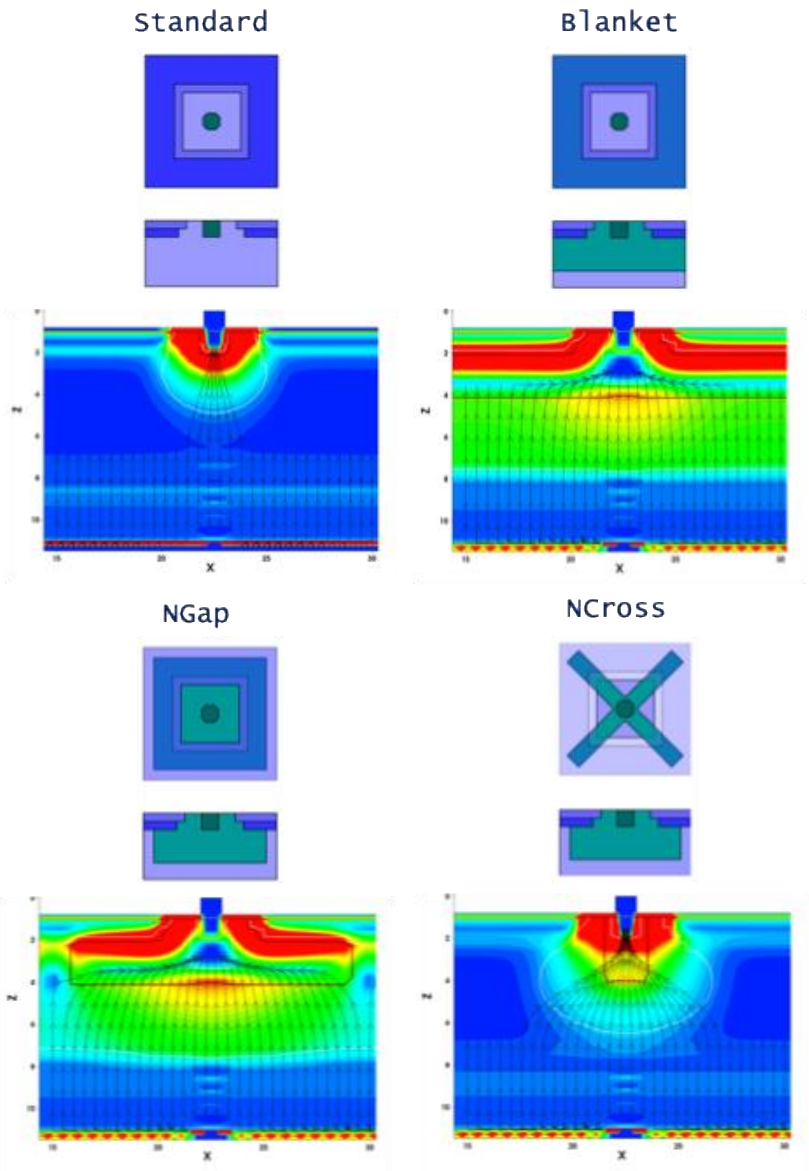
# Process Variants and new *NCross*

*Standard* process: undepleted volume around the pixel boundary below the deep p-well

- Limiting charge collection, timing performance and radiation hardness

➔Process modification introducing a low-doped layer
  ➔first homogenous "*blanket*" design
  ➔later patterned in the N*gap* design"
  - still suffering from a low electric field inside the doped layer

OCTOPUS development: *Ncross* ➔ Balance between collection time, resolution and efficiency

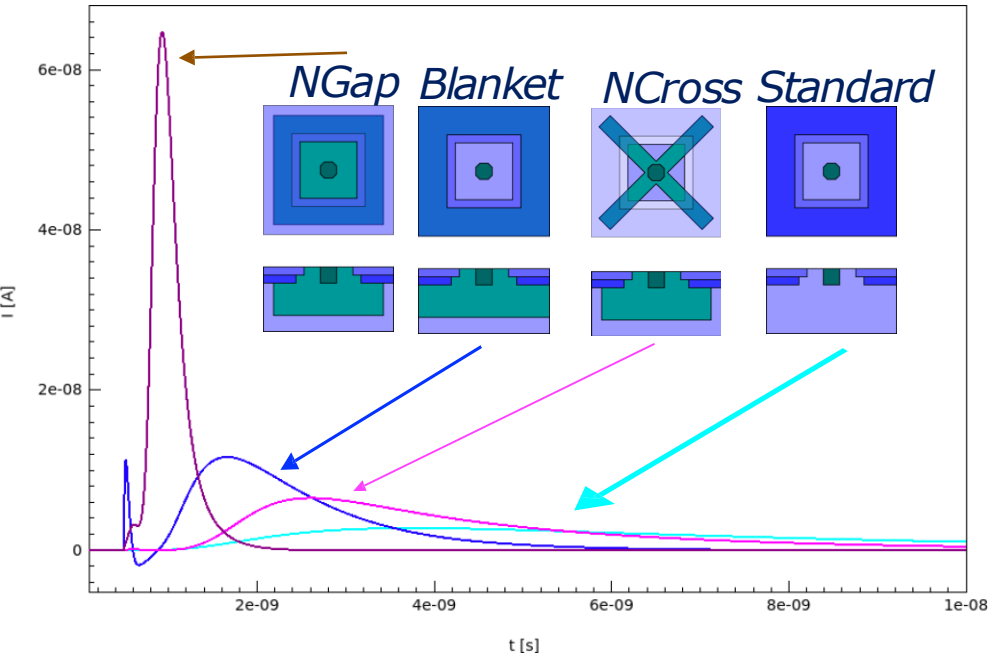


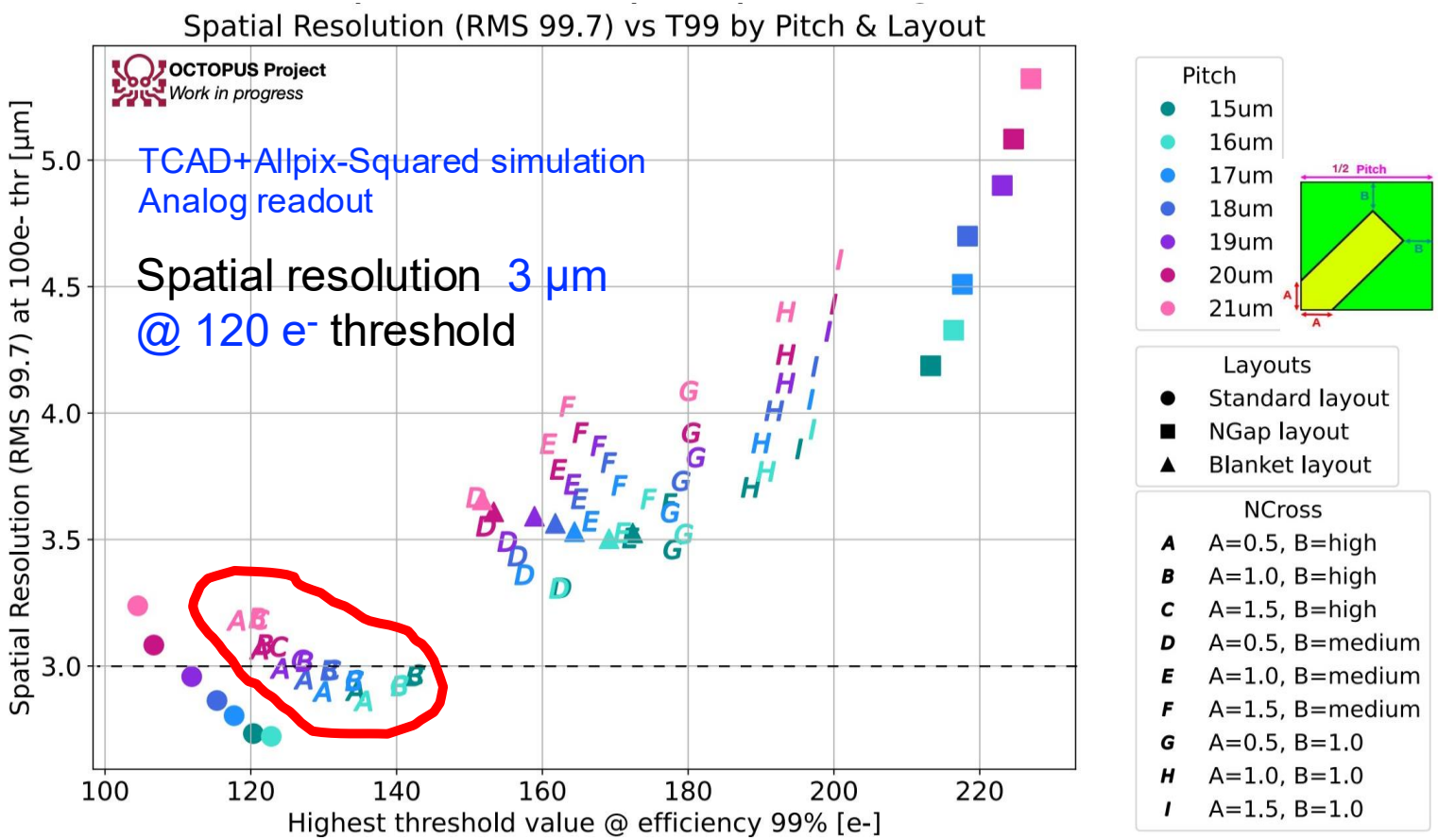

*A. Velyka, https://indico.desy.de/event/51462/contributions/197351*

# *Ncross* Sensor layout optimization

- Sensor-design optimization with TCAD + Allpix² MC simulations
- NCross layout combines 3 µm position resolution with adequate CCE and timing for ~20 µm pitch
- Currently in simulations only

Pixel-corner transient simulation

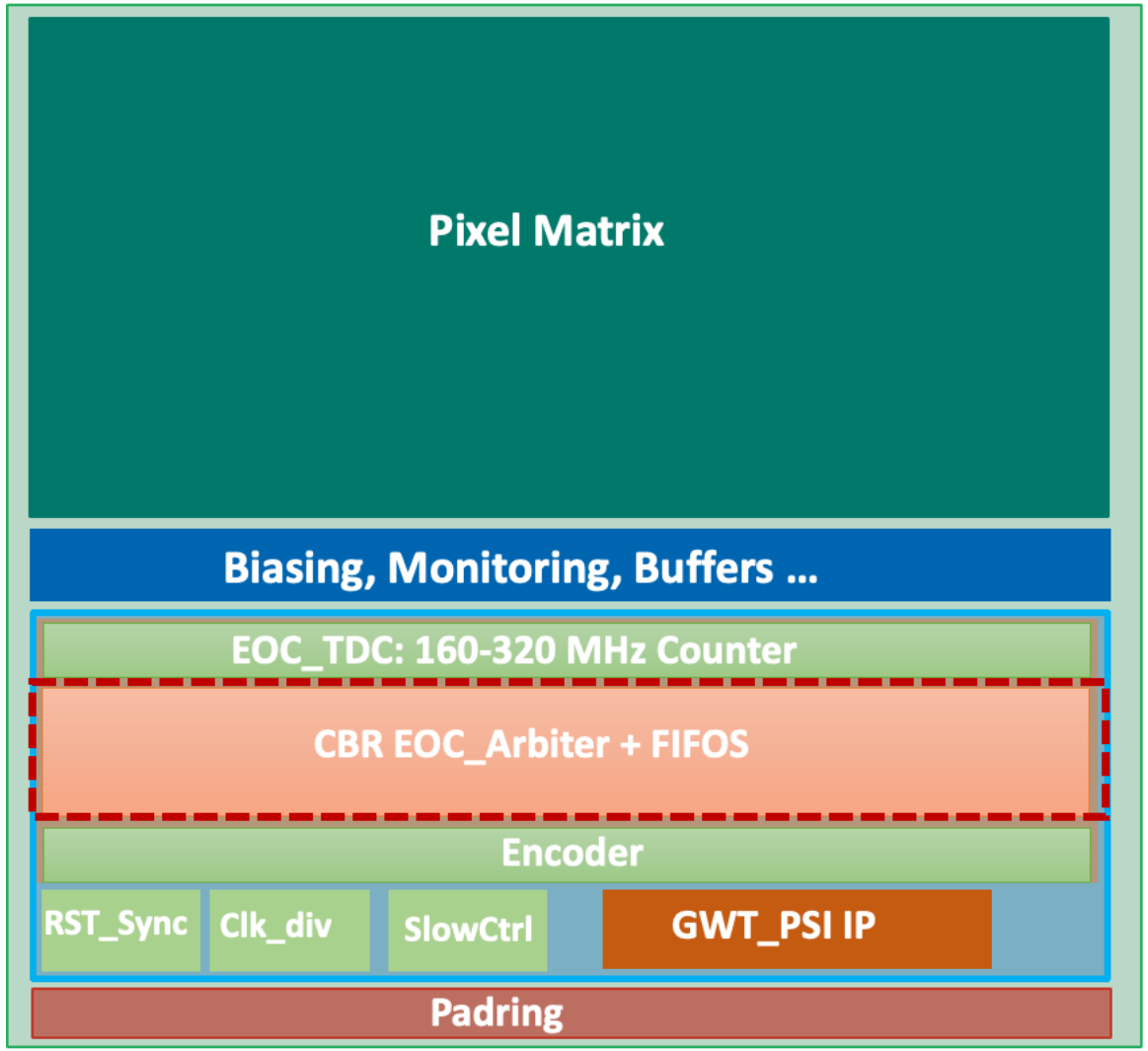


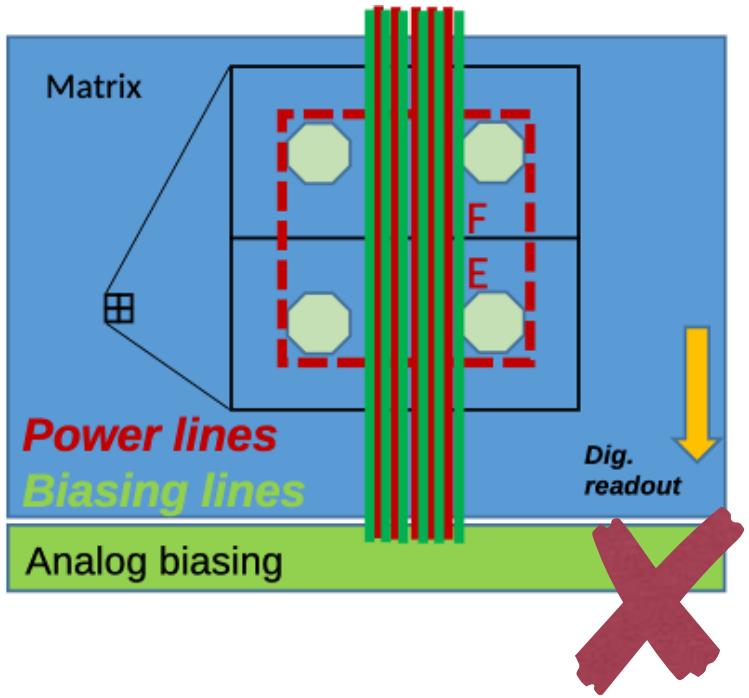
# OCTOPUS design overview

- Target full reticle chip, no stitching
  - Matrix size ~ 2 cm x 3 cm (final chip)
  - Matrix with 1024 rows x ~1500 columns
  - Pitch ~20 µm
- Analog frontend based on DPTS
- Readout by fully **asynchronous priority arbiter (APA)**
- Chip periphery only at the bottom (3-side buttable)

OCTOPUS chip schematic

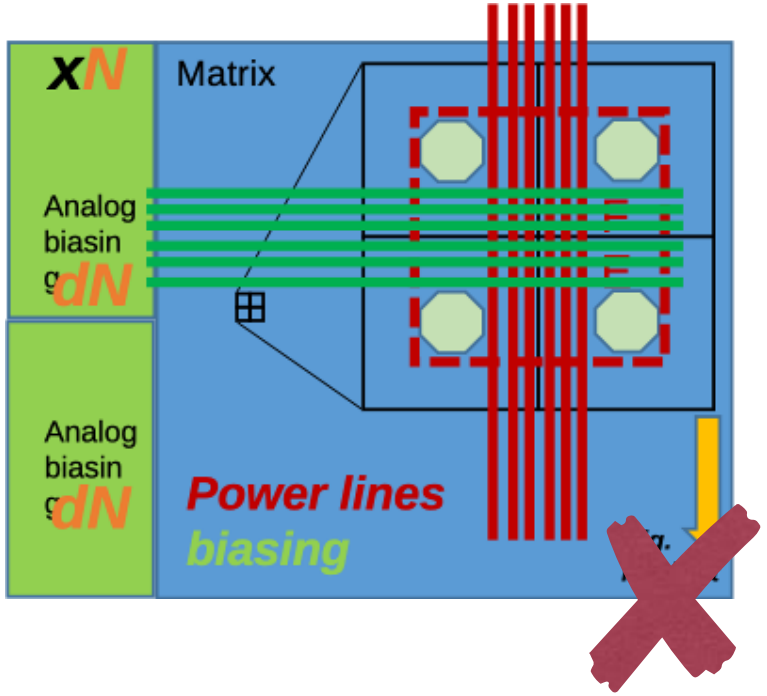


# Analog biassing schemes



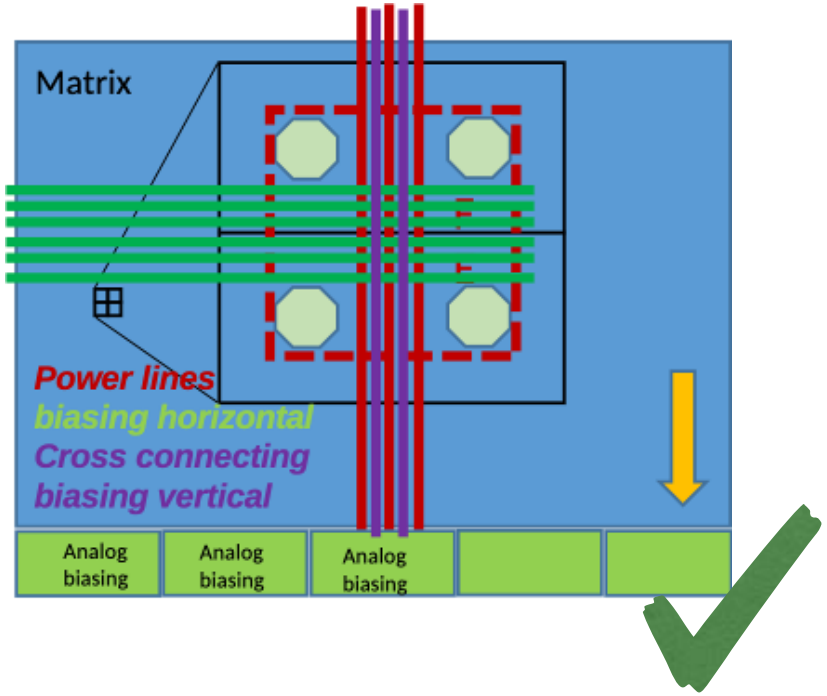

**Biasing full column from bottom periphery**

- Column segments driven by total capability of bias block
- ~5mV voltage drop to top
- Will cause threshold dispersion and operating point differences




**Biasing from the side**

- Independent biasing block compensating the power drop
- Additional periphery on the sides
- Chip will not 3-side buttable ➔ inactive sections in vertex detector




**Biasing from the bottom, but local distribution**

- Create biasing regions
- Compensation of voltage drop
- Needs careful shielding of digital lines to suppress crosstalk

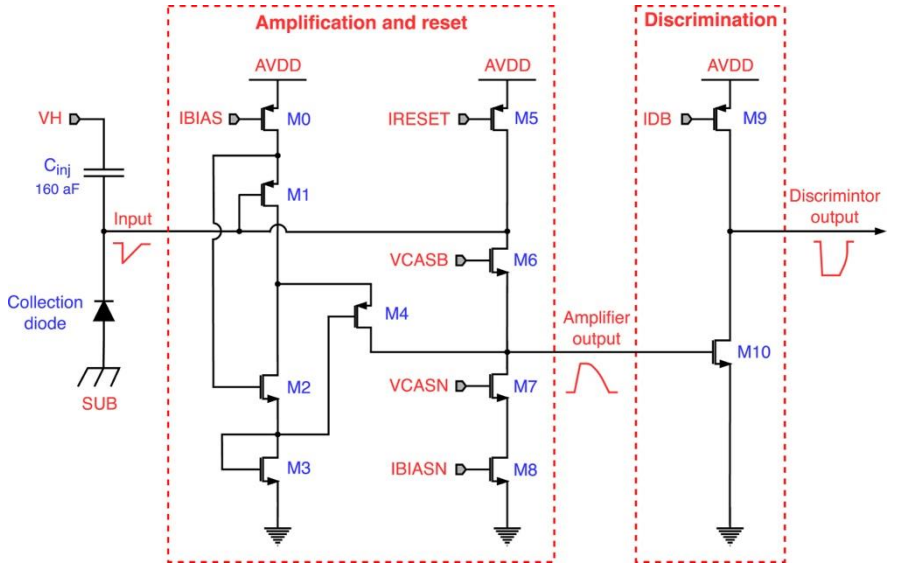
# Analog frontend

Analog FE based on DPTS amplifier + discriminator

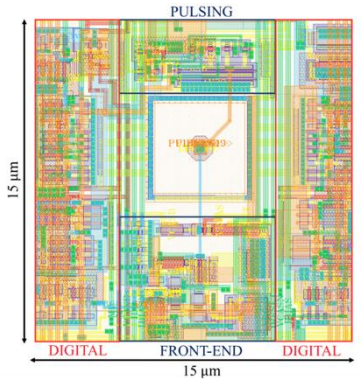
- Small footprint → leaves space to place digital circuitry
- Low power - tuneable from 12 nW to 5 µW / pixel
- Uncorrected MIP time resolution 30 ns @ 120 nW / px (dominated by time walk) at 120 nW / px (~ 30 mW/cm²) analog power at 20x20 µm² pitch)

- Time-over-Threshold measurement required to:
  → correct for time walk offline → time resolution down to 6 ns @ 120 nW / px
  → improve spatial resolution by charge interpolation

DPTS analog frontend



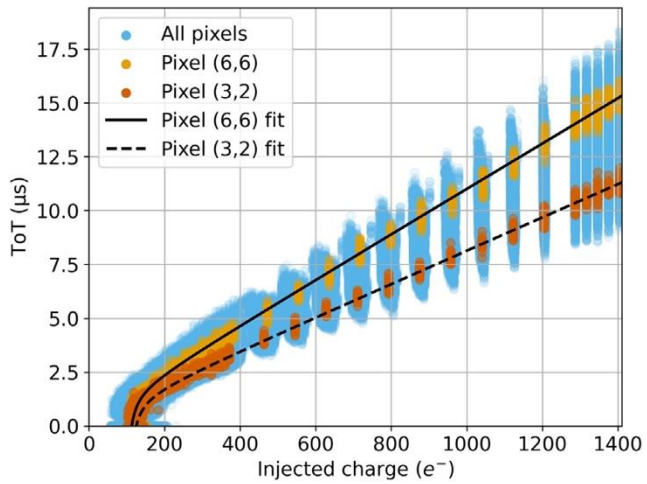

DPTS analog pixel




**DPTS Pixel: 15 µm x 15 µm**

F.Piro, A Compact Front-End Circuit for a Monolithic Sensor in a 65-nm CMOS Imaging Technology, 09.09.2023, IEEE Transactions on Nuclear Science

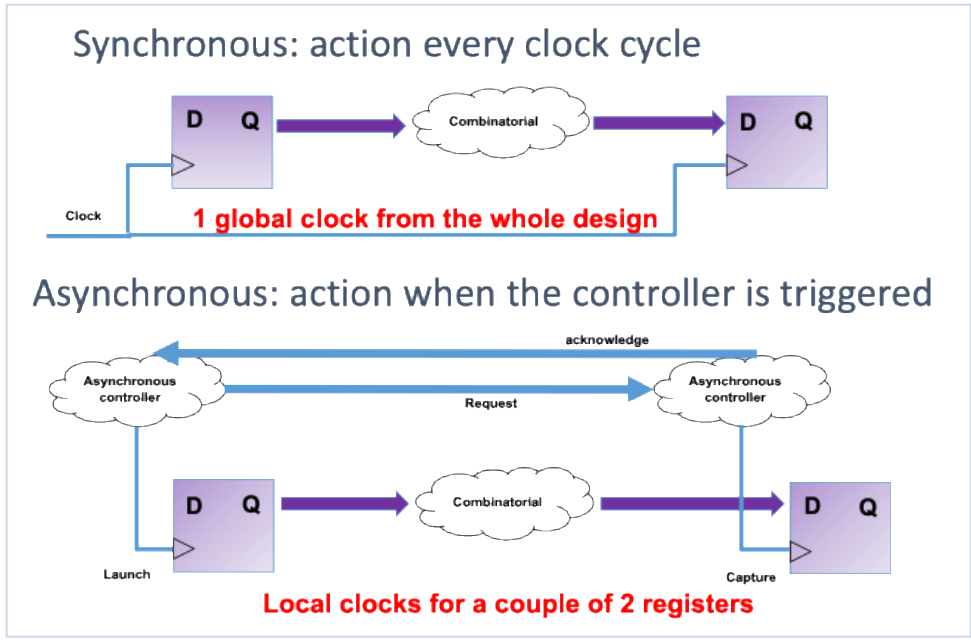
DPTS time-over-threshold

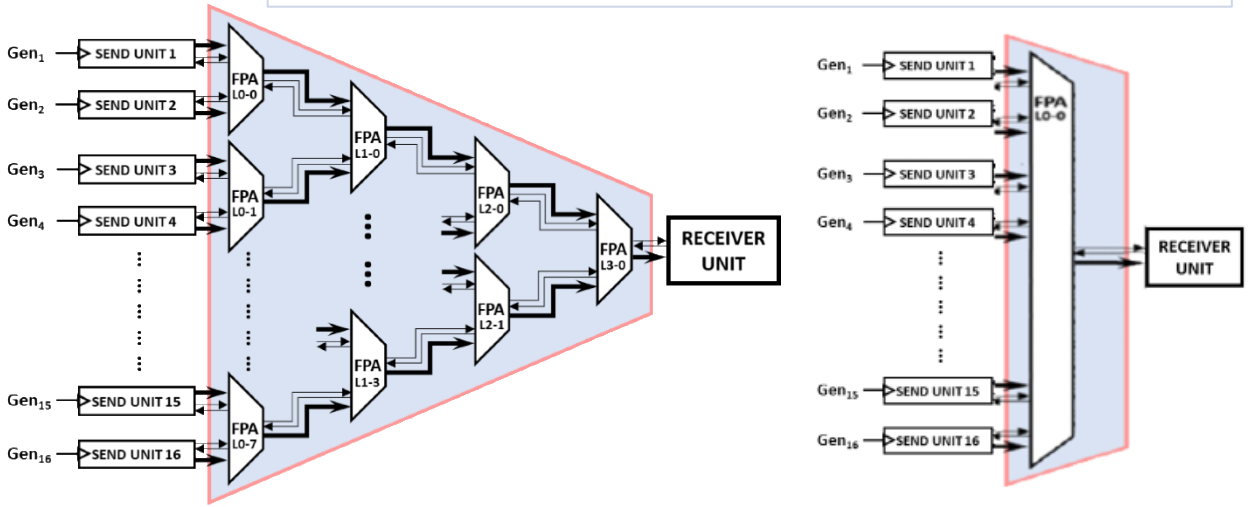


# Matrix Readout

Asynchronous Priority Arbiter (APA) readout scheme

- High-rate readout at low power
- Pixel grouping and multi-column readout
- Data-driven hit readout through arbiter tree
  - No clock in matrix (TDC time stamping in periphery)
    - Request prioritization, address forwarding, acknowledgement
    - Jitter of APA < 8ns (simulation); offline correction possible
- Compact scheme ➔ fits in <= 20µm pitch
- Resolution <5ns feasible
- 65nm proof-of-concept test chip SPARC (IPHC) currently under test → see next slides



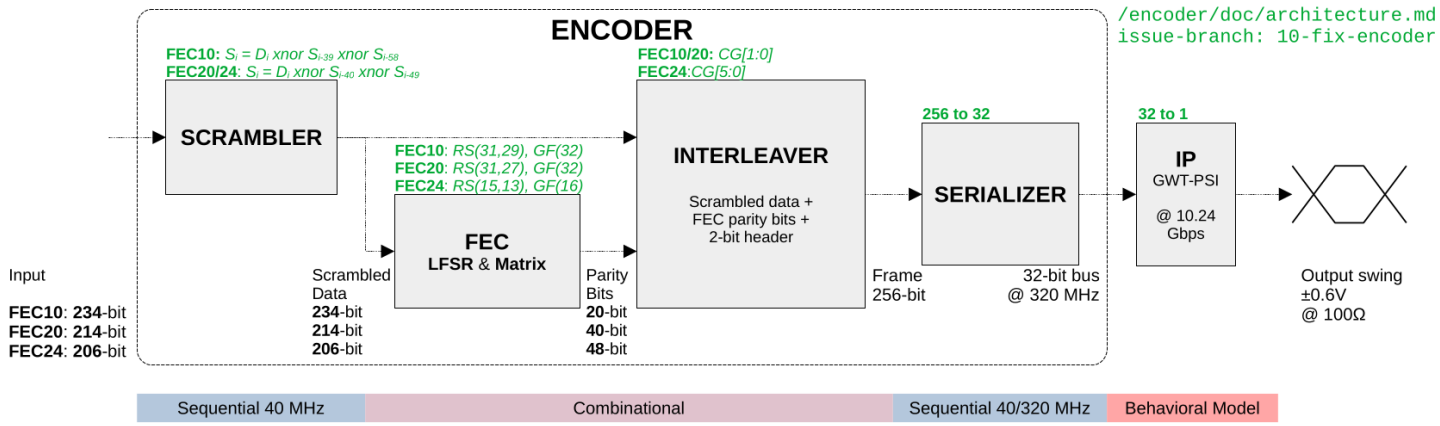



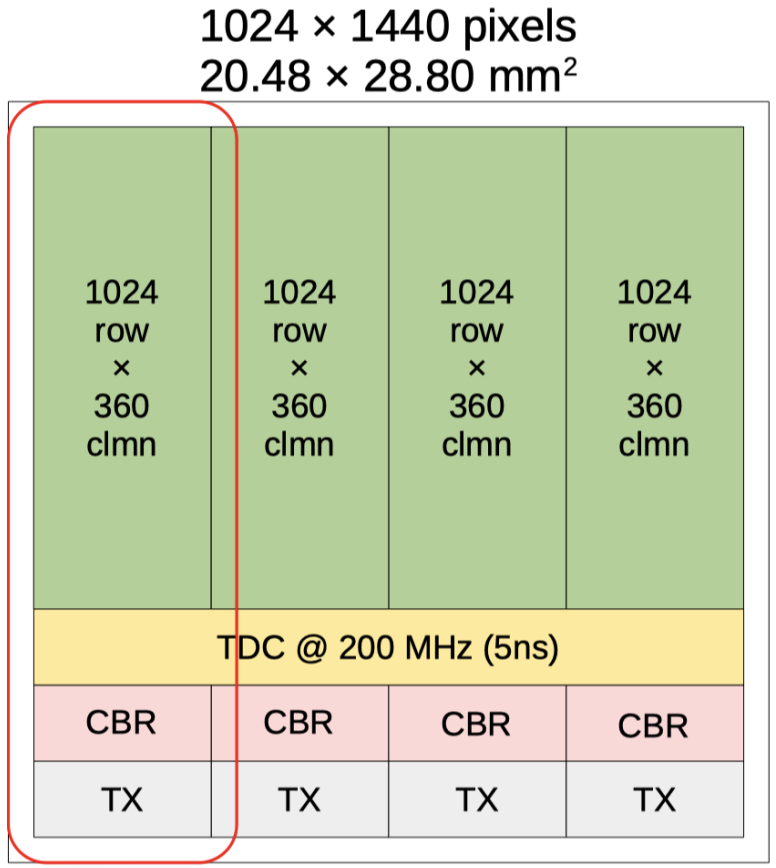

https://indico.desy.de/event/51462/contributions/197348/

# End-of-Column readout and structure

- Current baseline: triggerless readout of 100 Mhz/cm² with matrix read out via asynchronous priority arbiter (APA)
- Data merging happens in End of column (EOC):
  - 5 ns TDC precision for time stamping
  - Buffering of hits (depth is being optimized)
  - Column merging logic (different options)
- Combination of columns into Readout Unit (ROU)
  - 1 ROU feeds one high-speed link
  - EoC encoder own development (based on the lpGPT manual only)

- FEC10/**20**/24 with 234/**214**/206 payload
  - **RTL completed** - Ready for High-level modeling & Top-level simulations




One Readout Unit


Gianpiero Vignola, DESY
Roberto Russo, MBI
Zdenko Janoska, CTU

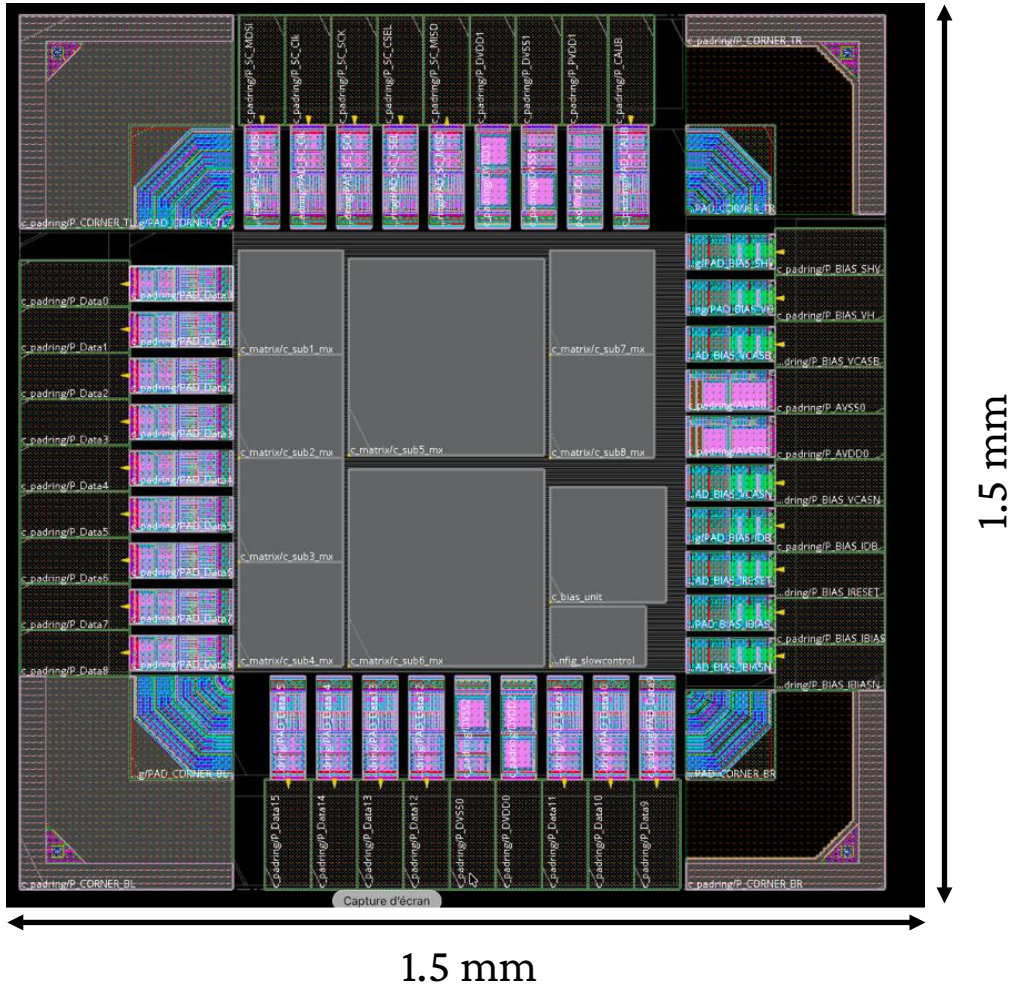
# Prototype Chip: OCEAN-65

OCEAN-65: Combined OCTOPUS/MANTA chiplet

- 8x8 pixel matrices with inner 4x4 active pixels using the *Ngap* process variant
  - Exploring different front-ends
    - AC and DC coupling
    - Different FE variants: DPTS-like FE, alternative approaches by CPPM and IPHC
  - Layout in progress ➔ verification and simulation ongoing

Additional chiplets for exploring n-layer layout variants NCross (using APTS structure)

- Submission on ITS3 ER3 submission (Q4/2026)

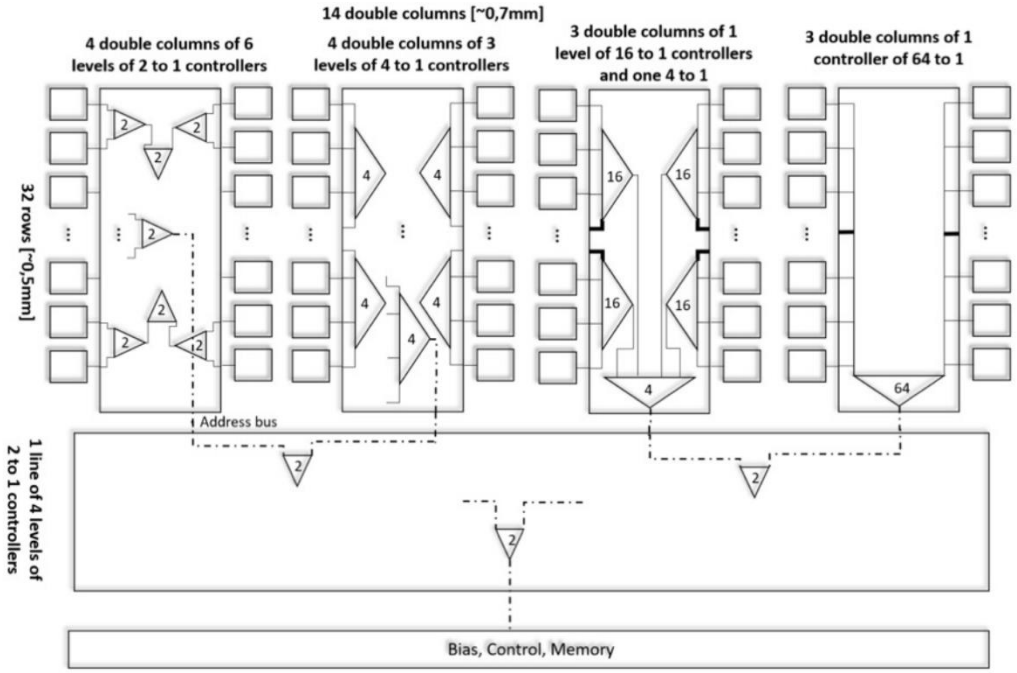


# SPARC APA Test Chip

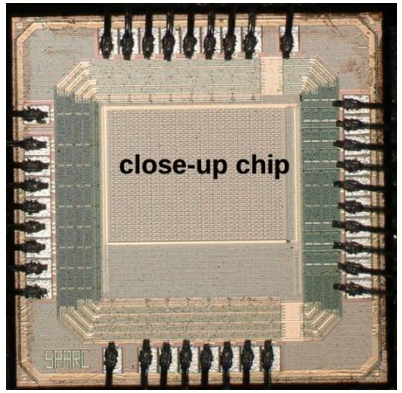
- Designed by IPHC Strasbourg and produced in ALICE-ER2 submission (1.5 x 1.5 $mm^2$ chiplet)
- 22.8 µm x 14.4 µm pixel size, 28 x 32 pixel matrix
- 28 columns read out by arbiters in a double column structure) in 4 different arbiter sizes and # of level

OCTOPUS institutes participate in characterization (lab + beam tests) using Caribou DAQ system

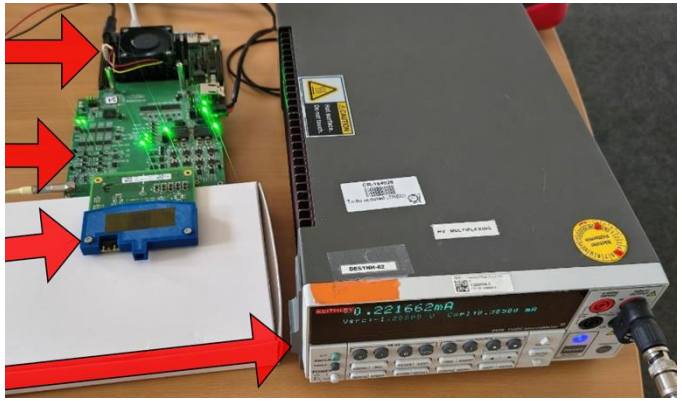
- Encouraging initial test results → Chip fully functional
- High-rate tests to study APA performance and optimization



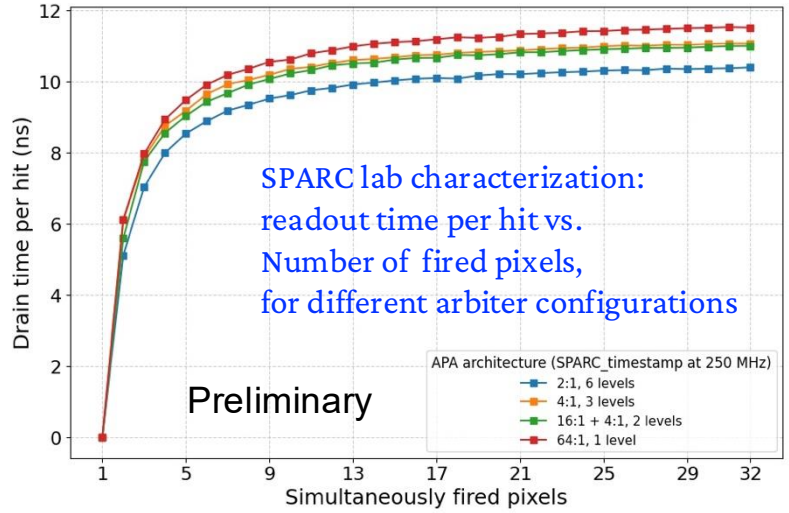

SPARC on test board




SPARC Caribou Lab setup



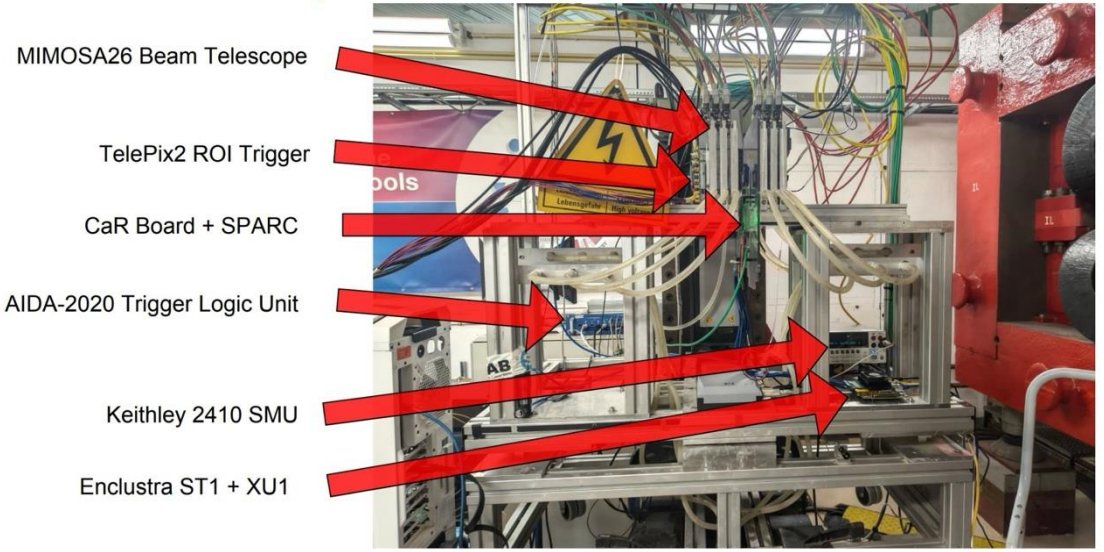
| Controller size | Number of levels |
|---|---|
| 2 to 1 | 6 |
| 4 to 1 | 3 |
| 16 to 1 + 4 to 1 | 2 |
| 64 to 1 | 1 |

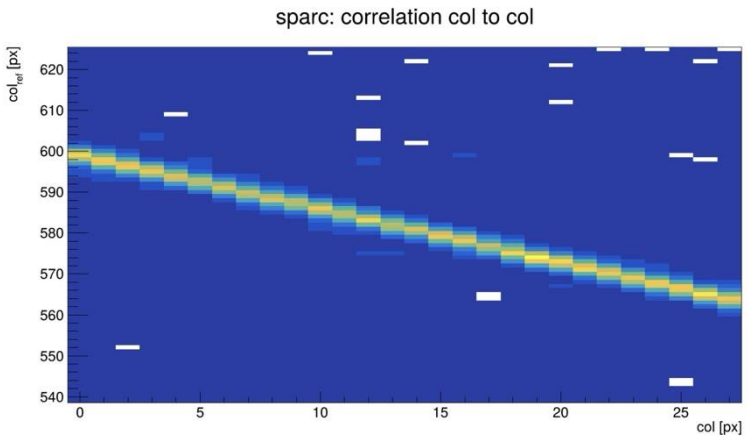


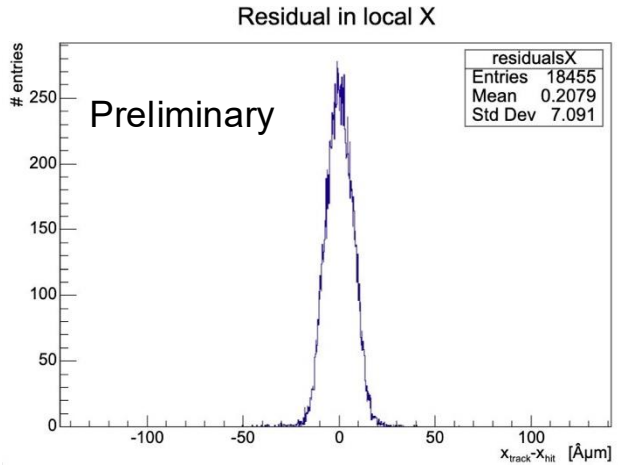

*J. Baudot, DRD3 week June 2026, https://indico.cern.ch/event/1634258/contributions/7142460*

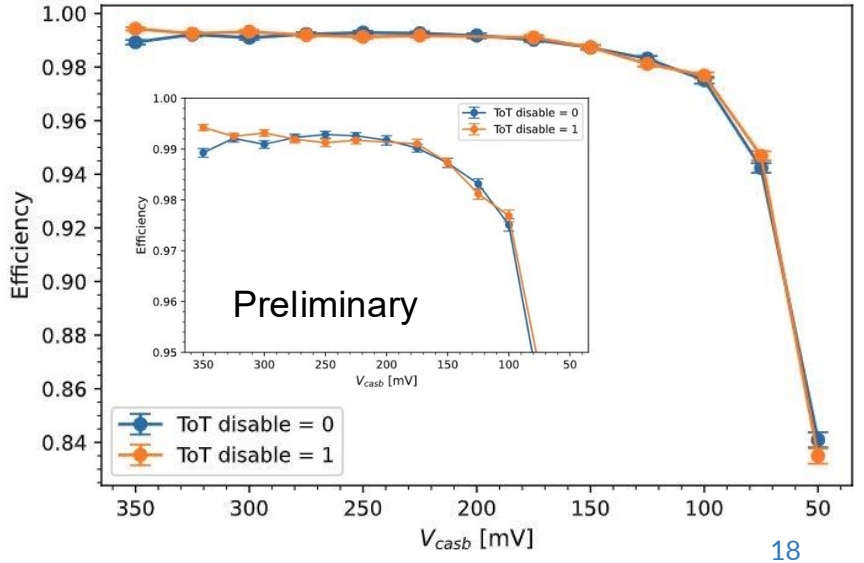
# SPARC Test Beam

- Very early results from beam test 29.6. to 5.7. 2026
  - Chip became available only very shortly before
- DESY beam line 21: 5.8 GeV electrons
- Using Mimosa telescope and analysis with Corryvreckan resulted in ~7 µm spatial resolution (roughly corresponds to binary res.)
- Efficiency close to 99% down to the threshold of 150 mV $V_{csab}$ (~200-250 $e^-$)



# Summary & Conclusions

- DRD3 OCTOPUS project aims to develop **MAPS sensor compatible with FCC-ee vertex detector needs**: 3 µm position resolution, 100 MHz/cm$^2$ hit rate, low power <50mW/cm$^2$ and material budget of 50µm Si equivalent
  - Reaching all performance targets **simultaneously** remains challenging
  - TPSCo 65 nm technology shows promising performance for reaching requirements

- Synergy and common developments with ***MANTA project*** for large-area tracker chip

- Systematic sensor and circuit optimization for OCTOPUS vertex-detector MAPS, based on detailed simulations and several generations of test chips:
  - Characterization of SPARC chip in lab and test beam (study of APA readout)
  - Design/submission of OCEAN-65 in Q4/2026
  - First full-size prototype ("beam-telescope sensor") to be submitted end of 2027

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# Thank you very much for your attention

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