Laboratory Session:
GRUPO G10-1.

TIDPAN
Valencia 2026
del 15 al 26 de junio

P10 Introduction to Hierarchical Trigger Systems: From FPGA Level-1 to High-Level Software

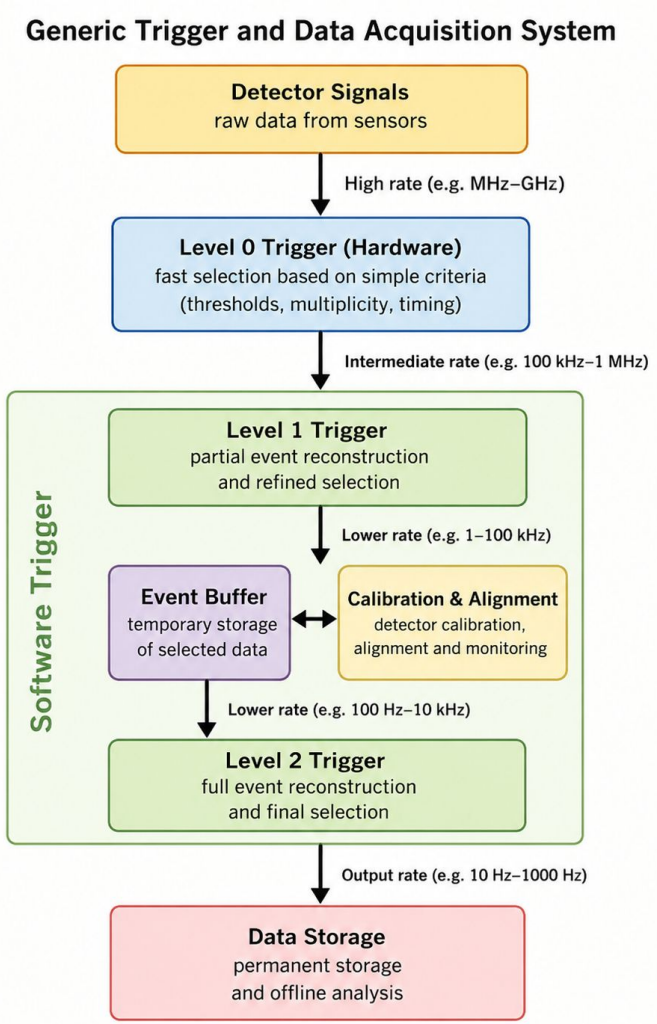
A. Navarro Tobar, J. Prado Pico, C. F. Bedoya, S. Folgueras

TIDPAN 2026 - Taller de Instrumentación y Detectores en Física de Particulas, Astropartículas y Nuclear

In this lab we would like to train on instrumentation and techniques used by Trigger systems

Why Trigger is important? => talk by S. Folgueras

To start with: **Trigger ends up being likely a hierarchical system**



How trigger systems look like?

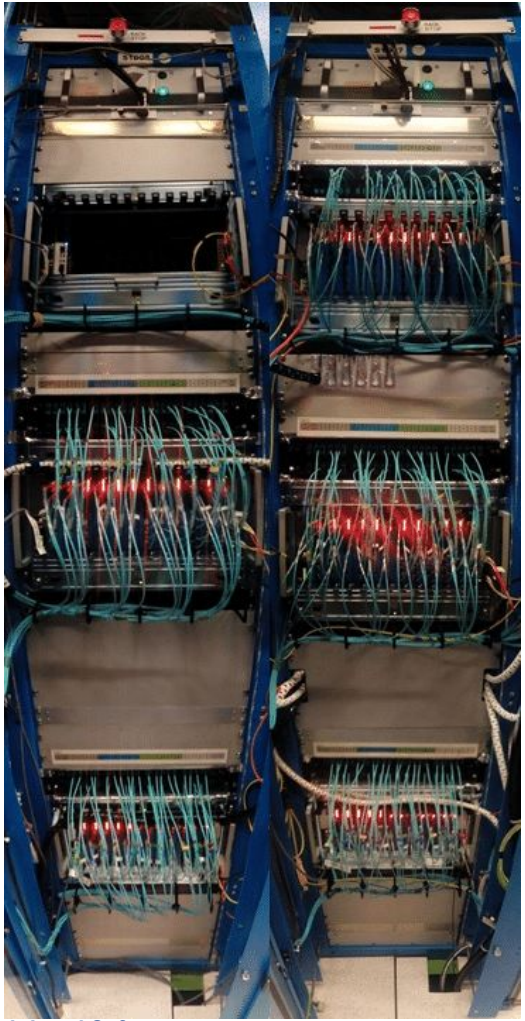
Modern trigger systems combine different layers of technologies to process enormous data volumes in real time and make rapid decisions.

High-Level Trigger (HLT): computing technologies

- Commodity computing infrastructure.
- Multi-core CPUs, servers, and GPU accelerators.
- Software-based event reconstruction and selection.
- Flexible algorithms that can be updated as requirements evolve.

Low-Level Triggers (Level-0 / Level-1): high speed digital technologies

- Ultra-fast digital electronics operating at the detector readout rate.
- Field-Programmable Gate Arrays (FPGAs) for real-time processing.
- High-speed optical links and networking technologies.
- Modular hardware architectures for scalability and maintainability.
- Deterministic, low-latency decision making within microseconds.



This lab:

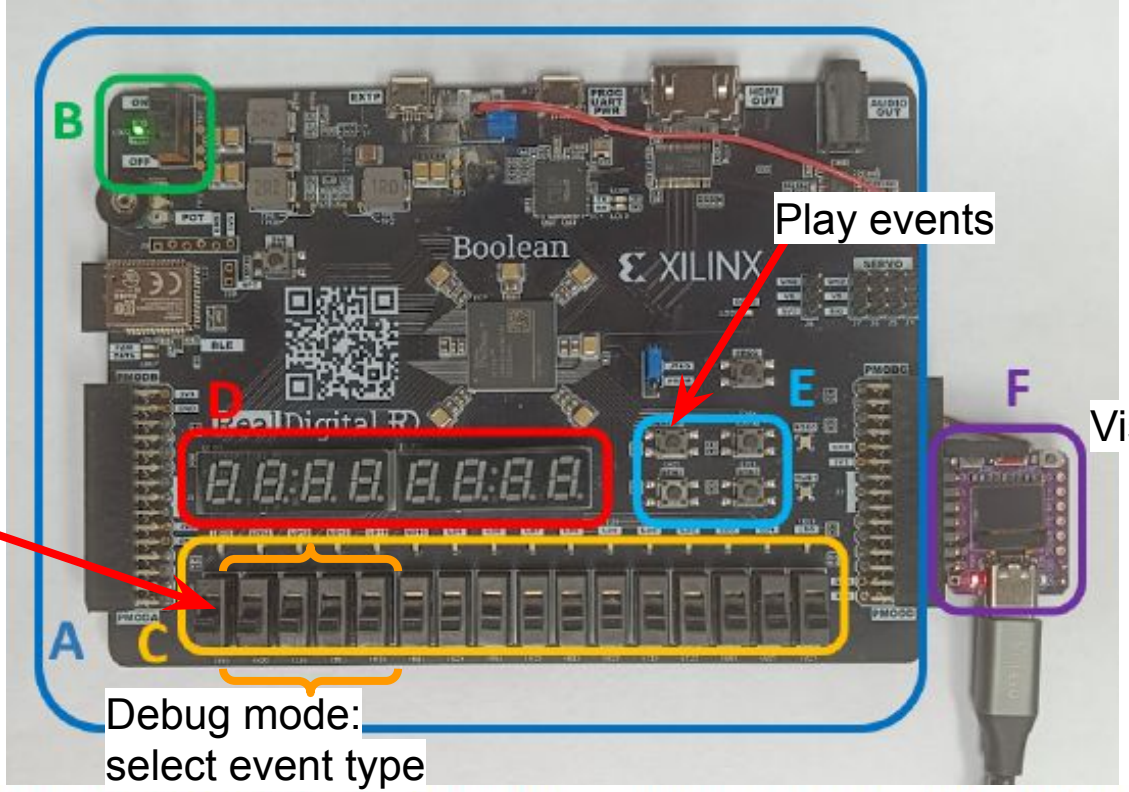


Figure 2: Hardware setup used in the trigger exercise. **Label A**: Boolean Board. **Label B**: power switch and status LED. **Label C**: switches and indicator LEDs used to control the operating mode. **Label D**: 7-segment displays for operating mode indication. **Label E**: action buttons used either to advance events in debug mode or to launch a complete data-taking sequence in run mode. **Label F**: ESP32 module with its OLED display.

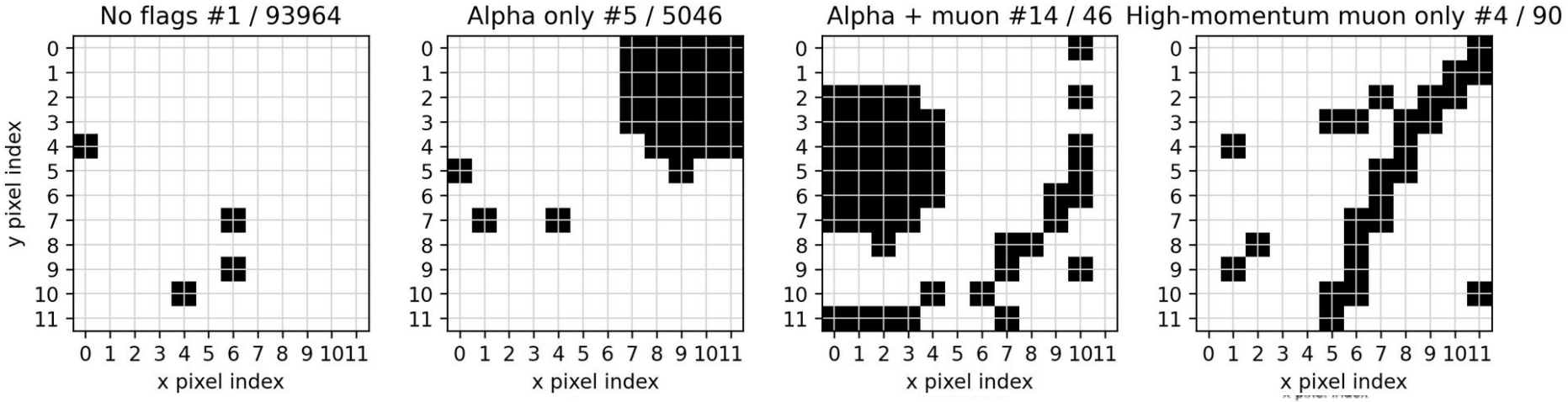


Figure 3: Representative event categories used in the notebook stage: background/noise, alpha-like activity, alpha+muon overlap, and a high-energy muon candidate.

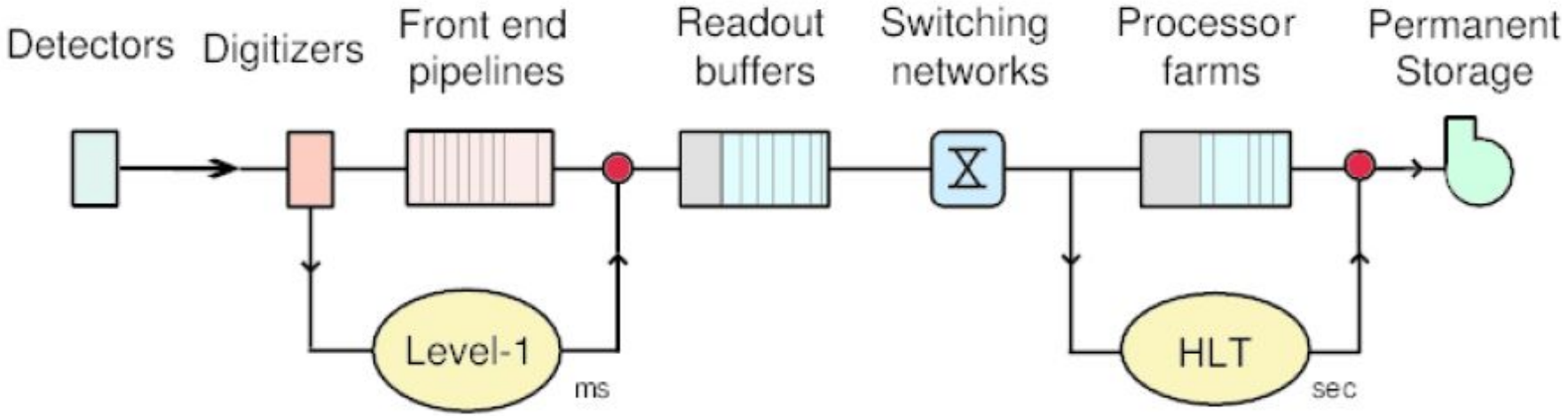

Detectors
Digitizers
Front end pipelines
Readout buffers
Switching networks
Processor farms
Permanent Storage
Level-1
ms
HLT
sec

Table 1: Representative trigger design values at the LHC (Run 3 and Upgrade eras).

Experiment	First stage	Second stage	Typical output target
CMS (Run 3)	Hardware L1, 3.8 μs, up to 100 kHz	CPU HLT with GPU acceleration for selected reconstruction tasks	1–1.5 kHz to permanent storage
CMS (Phase-2)	Track-trigger L1, 12.5 μs, 750 kHz design (about 1 MHz margin)	More selective HLT on a heterogeneous CPU/GPU farm	About 5–7.5 kHz
ATLAS (Run 3)	Hardware L1 trigger, about 2.5 μs, up to 100 kHz	Software Event Filter on a large CPU farm	About 1–2 kHz
ATLAS (Phase-II)	Hardware L0, about 1 MHz with about 10 μs latency; L1 track-trigger refinements studied	Software Event Filter; accelerator use under study	About 10 kHz
LHCb (Run 3)	Triggerless 30 MHz readout	GPU HLT1 (Allen) followed by CPU HLT2	HLT1 about 1–2 MHz to disk, final about 10 kHz
LHCb (Upgrade)	Triggerless O(30 MHz) readout at higher luminosity	Expanded GPU HLT1 plus CPU HLT2	Higher throughput than Run 3

LINK TO GOOGLECOLAB
https://colab.research.google.com/drive/1SFKwOMbxL8E6SvcEPiF17DNUkjyBKIDL#scrollTo=LQsEkfaKSsXt

REPO HLT
https://gitlab.cern.ch/cnid_trigger_practicum/student_materials