| ZUBoard 1CG |
|---|
| Avnet Engineering Services |
| www.avnet.me/ZUBoard-1CG |
| **Sheet Name** |
| 01 - Avnet Lead Sheet |
| 02 - Block Diagram |
| 03 - Bank 500, Bank 501, Bank 502, Bank 503 |
| 04 - Bank 504, Bank 505 |
| 05 - uSD, QSPI, Voltage Translation |
| 06 - USB 2.0, JTAG/UART MicroUSB |
| 07 - Gigabit Ethernet PHY |
| 08 - Bank 0, Bank 44, Bank 65, Bank 66 |
| 09 - Switches, LEDs, Push Buttons |
| 10 - Bank Power and Decoupling |
| 11 - LPDDR4 Device #1 |
| 12 - JTAG, UART Redacted |
| 13 - SYZYGY, Click Expansion |
| 14 - I2C & SPI Sensor, Power On Enable |
| 15 - USB-C Power In |
| 16 - Power Supplies |
| 17 - Back Page |

| REVISION | INITIALS | DATE | NOTES |
|---|---|---|---|
| 1 | JF | 07/27/22 | Initial Production Release Rev 1 |
| | | | |

AVNET
Reach Further

# ZUBoard 1CG

## AES-ZUB-1CG-DK-G

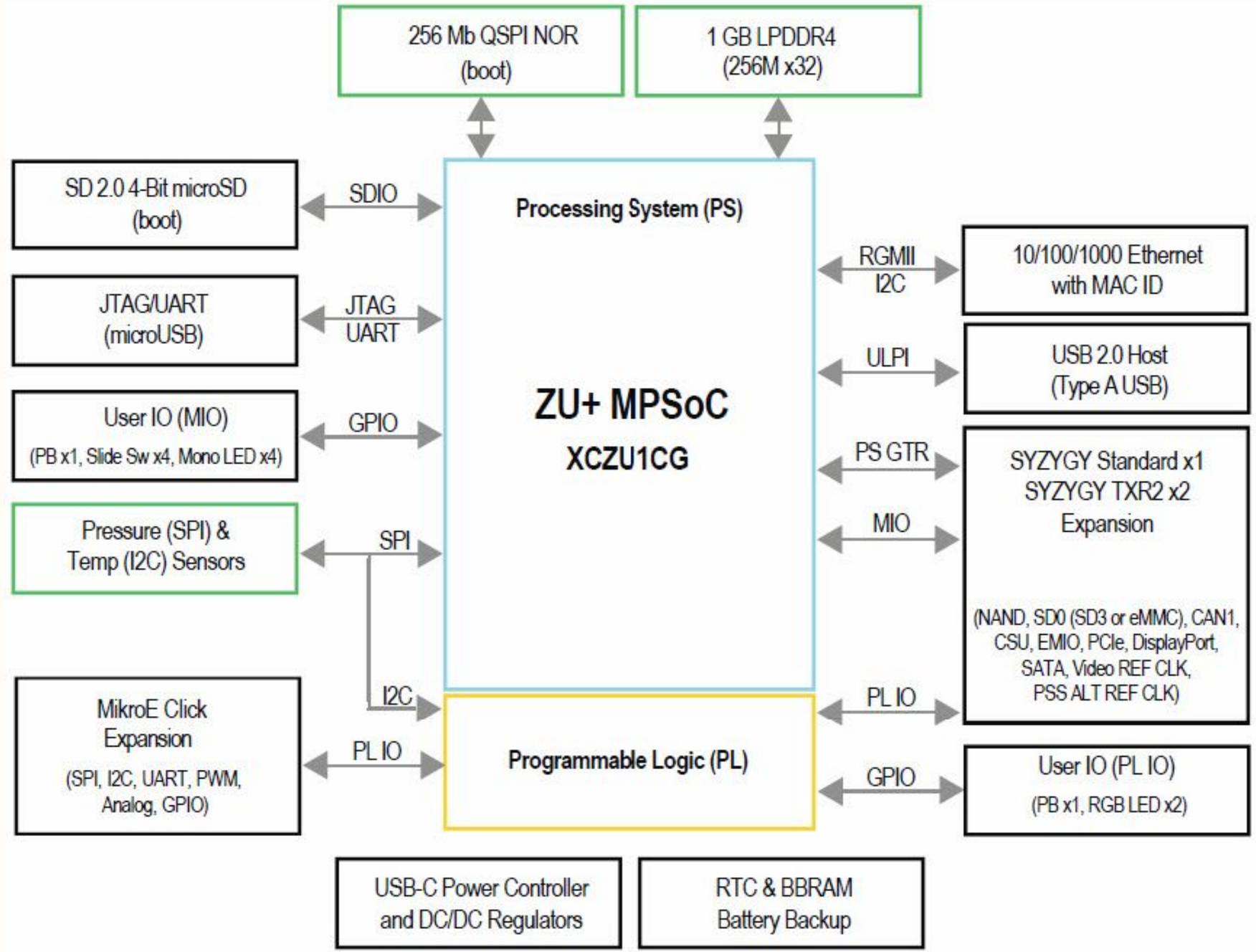
### Revision 1

| Variants |
|---|
| 02 - Production |



| AVNET Avnet Engineering Services | | | |
|---|---|---|---|
| Project Name: ZUBoard 1CG | PCB Rev: 1 | BOM: 02 | Variant: 02 |
| Doc Num: SCH-ZUB-1CG | Date: 05-Aug-22 | Time: 1:59:29 PM | |
| Sheet Title: 01 - Avnet Lead Sheet.SchDoc | Size: C | Sheet: 1 of 17 | |

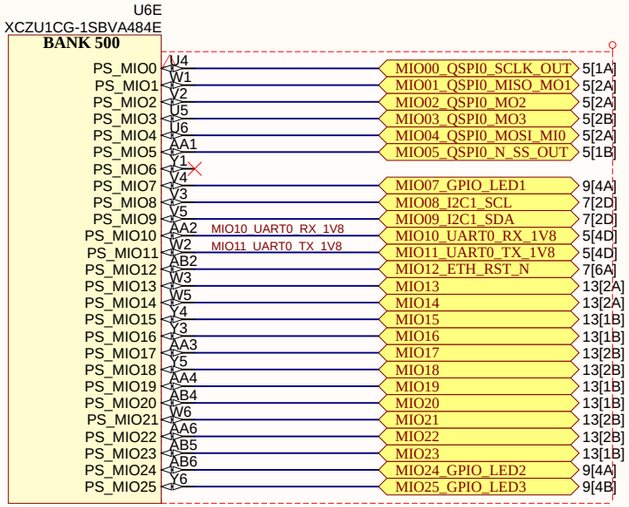
# Block Diagram



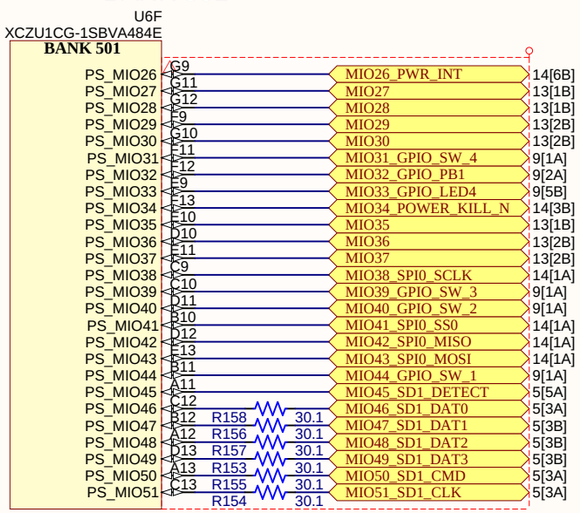

| | | | |
|---|---|---|---|
| AVNET Avnet Engineering Services | | | |
| Project Name: ZUBoard 1CG | PCB Rev: 1 | BOM: 02 | Variant: 02 |
| Doc Num: SCH-ZUB-1CG | Date: 05-Aug-22 | Time: 1:59:29 PM | |
| Sheet Title: 02 - Block Diagram.SchDoc | Size: C | Sheet: 2 of 17 | |

# BANK 500, BANK 501, BANK 502, BANK 503

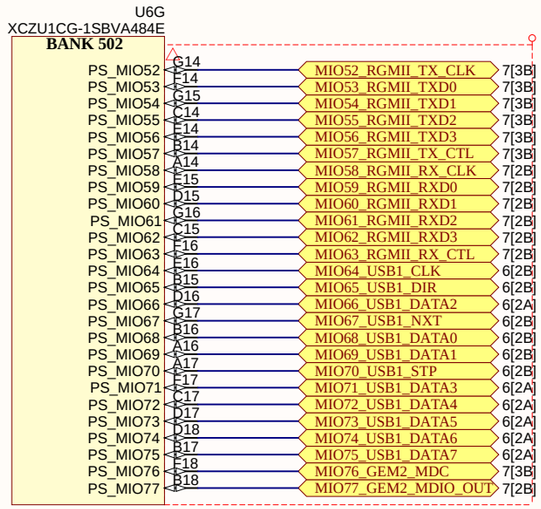
## BANK 500



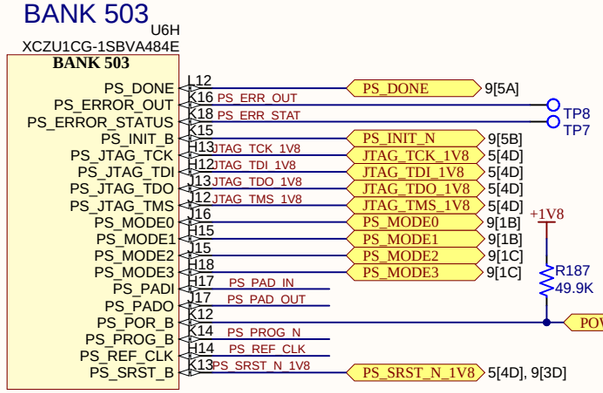

## BANK 501

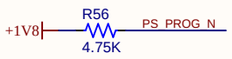


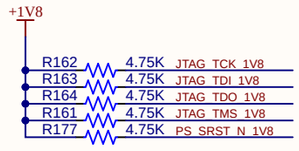

## BANK 502

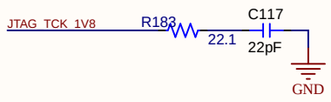



## BANK 503

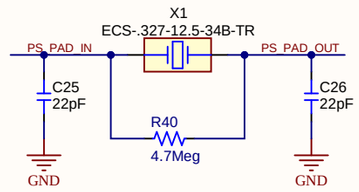


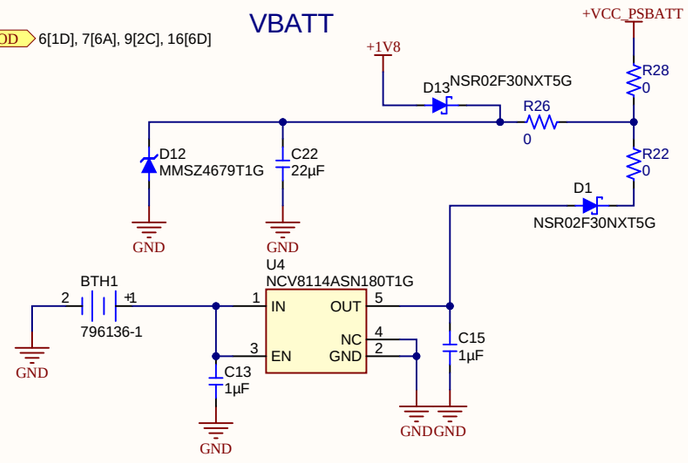



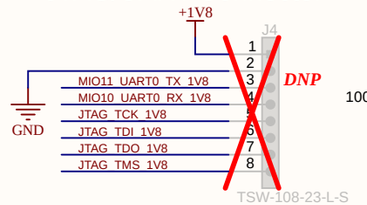

## 32KHz RTC XTAL



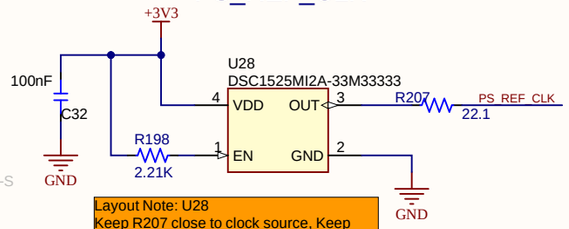

## VBATT




## JTAG/UART Connector




## PS_REF_CLK



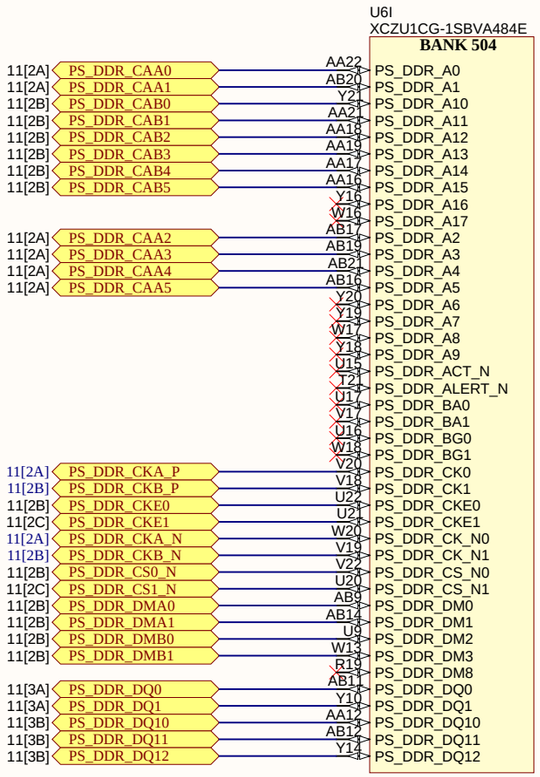

Layout Note: U28
Keep R207 close to clock source, Keep clock trace as short as possible to Pin H14

AVNET Avnet Engineering Services

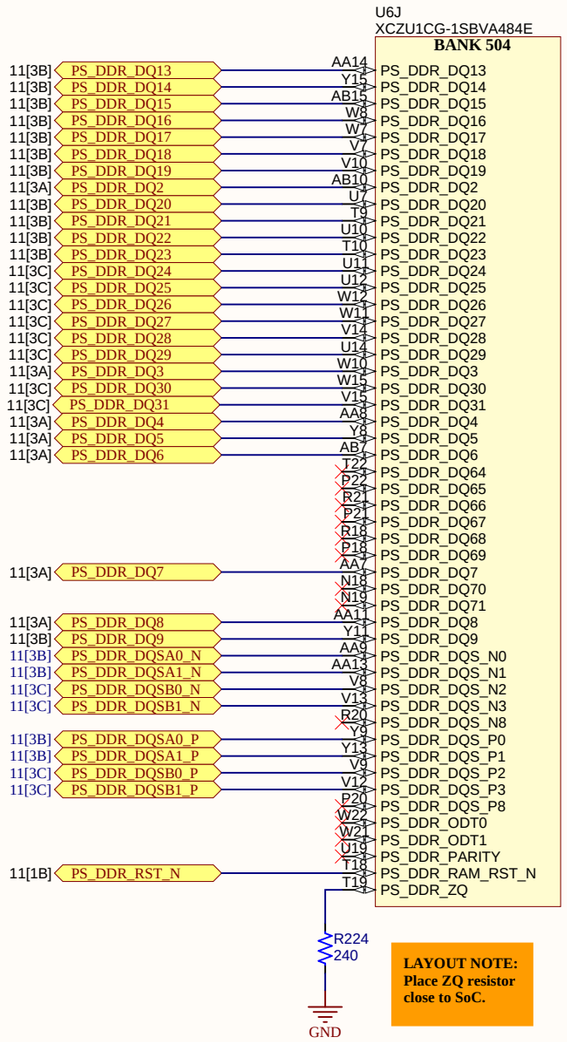
| | | | |
|---|---|---|---|
| Project Name: ZUBoard 1CG | PCB Rev: 1 | BOM: 02 | Variant: 02 |
| Doc Num: SCH-ZUB-1CG | Date: 05-Aug-22 | Time: 1:59:30 PM | |
| Sheet Title: 03 - Bank 500, Bank 501, Bank 502, Bank 503.SchDoc | Size: C | Sheet: 3 of 17 | |

# BANK 504, BANK 505

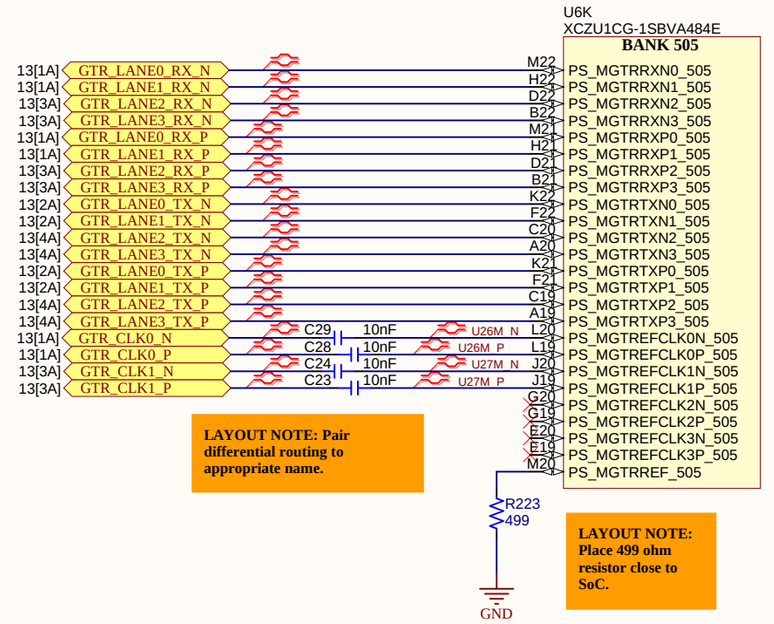
## BANK 504 - DDR




## BANK 504 - DDR




## BANK 505 - GTR

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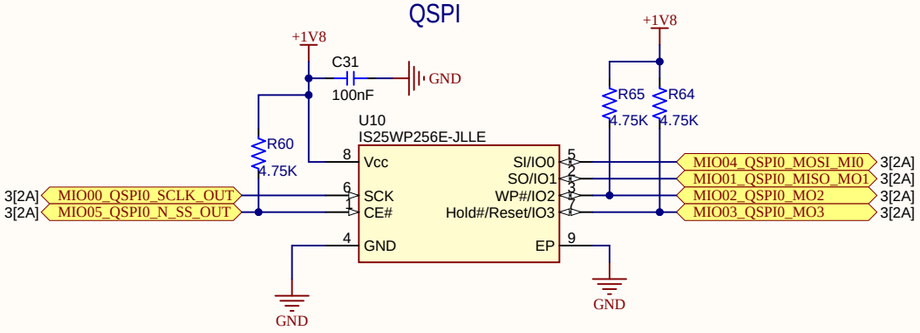
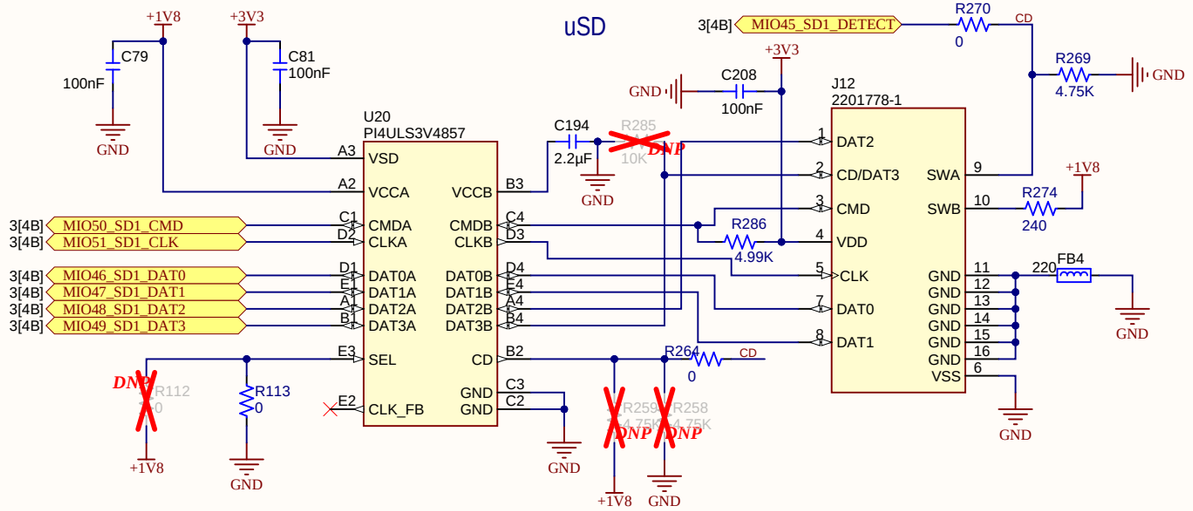
| | | | |
|---|---|---|---|
| Project Name: ZUBoard 1CG | PCB Rev: 1 | BOM: 02 | Variant: 02 |
| Doc Num: SCH-ZUB-1CG | Date: 05-Aug-22 | Time: 1:59:30 PM | |
| Sheet Title: 04 - Bank 504, BANK 505.SchDoc | Size: C | Sheet: 4 of 17 | |

# QSPI, uSD, and Voltage Translation

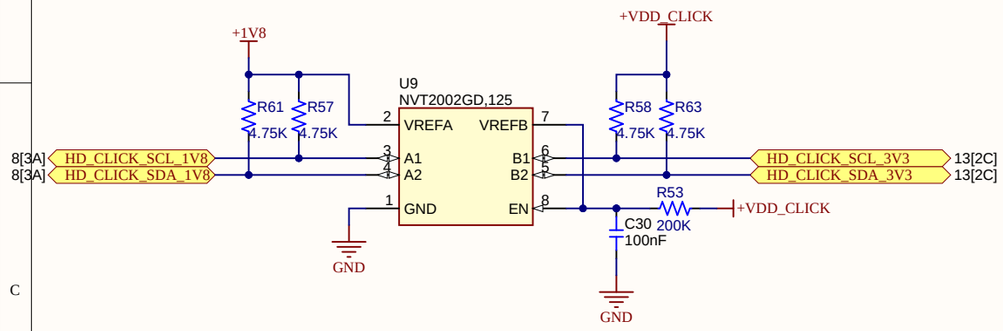
## QSPI



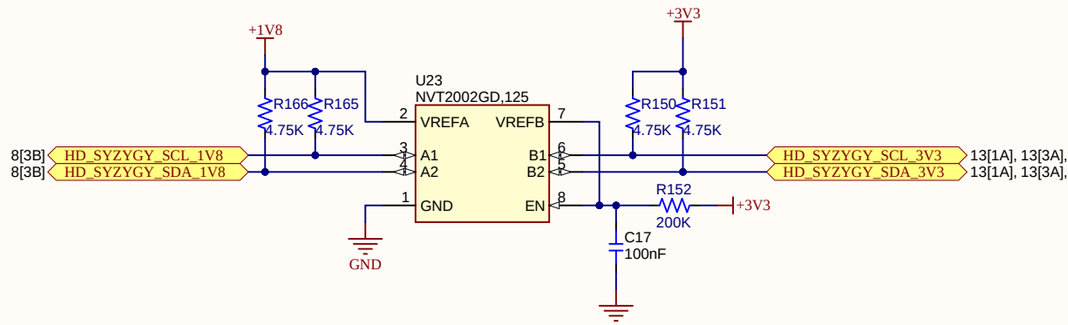

## uSD




## Click_I2C_I/O_Translation

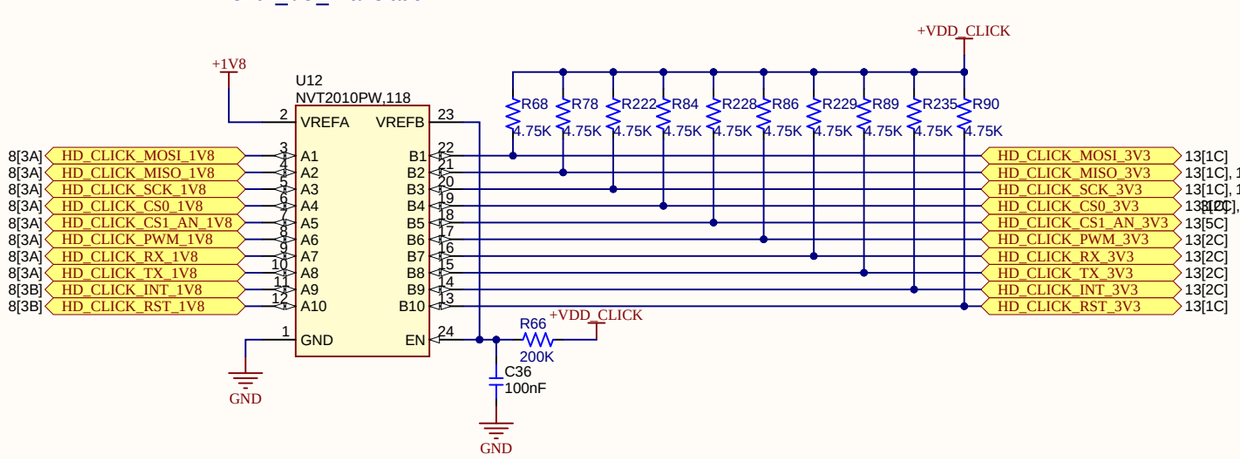


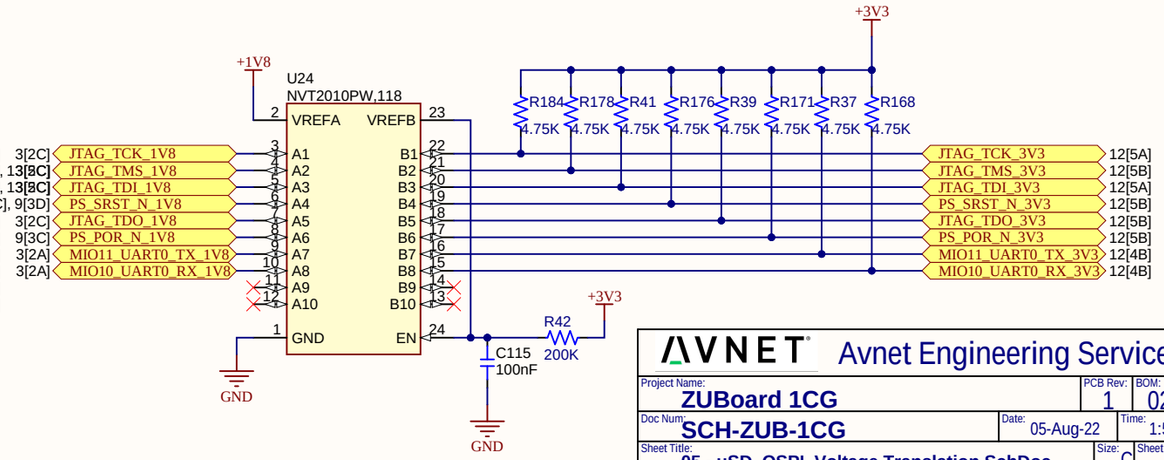

## SYZYGY_I2C_I/O_Translation




## JTAG_UART_I/O_Translation

## Click_I/O_Translation

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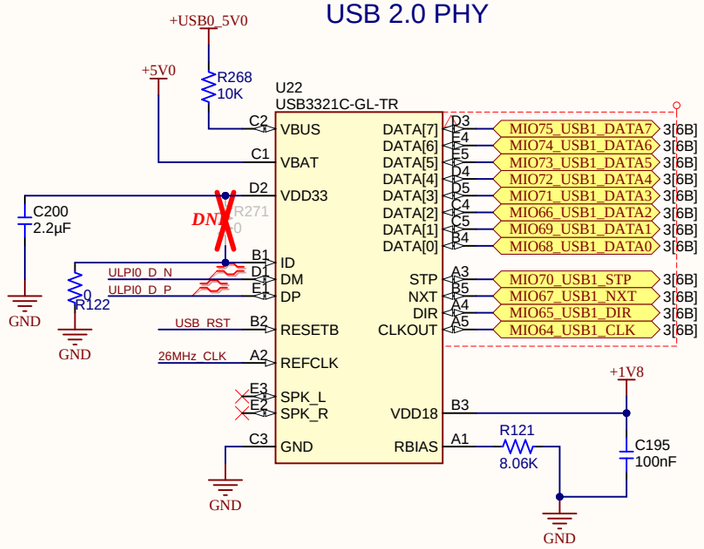
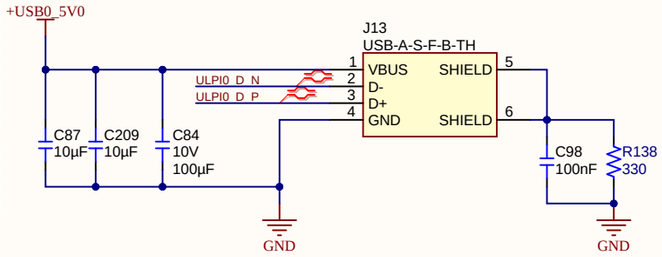
| | | | |
|---|---|---|---|
| Project Name: ZUBoard 1CG | PCB Rev: 1 | BOM: 02 | Variant: 02 |
| Doc Num: SCH-ZUB-1CG | Date: 05-Aug-22 | Time: 1:59:31 PM | |
| Sheet Title: 05 - uSD, QSPI, Voltage Translation.SchDoc | Size: C | Sheet: 5 of 17 | |

# USB 2.0, JTAG/UART MicroUSB

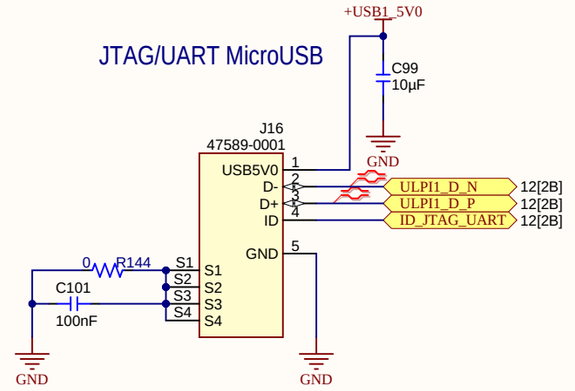
## USB 2.0 PHY



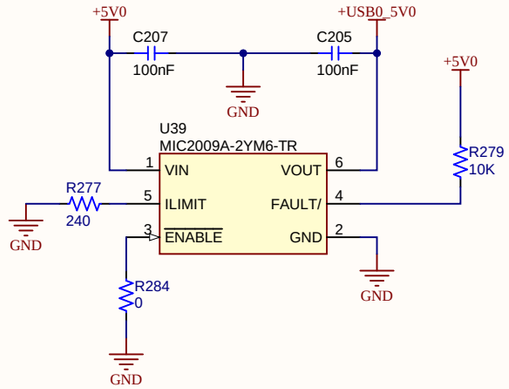

## USB 2.0 Type A Connector




## JTAG/UART MicroUSB

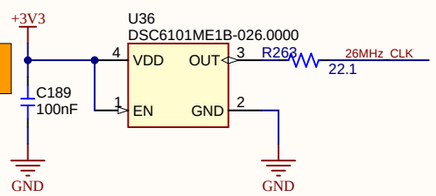



## Over Current Fault 900mA

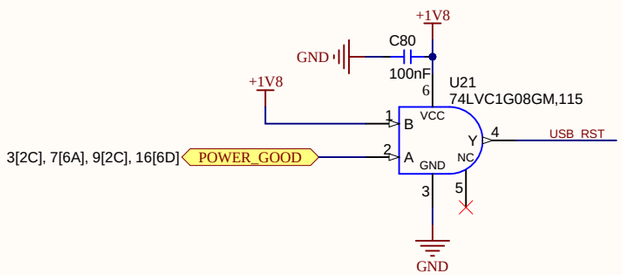



## 26MHz Clock

Layout Note: U36
Keep R263 close to clock source, Keep clock trace as short as possible to Pin A2




## USB 2.0 PHY Reset




| | | | |
|---|---|---|---|
| AVNET Avnet Engineering Services | | | |
| Project Name: ZUBoard 1CG | PCB Rev: 1 | BOM: 02 | Variant: 02 |
| Doc Num: SCH-ZUB-1CG | Date: 05-Aug-22 | Time: 1:59:31 PM | |
| Sheet Title: 06 - USB 2.0, JTAG & Uart MicroUSB.SchDoc | Size: C | Sheet: 6 of 17 | |

# Ethernet 10/100/1000

## PHY Decoupling

+AVDDL_1V2 — 220 FB1 — PWR — +DVDDL_1V2 — +1V8

C49 10µF, C57 100nF, C52 100nF, C50 100nF, C48 100nF, C45 100nF

Layout Note: U32
Place close to Pin14, Pin18, Pin23, Pin26, Pin39

C47 100nF, C51 100nF, C46 100nF

Layout Note: U32
Place close to Pin16, Pin34, Pin40

+3V3 — 220 FB2 — PWR — +AVDDH_3V3

C68 10µF, C58 100nF, C62 100nF, C63 100nF

Layout Note: U32
Place close to Pin1, Pin12, Pin47

+AVDDL_1V2

C66 10µF, C65 100nF, C64 100nF

Layout Note: U32
Place close to Pin4, Pin9

Layout Note: U18
Keep R249 close to clock source, Keep clock trace as short as possible to Pin 46

## U34 25MHz Clock

DSC1121DE2-025.0000T

+3V3 — R240 2.21K — 100nF C166

VDD, EN, GND, OUT, NC, NC — R249 22.1 — XI

Layout Note: U32
Pin 32, 31, 28, 27, 33, 35 to be length matched withing 20 mils and 50 Ohm

## Ethernet Reset

+1V8 — D25 SMMSD914T3G DNP — R232 10K DNP — ETH_RST_N — C162 10nF DNP — GND

+1V8 — C43 100nF — GND — D19 — R316 10K

U15 74LVC1G08GM,115 (VCC, B, Y, NC, GND, A)

C211 10µF — GND

MIO12_ETH_RST_N 3[2B]

POWER_GOOD 3[2C], 6[1D], 9[2C

## Ethernet PHY

U32
KSZ9131RNXC

| | | | |
|---|---|---|---|
| 3[6A] MIO59_RGMII_RXD0 | MIO59_RGMII_RXD0 | 32 | RXD0/MODE0 |
| 3[6A] MIO60_RGMII_RXD1 | MIO60_RGMII_RXD1 | 31 | RXD1/MODE1 |
| 3[6A] MIO61_RGMII_RXD2 | MIO61_RGMII_RXD2 | 28 | RXD2/MODE2 |
| 3[6B] MIO62_RGMII_RXD3 | MIO62_RGMII_RXD3 | 27 | RXD3/MODE3 |
| 3[6A] MIO58_RGMII_RX_CLK | MIO58_RGMII_RX_CLK | 35 | RXC/PHYAD2 |
| 3[6B] MIO63_RGMII_RX_CTL | MIO63_RGMII_RX_CTL | 33 | RX_CTL/CLK125_EN |
| | ETH_RST_N — R250 6.04K | 42 | RESET_N |
| | | 48 | ISET |
| 3[6A] MIO53_RGMII_TXD0 | | 19 | TXD0 |
| 3[6A] MIO54_RGMII_TXD1 | | 20 | TXD1 |
| 3[6A] MIO55_RGMII_TXD2 | | 21 | TXD2 |
| 3[6A] MIO56_RGMII_TXD3 | | 22 | TXD3 |
| 3[6A] MIO52_RGMII_TX_CLK | | 24 | TXC |
| 3[6A] MIO57_RGMII_TX_CTL | | 25 | TX_CTL |
| 3[6B] MIO76_GEM2_MDC | | 36 | MDC |
| 3[6B] MIO77_GEM2_MDIO_OUT | | 37 | MDIO |
| LED_ACT | | 17 | LED1/PME_N1/PHYAD0 |
| LED_LINK_1V8 | | 15 | LED2/PHYAD1 |

AVDDH 1, 12, NC 47 — +AVDDH_3V3

AVDDL 9, 4 — +AVDDL_1V2

AVDDL_PLL 44 — +AVDDL_1V2 — C53 10µF, C55 100nF, C56 10nF — GND

DVDDH 40, 34, 16 — +1V8

DVDDL 39, 30, 26, 23, 18, 14, NC — +DVDDL_1V2

LDO_O 43

XI 46 — XI — XO 45

| | |
|---|---|
| TXRXP_A 2 | TXRXA_P |
| TXRXM_A 3 | TXRXA_N |
| TXRXP_B 6 | TXRXB_P |
| TXRXM_B 7 | TXRXB_N |
| TXRXP_C 8 | TXRXC_P |
| TXRXM_C 9 | TXRXC_N |
| TXRXP_D 10 | TXRXD_P |
| TXRXM_D 11 | TXRXD_N |

INT_N/PME_N2/ALLPHYAD 38 — R75 4.75K — +1V8

CLK125_NDO/LED_MODE 41 — CLK_125M

NC 13, VSS 29, P_VSS 49 — GND

## AVDDL_1V2 LDO

U35
NCV8114ASN120T1G (IN, OUT, NC, EN, GND)

+3V3 — C175 1µF — GND

R253 10K — C182 100nF — GND

+AVDDL_1V2 — PWR — C176 1µF — GND

## Strapping Options:

MODE: (D3,D2,D1,D0)
1110
RGMII MODE
10/100/1000M
1000M Full Duplex
100M/10M Half/Full Duplex

PHY Addess:
(AD4, AD3), AD2, AD1, AD0
(00)111

LED_MODE
LED MODE=1 & Pull Up -> Single-LED Mode
LED MODE=0 & Pull Down -> Tri-color LED Mode
LED MODE=0 & strap is unsed -> Enhanced LED Mode

+1V8 — R69 10K — MIO62_RGMII_RXD3 — R70 1K DNP — GND

+1V8 — R216 10K — MIO61_RGMII_RXD2 — R217 1K DNP — GND

+1V8 — R71 10K — MIO60_RGMII_RXD1 — R76 1K DNP — GND

+1V8 — R72 10K DNP — MIO59_RGMII_RXD0 — R73 1K — GND

+1V8 — R218 10K — MIO58_RGMII_RX_CLK — R219 1K DNP — GND

+1V8 — R247 10K — LED_ACT — R246 1K DNP — GND

+1V8 — R94 10K — LED_LINK_1V8 — R93 1K DNP — GND

+1V8 — R243 10K DNP — CLK_125M — R236 1K — GND

+1V8 — R215 10K DNP — MIO63_RGMII_RX_CTL — R220 1K — GND

MIO63_RGMII_RX_CTL:
Pull Up : Enable 125MHz Clk
Pull Down : Disable 125 MHz Clk

+1V8 — R1 1K — MIO77_GEM2_MDIO_OUT

Layout Note: U32
Pin 19, 20, 21, 22, 24, 25 to be length matched withing 20 mils and 50 Ohm impedance

## PHY LED OR

+1V8 — R230 0 DNP — C79 100nF DNP — GND

U31 74LVC1G32GV,125 (A, B, Y)

LED_ACT — R231 0 DNP — LED_LINK_1V8 — R225 0 DNP

LED_ACT — R83 0 — LED_Y_1V8 — R77 0 DNP

## MAC EEPROM

EEPROM 7 bit device address = 1010000 (0x50)
EUI 7 bit device address = 1011000 (0x58)

U7
AT24MAC402 (A0, A1, A2, GND, VCC, WP, SCL, SDA)

+1V8 — C27 100nF — GND

R49 4.75K, R54 4.75K

WP

MIO08_I2C1_SCL 3[2A]
MIO09_I2C1_SDA 3[2A]

## MAC EEPROM Addressing

+1V8 — R194 4.75K DNP — A2 — R52 0 — GND

+1V8 — R188 4.75K DNP — A1 — R48 0 — GND

+1V8 — R186 4.75K DNP — A0 — R44 0 — GND

+1V8 — R45 4.75K DNP — WP — R43 0 — GND

## LED 1V8 To 3V3 Translation

+3V3 — R127 1K — LED_LINK_1V8 — Q8 SSM3K7002CFU — LED_LINK_3V3 — Q9 SSM3K7002CFU — GND

+3V3 — R88 1K — LED_Y_1V8 — Q4 SSM3K7002CFU — LED_Y_3V3 — Q5 SSM3K7002CFU — GND

## RJ-45

J11
ARJM11C7-502-KB-EW2

LED_LINK_3V3 — R140 240 — P12 — +3V3

TXRXA_P P1, TXRXA_N P2 — TXRXB_P P3, TXRXB_N P4 — C78 100nF P5, C77 100nF P6 — TXRXC_P P7, TXRXC_N P8 — TXRXD_P P9, TXRXD_N P10

LED_Y_3V3 — R139 240 — P14

R132 0 — C91 100nF — GND

SHIELD

RJ-45 (TD1+, TD1-, TD2+, TD2-, CT, CT, TD3+, TD3-, TD4+, TD4-, D1, D0, D3, D2)

J1 TX1+, J2 TX1-, J3 TX2+, J6 TX2-, J4 TX3+, J5 TX3-, J7 TX4+, J8 TX4-

P11, P13

| | | | |
|---|---|---|---|
| Project Name: | ZUBoard 1CG | PCB Rev: 1 | BOM: 02 / Variant: 02 |
| Doc Num: | SCH-ZUB-1CG | Date: 05-Aug-22 | Time: 1:59:32 PM |
| Sheet Title: | 07 - Gigabit Ethernet PHY.SchDoc | Size: C | Sheet: 7 of 17 |

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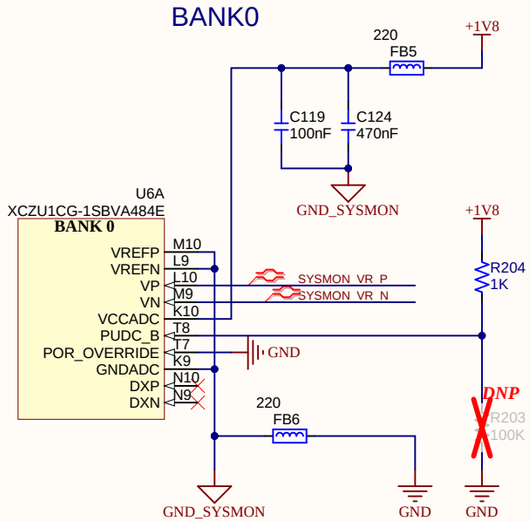
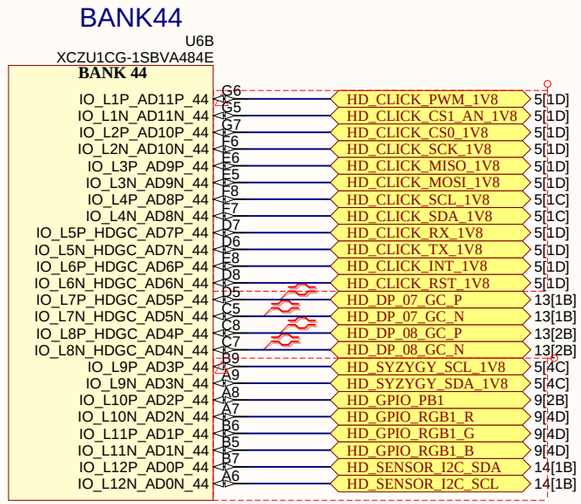
# BANK0, BANK44, BANK65, BANK66

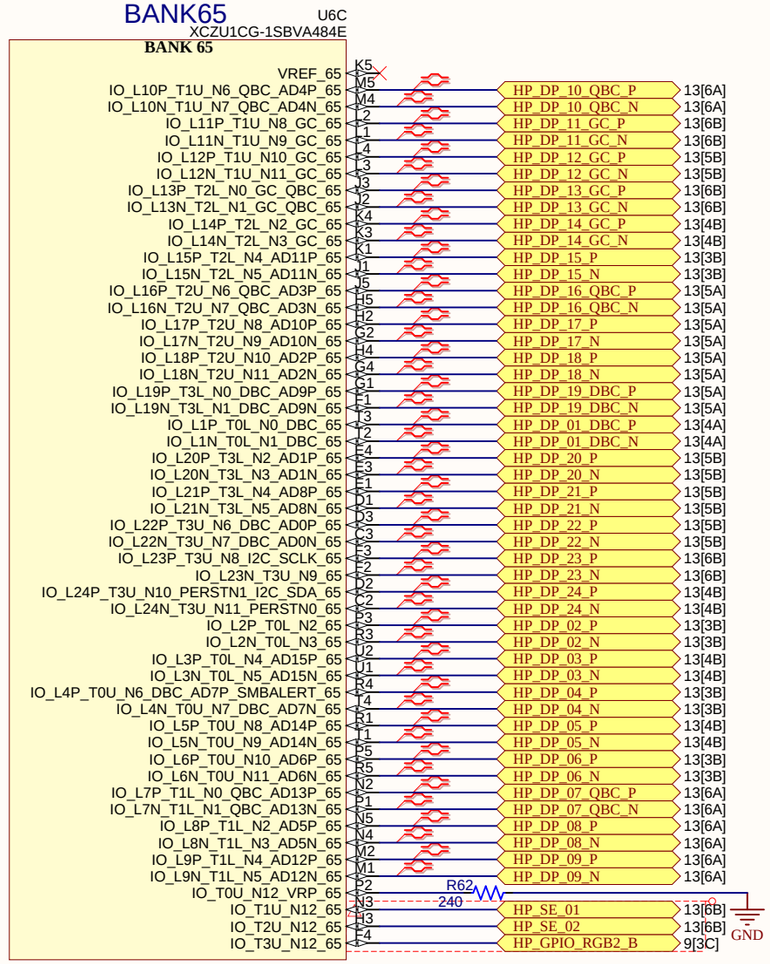
## BANK0



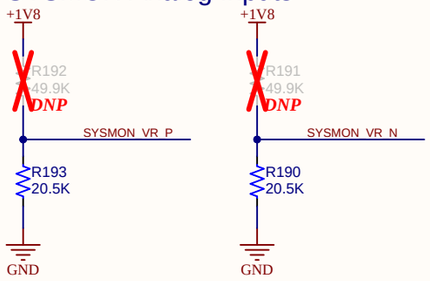

## BANK44



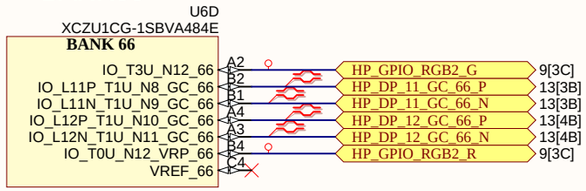

## BANK65




## SYSMON Analog Inputs




## BANK66





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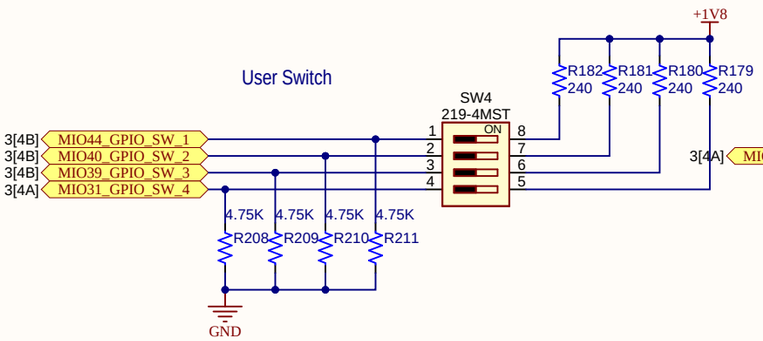
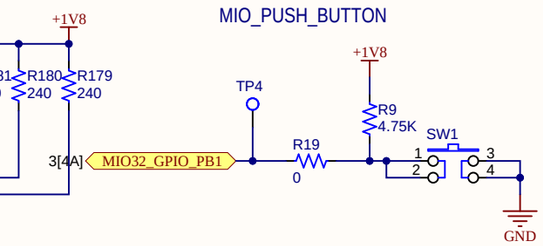
| Project Name: ZUBoard 1CG | PCB Rev: 1 | BOM: 02 | Variant: 02 |
| Doc Num: SCH-ZUB-1CG | Date: 05-Aug-22 | Time: 1:59:33 PM | |
| Sheet Title: 08 - Bank 0, Bank 44, Bank65, Bank66.SchDoc | Size: C | Sheet: 8 of 17 | |

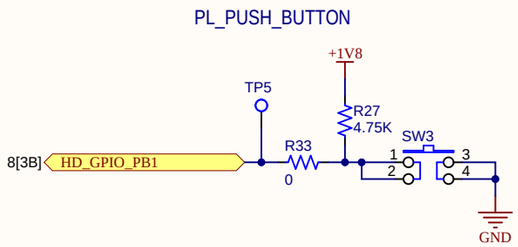
# SWITCHES, LEDs, Push Buttons

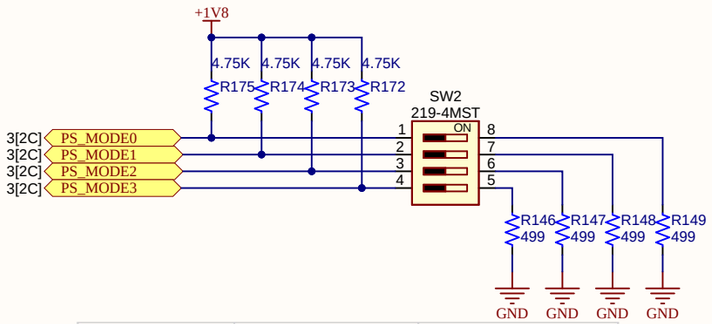
## Switches




## Push Buttons

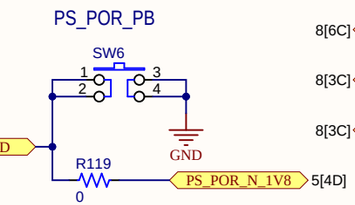


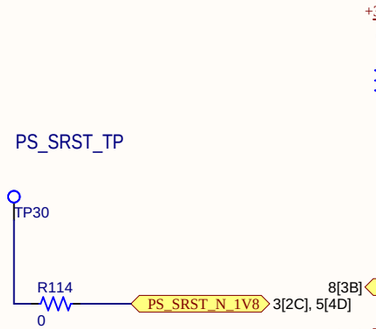



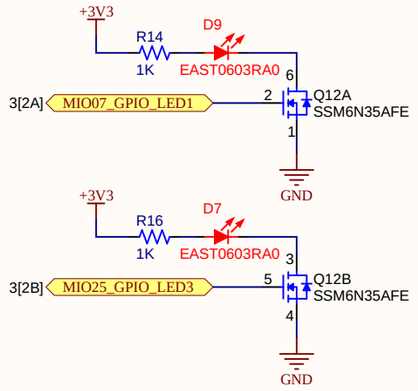

| BOOT MODE | MODE PIN [3:0] | SW2 [1-4] |
|---|---|---|
| JTAG | 0x0 | ON-ON-ON-ON |
| QSPI32 | 0x2 | ON-OFF-ON-ON |
| SD1 (2.0) | 0x5 | OFF-ON-OFF-ON |
| eMMC (1.8V) | 0x6 | ON-OFF-OFF-ON |

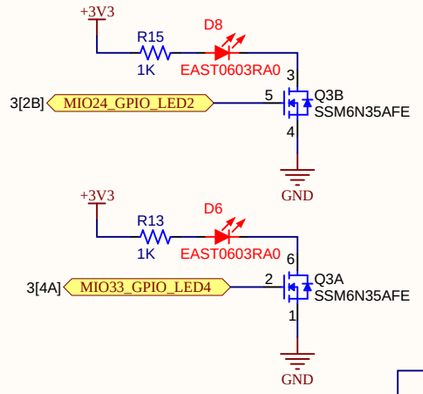
NOTE:
eMMC Boot is only suppored through SYZYGY Expansion POD

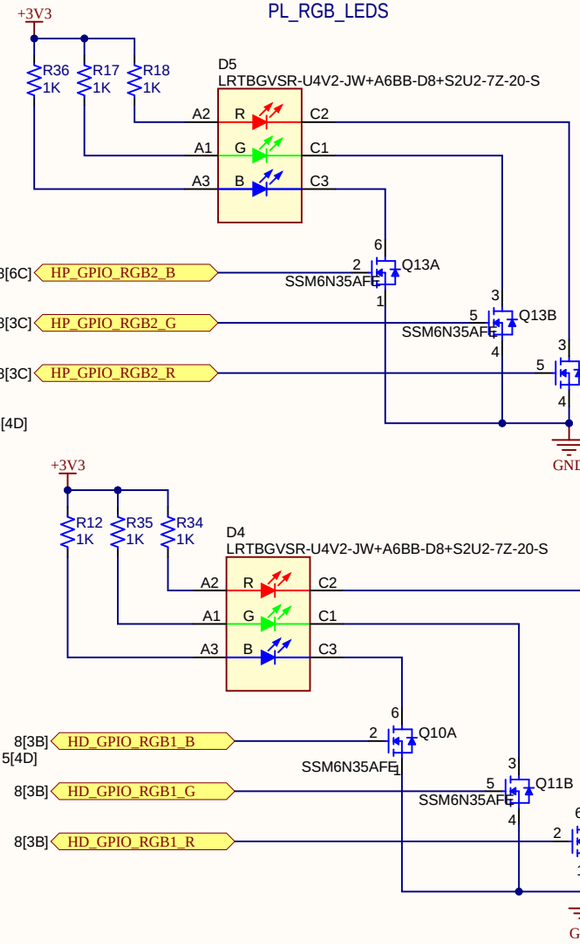



## User LEDs



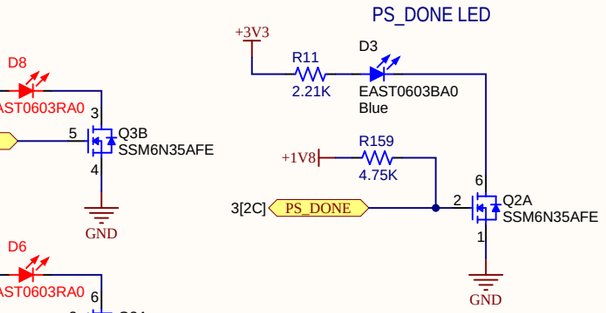



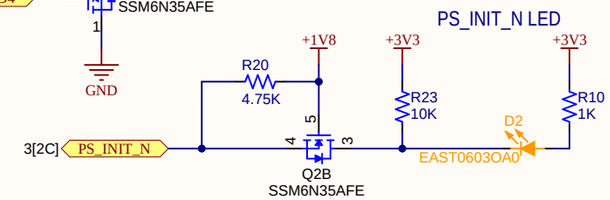





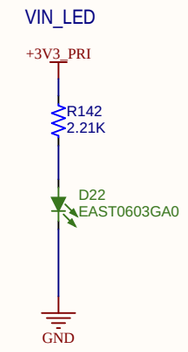


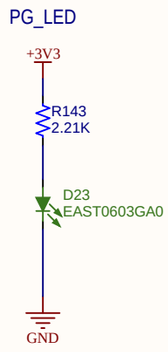
## LED INDICATORS:




INIT_N = 0, LED ON
INIT_N = 1, LED OFF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| | | | |
|---|---|---|---|
| Project Name: ZUBoard 1CG | PCB Rev: 1 | BOM: 02 | Variant: 02 |
| Doc Num: SCH-ZUB-1CG | Date: 05-Aug-22 | Time: 1:59:33 PM | |
| Sheet Title: 09 - Switches, LEDs, Push Buttons.SchDoc | Size: C | Sheet: 9 of 17 | |

# BANK POWER & DECOUPLING

U6L
XCZU1CG-1SBVA484E
**PL CORE POWER**

| | | |
|---|---|---|
| VCCAUX | M6 | +1V8 |
| VCCAUX | P6 | |
| VCCAUX_IO | J6 | |
| VCCAUX_IO | K6 | |
| VCCAUX_IO | L6 | |
| VCCBRAM | N7 | +0V85 |
| VCCBRAM | R6 | |
| VCCBRAM | R7 | |
| VCCBRAM | T6 | |
| VCCINT | H10 | |
| VCCINT | H8 | |
| VCCINT | J11 | |
| VCCINT | J9 | |
| VCCINT | K8 | |
| VCCINT | L11 | |
| VCCINT | M8 | |
| VCCINT | N11 | |
| VCCINT | P10 | |
| VCCINT | P8 | |
| VCCINT | R11 | |
| VCCINT | R9 | |
| VCCINT_IO | H7 | |
| VCCINT_IO | J7 | |
| VCCINT_IO | L7 | |
| VCCINT_IO | M7 | |

+0V85: C141 470nF, C129 470nF → GND

+1V8: C102 4.7µF, C123 470nF, C112 470nF → GND

+1V8: C159 470nF, C121 470nF, C133 470nF, C108 470nF, C122 470nF, C103 470nF, C106 1nF → GND

+0V85: C143 470nF, C137 470nF → GND

+0V85: C113 4.7µF, C145 470nF, C132 470nF → GND

+1V1: C148 10µF, C153 4.7µF, C131 470nF, C144 47nF, C142 1nF, C154 1nF, C146 1nF → GND

+1V8: C104 4.7µF, C109 470nF, C107 100nF → GND

+0V85: C136 4.7µF, C120 470nF, C114 100nF → GND

+VCCO_HP: C1 4.7µF, C2 470nF, C3 100nF → GND

U6M
XCZU1CG-1SBVA484E
**VCCO**

| | | | |
|---|---|---|---|
| +1V8 | AA5 | VCCO_PSIO0_500 | VCCO_44 B8 +1V8 |
| | V6 | VCCO_PSIO0_500 | VCCO_44 E7 |
| | C11 | VCCO_PSIO1_501 | VCCO_65 B3 |
| | F10 | VCCO_PSIO1_501 | VCCO_65 G3 +VCCO_HP |
| | C16 | VCCO_PSIO2_502 | VCCO_65 K2 |
| | D14 | VCCO_PSIO2_502 | VCCO_65 P4 |
| | G13 | VCCO_PSIO3_503 | |
| +1V1 | H16 | VCCO_PSIO3_503 | |
| | AB18 | VCCO_PSDDR_504 | |
| | P19 | VCCO_PSDDR_504 | |
| | T20 | VCCO_PSDDR_504 | |
| | V16 | VCCO_PSDDR_504 | |
| | V21 | VCCO_PSDDR_504 | |
| | Y17 | VCCO_PSDDR_504 | |
| | Y22 | VCCO_PSDDR_504 | |

C157 10nF, C161 10nF, C150 10nF → GND

NOTE: Bank 66 HP I/Os are attached to VCCO 65 internally.

Layout Note: Place direct pin connect CAPs under Zynq.

U6N
XCZU1CG-1SBVA484E
**PS CORE POWER**

| | | |
|---|---|---|
| PS_MGTRAVCC | F19 | +0V85 |
| PS_MGTRAVCC | H19 | |
| PS_MGTRAVCC | K19 | |
| PS_MGTRAVTT | A21 | +1V8 |
| PS_MGTRAVTT | B19 | |
| PS_MGTRAVTT | D19 | |
| VCC_PSADC | P15 | |
| VCC_PSAUX | L16 | +1V8 |
| VCC_PSAUX | L17 | |
| VCC_PSAUX | M16 | |
| VCC_PSAUX | M17 | |
| VCC_PSAUX | N15 | |
| VCC_PSBATT | M14 | +VCC_PSBATT |
| VCC_PSDDR_PLL | M15 | |
| VCC_PSDDR_PLL | N14 | +0V85 |
| VCC_PSINTFP | R15 | |
| VCC_PSINTFP | R16 | |
| VCC_PSINTFP | T12 | |
| VCC_PSINTFP | T13 | |
| VCC_PSINTFP | T14 | |
| VCC_PSINTFP | T16 | |
| VCC_PSINTFP | N17 | |
| VCC_PSINTFP_DDR | P17 | |
| VCC_PSINTFP_DDR | T17 | |
| VCC_PSINTFP_DDR | N12 | |
| VCC_PSINTLP | N13 | +0V85 |
| VCC_PSINTLP | P12 | |
| VCC_PSINTLP | P13 | |
| VCC_PSINTLP | R13 | |
| VCC_PSINTLP | R14 | |
| VCC_PSINTLP | L13 | |
| VCC_PSPLL | L14 | +1V2 |
| VCC_PSPLL | M12 | |
| VCC_PSPLL | | |

+1V8 → 220 FB7 → +1V8

R195 0 DNP: +1V8 → +VCC_PSBATT

C138 470nF, C139 100nF → GND_SYSMON

C128 10µF → GND

GND_SYSMON

XCZU1CG-1SBVA484E
U6O
**DIGITAL GND**

| | | | |
|---|---|---|---|
| A1 | GND | GND | P7 |
| A10 | GND | GND | P14 |
| A15 | GND | GND | P11 |
| A18 | GND | GND | N8 |
| A22 | GND | GND | N6 |
| A5 | GND | GND | N22 |
| AA10 | GND | GND | N21 |
| AA15 | GND | GND | N20 |
| AA20 | GND | GND | N16 |
| AB1 | GND | GND | N1 |
| AB13 | GND | GND | M3 |
| AB22 | GND | GND | M19 |
| AB3 | GND | GND | M18 |
| AB8 | GND | GND | M13 |
| B13 | GND | GND | M11 |
| B20 | GND | GND | L8 |
| C1 | GND | GND | L5 |
| C18 | GND | GND | L22 |
| C21 | GND | GND | L21 |
| C22 | GND | GND | L18 |
| C6 | GND | GND | L15 |
| D20 | GND | GND | K7 |
| D4 | GND | GND | K20 |
| D9 | GND | GND | K17 |
| E12 | GND | | |

GND_SYSMON: Y7 Y2 Y14 W9 W4 W10 W1 V11 V1 U8 U3 U15 P16 U13 T5 T15 T11 R8 R22 R2 R17 R11 R14 P9 GND_PSADC

GND: E17 E18 E2 E21 E22 E15 E20 F5 G18 G21 G22 G8 H1 H11 H20 H6 H9 J10 J14 J18 J21 J22 J4 J8 K11

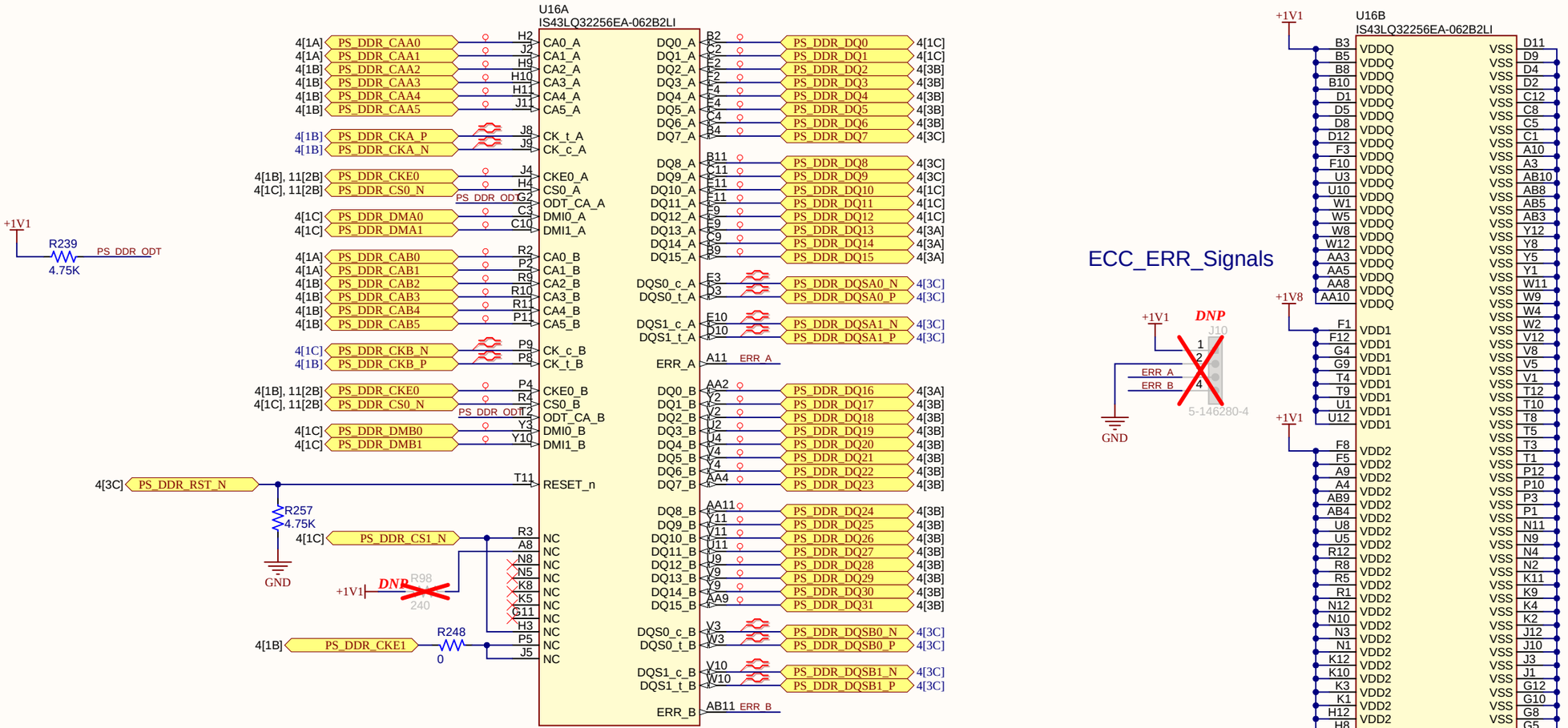
GND

| | | | |
|---|---|---|---|
| AVNET | Avnet Engineering Services | | |
| Project Name: ZUBoard 1CG | | PCB Rev: 1 | BOM: 02 / Variant: 02 |
| Doc Num: SCH-ZUB-1CG | Date: 05-Aug-22 | Time: 1:59:34 PM | |
| Sheet Title: 10 - Bank Power and Decoupling.SchDoc | Size: C | Sheet: 10 of 17 | |

# LPDDR4 8Gb (1GB) RAM

## POINT-TO-POINT: NO DDR TERM RESISTORS

## 40 OHM INTERFACE IMPEDANCE







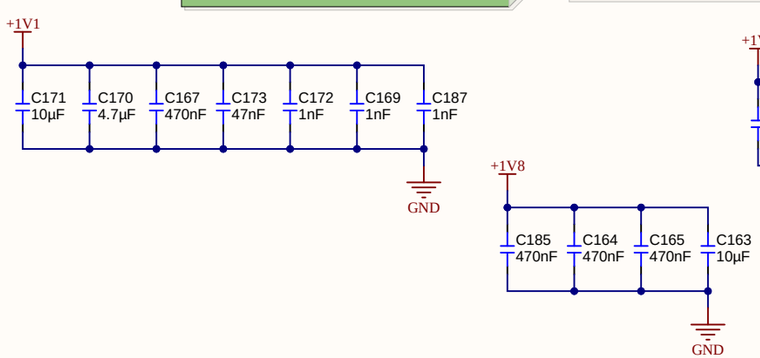



PS_DDR_CS and CKE signals connected to maintain backwards DDR compatibility.

LAYOUT NOTEs: 1) 40 Ohm Interface impedance. 2) Place DDR within 1 inch of Zynq device. 3) Place decoupling capacitors as close as possible to DDR device.

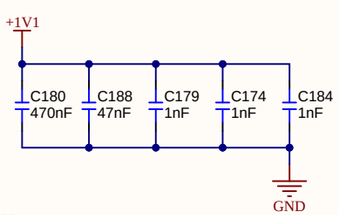
Note:
Compatible with ISSI LPDDR4 16Gb, 2GB RAM

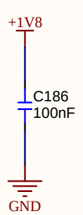
LAYOUT NOTE: Place ZQ resistor close to DDR IC.







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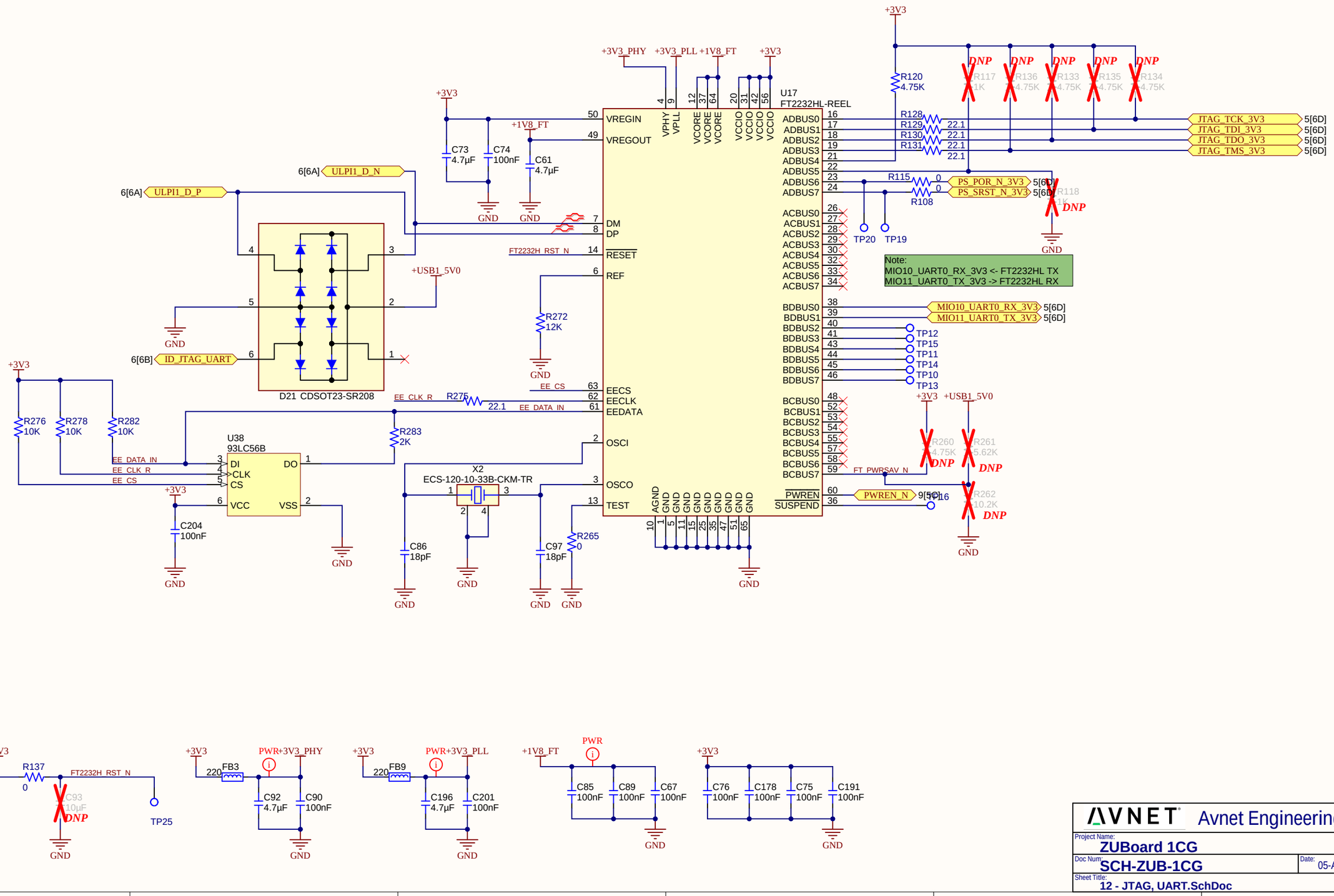
|---|---|---|---|
| Project Name: ZUBoard 1CG | PCB Rev: 1 | BOM: 02 | Variant: 02 |
| Doc Num: SCH-ZUB-1CG | Date: 05-Aug-22 | Time: 1:59:35 PM | |
| Sheet Title: 11 - LPDDR4 Device #1.SchDoc | Size: C | Sheet: 11 of 17 | |

# JTAG & UART





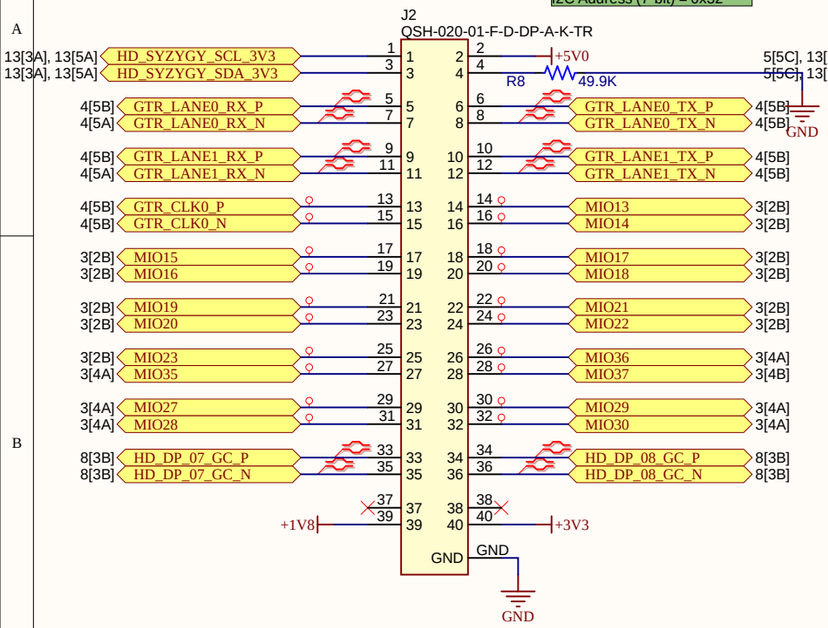


| | | | |
|---|---|---|---|
| AVNET Avnet Engineering Services | | | |
| Project Name: ZUBoard 1CG | PCB Rev: 1 | BOM: 02 | Variant: 02 |
| Doc Num: SCH-ZUB-1CG | Date: 05-Aug-22 | Time: 1:59:35 PM | |
| Sheet Title: 12 - JTAG, UART.SchDoc | Size: C | Sheet: 12 of 17 | |

# SYZYGY/Click Expansion

## SYZYGY TXR-2 MIO

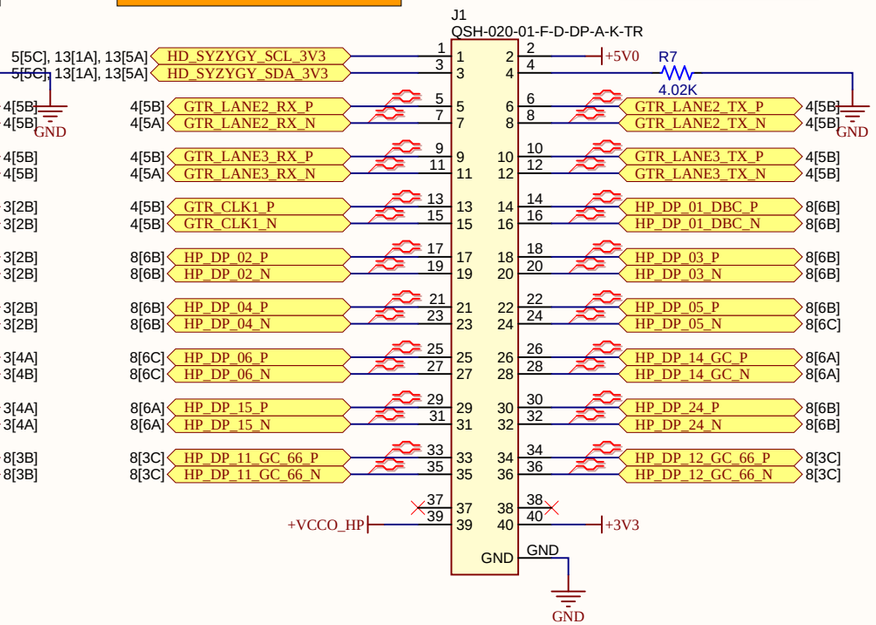
RGA Resistor = 49.9k Ohm
Nominal RGA Voltag - 2.740V
I2C Address (7-bit) = 0x32




## SYZYGY TXR-2 PL

Layout Note: J1 & J2
Place J1 & J2 into double wide POD layout with POD hanging off PCB

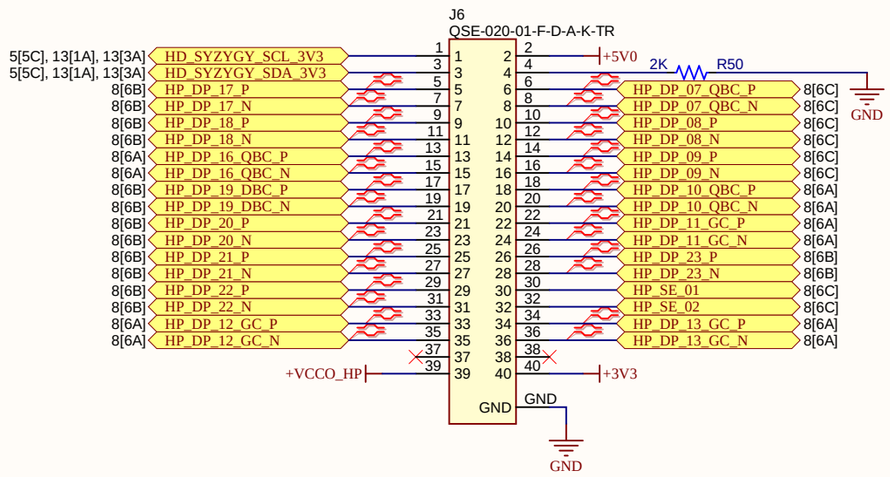
RGA Resistor = 4.02k Ohm
Nominal RGA Voltag - 0.933V
I2C Address (7-bit) = 0x3B



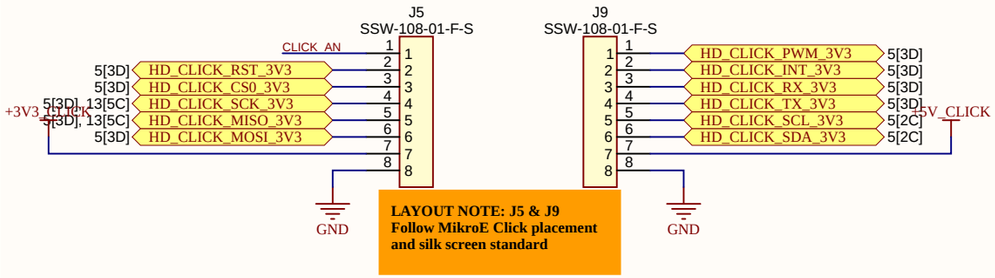

## SYZYGY Standard

Layout Note: J6
Place J6 with POD hanging off PCB

RGA Resistor = 2k Ohm
Nominal RGA Voltag - 0.541V
I2C Address (7-bit) = 0x3D

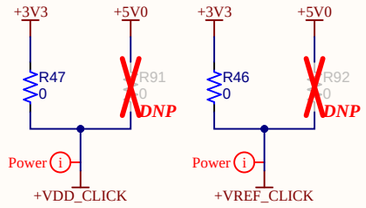



## MikroE Click Site



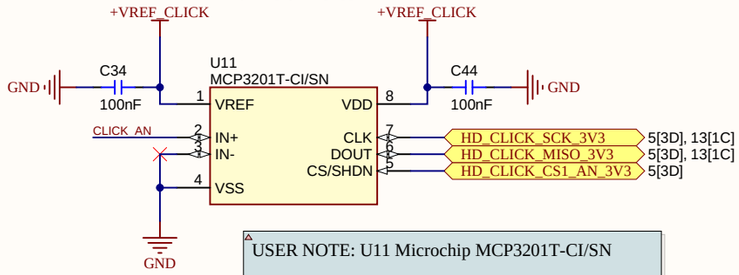

**LAYOUT NOTE: J5 & J9**
**Follow MikroE Click placement and silk screen standard**

## MIkroE Click I/O Level




**LAYOUT NOTE: R47,R91,R46,R92**
**Place resistors in an easy to rework location**

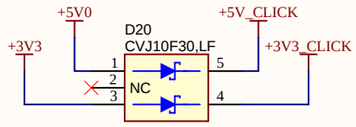
## A/D Converter




USER NOTE: U11 Microchip MCP3201T-CI/SN

Device SPI SCK signal is limited to be < 1MHz in order for it to work as expected

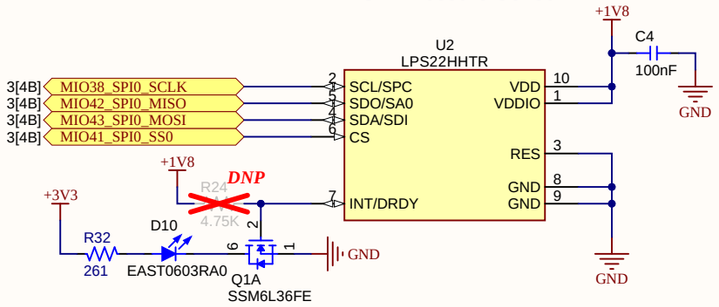
## Click Site Voltage Protection



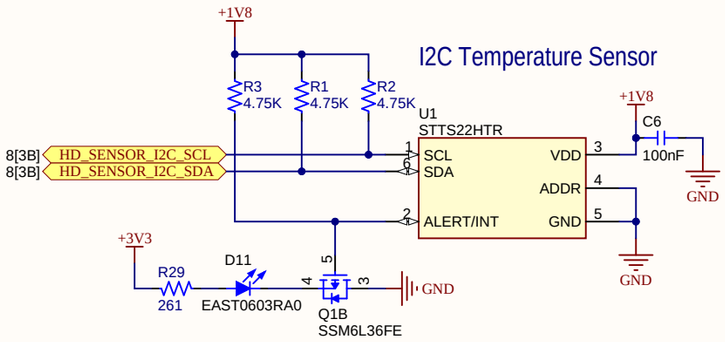

| | | | |
|---|---|---|---|
| Avnet Engineering Services | | | |
| Project Name: ZUBoard 1CG | PCB Rev: 1 | BOM: 02 | Variant: 02 |
| Doc Num: SCH-ZUB-1CG | Date: 05-Aug-22 | Time: 1:59:36 PM | |
| Sheet Title: 13 - SYZYGY, Click Expansion.SchDoc | Size: C | Sheet: 13 of 17 | |

# I2C & SPI Sensor, ON/OFF CONTROLLER

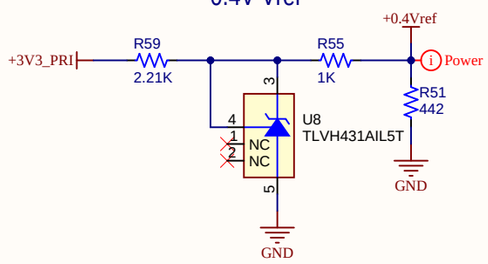
## SPI Pressure Sensor




## I2C Temperature Sensor

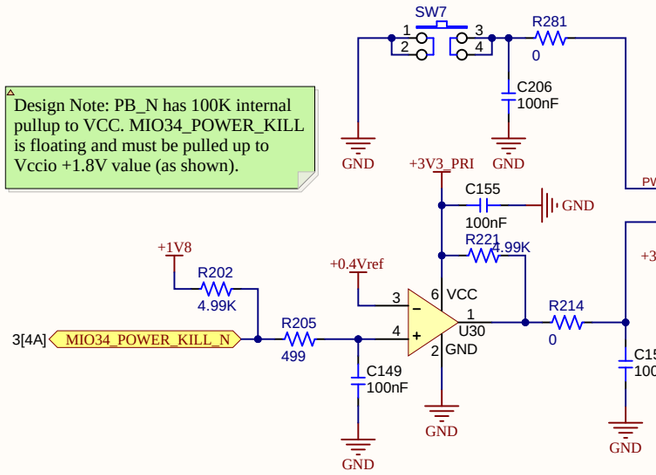



## 0.4V Vref

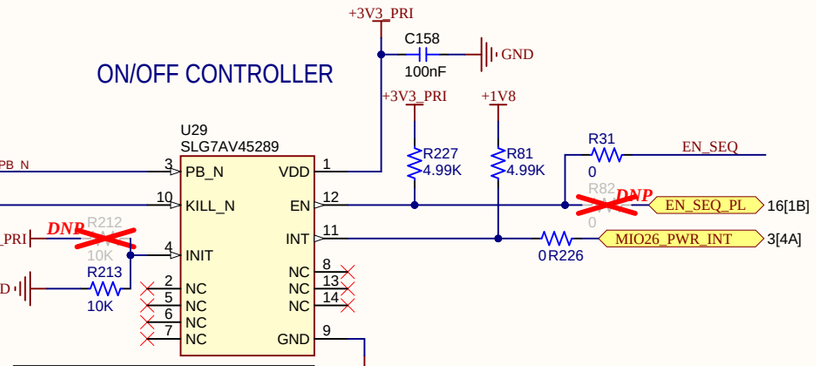



## POWER BUTTON

Design Note: PB_N has 100K internal pullup to VCC. MIO34_POWER_KILL is floating and must be pulled up to Vccio +1.8V value (as shown).

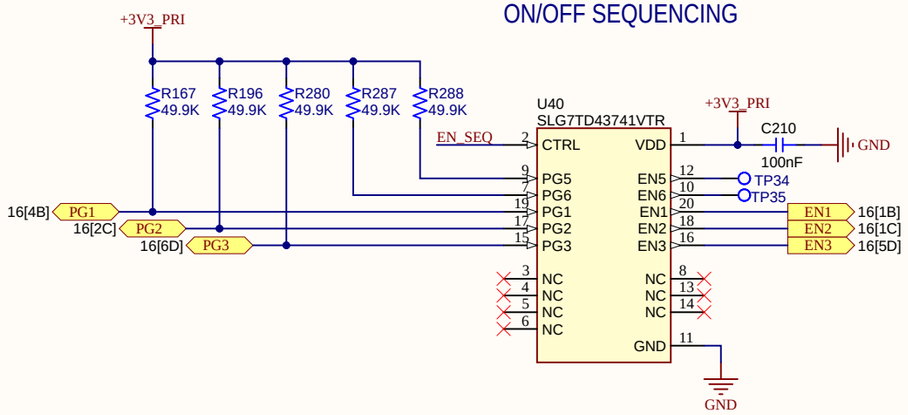



## ON/OFF CONTROLLER




USER NOTE: R212 & R213 configures the board power up operation.
Position R213 Populated (default): user must press Power On switch.
R212 Populated: board powers up when power applied.

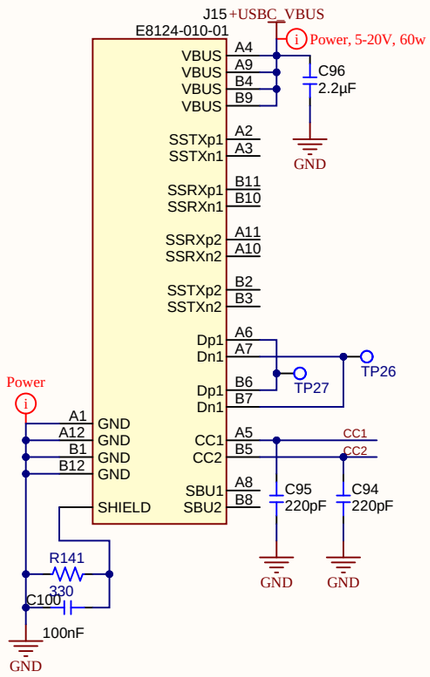
## ON/OFF SEQUENCING



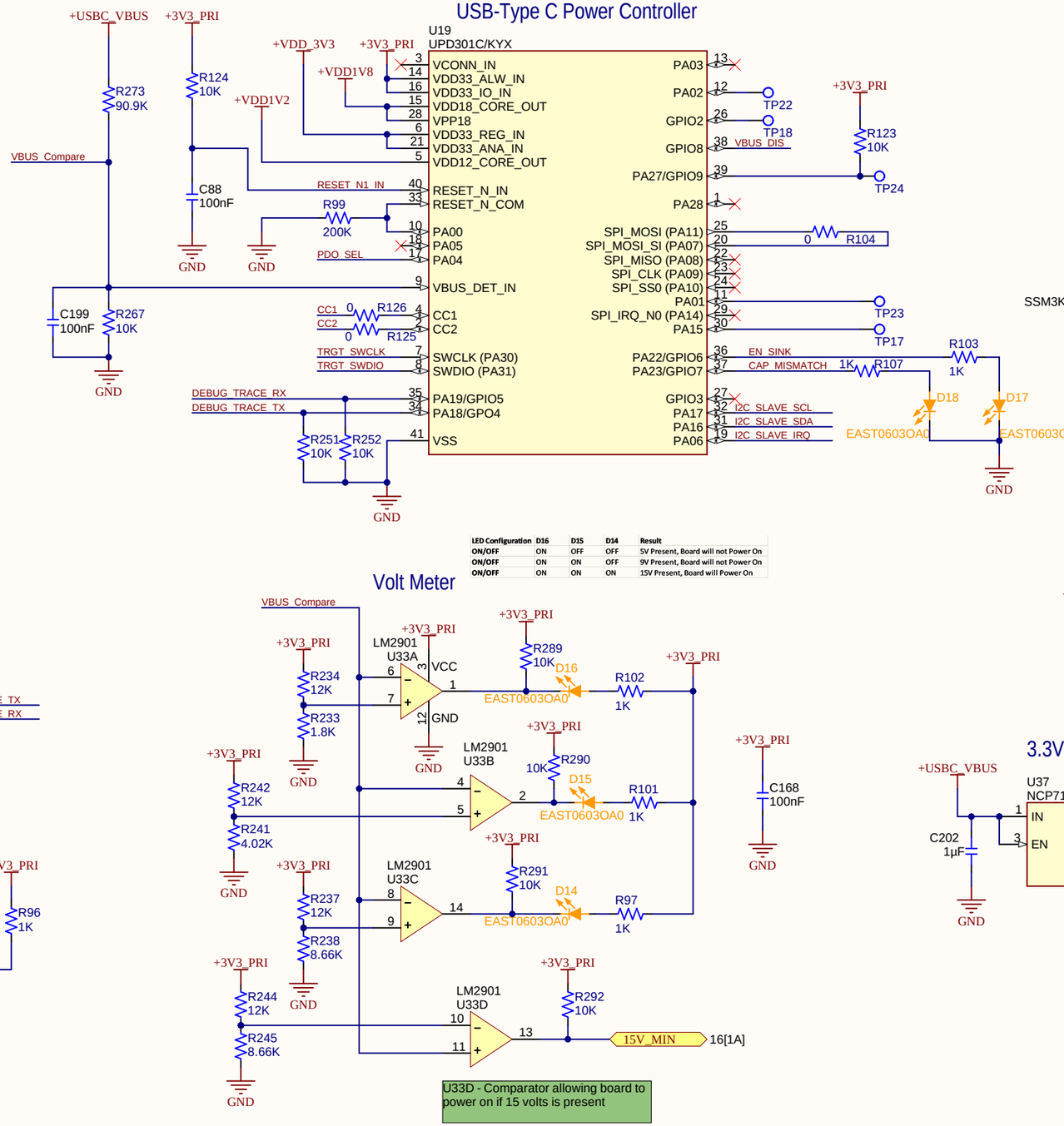

| | | | |
|---|---|---|---|
| AVNET Avnet Engineering Services | | | |
| Project Name: ZUBoard 1CG | PCB Rev: 1 | BOM: 02 | Variant: 02 |
| Doc Num: SCH-ZUB-1CG | Date: 05-Aug-22 | Time: 1:59:36 PM | |
| Sheet Title: 14 - I2C & SPI Sensor, Power On Enable.SchDoc | Size: C | Sheet: 14 of 17 | |

# USB-C Power In

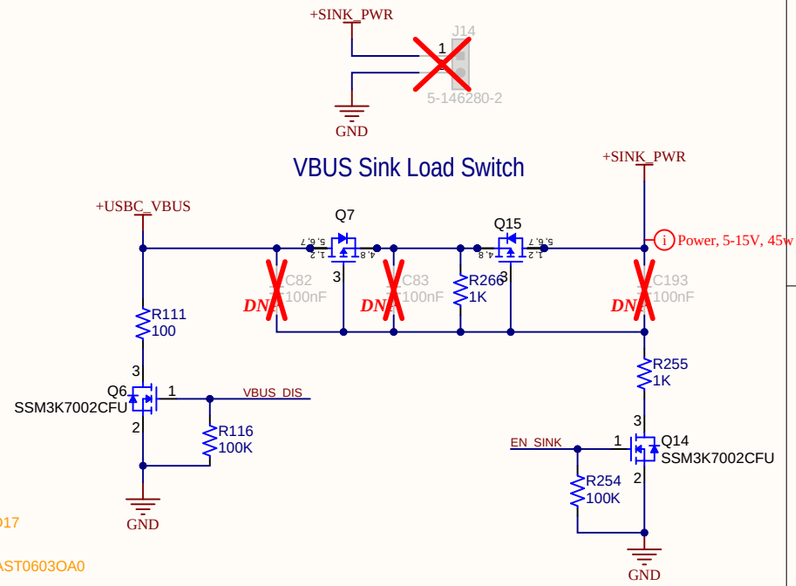
## USB-Type C Power In Connector



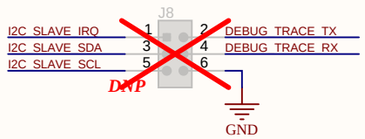

## USB-Type C Power Controller



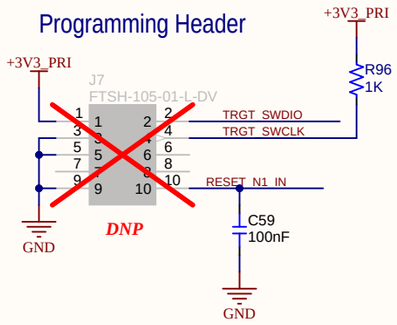

## VBUS Sink Load Switch




## Debug Header




## Programming Header



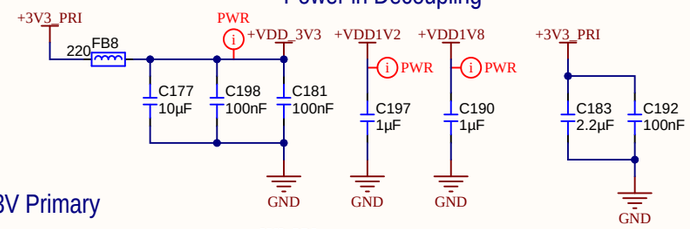

## Volt Meter

| LED Configuration | D16 | D15 | D14 | Result |
|---|---|---|---|---|
| ON/OFF | ON | OFF | OFF | 5V Present, Board will not Power On |
| ON/OFF | ON | ON | OFF | 9V Present, Board will not Power On |
| ON/OFF | ON | ON | ON | 15V Present, Board will Power On |

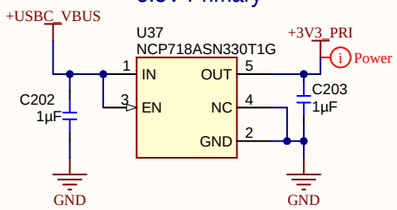



U33D - Comparator allowing board to power on if 15 volts is present

## Power in Decoupling

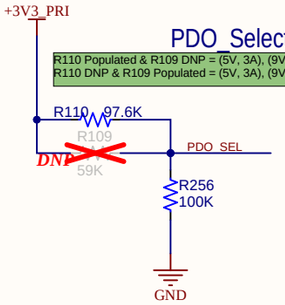



## 3.3V Primary




## PDO_Selection

R110 Populated & R109 DNP = (5V, 3A), (9V, 3A), (15V, 3A) Mode A
R110 DNP & R109 Populated = (5V, 3A), (9V, 3A), (15V, 3A) Mode B

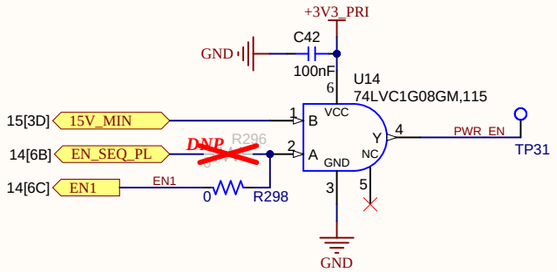



| | |
|---|---|
| Project Name: | ZUBoard 1CG |
| PCB Rev: | 1 |
| BOM: | 02 |
| Variant: | 02 |
| Doc Num: | SCH-ZUB-1CG |
| Date: | 05-Aug-22 |
| Time: | 1:59:37 PM |
| Sheet Title: | 15 - USB-C Power In.SchDoc |
| Size: | C |
| Sheet: | 15 of 17 |

Avnet Engineering Services

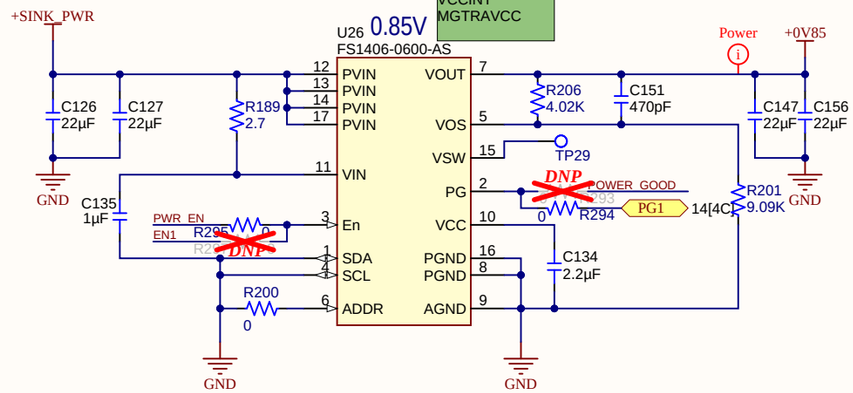
# Power Supplies

## 15V Min PWR On

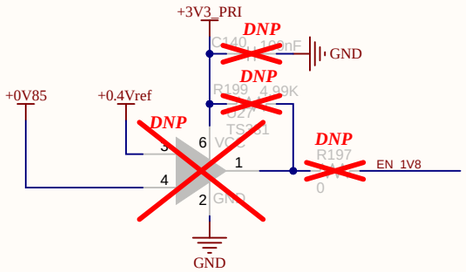



## U26 0.85V — FS1406-0600-AS

+0V85 Supplies:
VCC_PSINTLP
VCC_PSINFP
VCCINT
MGTRAVCC

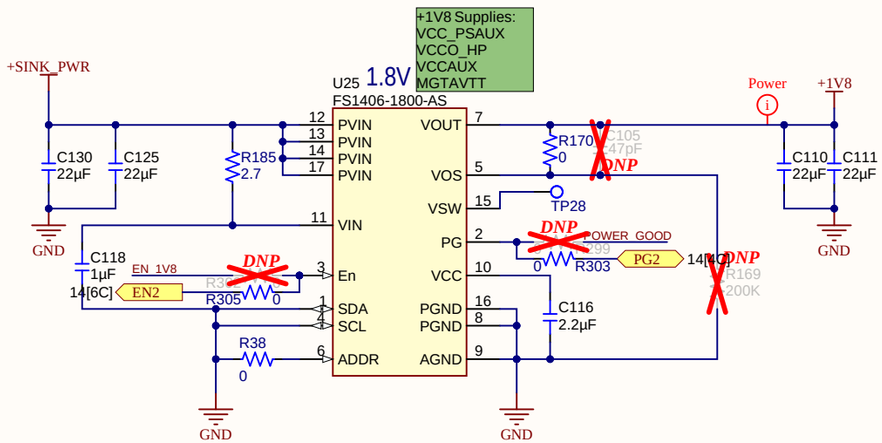



## 1.8V Enable



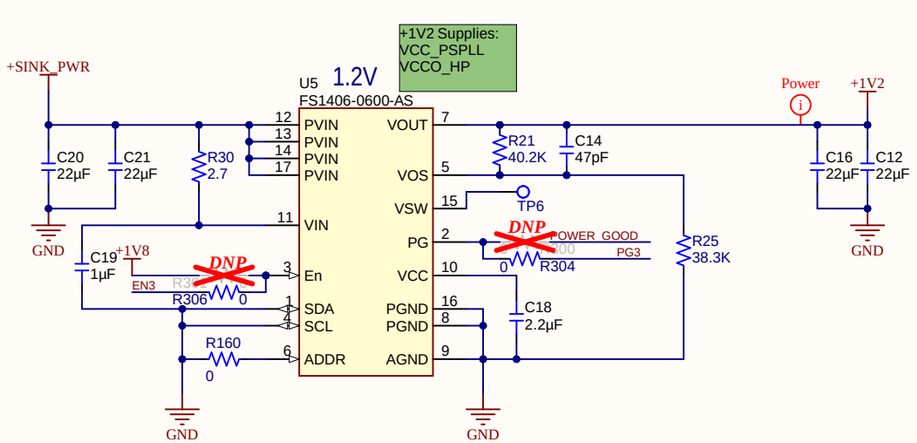

## U25 1.8V — FS1406-1800-AS

+1V8 Supplies:
VCC_PSAUX
VCCO_HP
VCCAUX
MGTAVTT

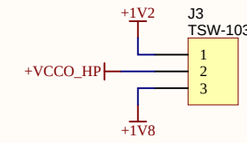



## U5 1.2V — FS1406-0600-AS

+1V2 Supplies:
VCC_PSPLL
VCC_PSPLL
VCCO_HP



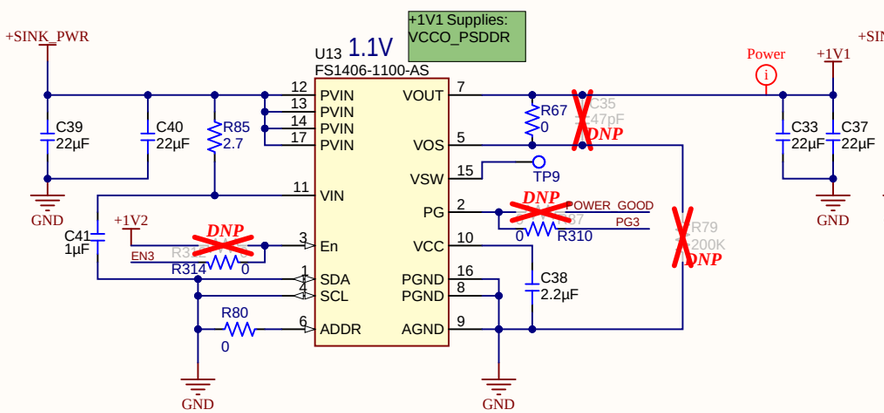

## +VCCO_HP Voltage Selection



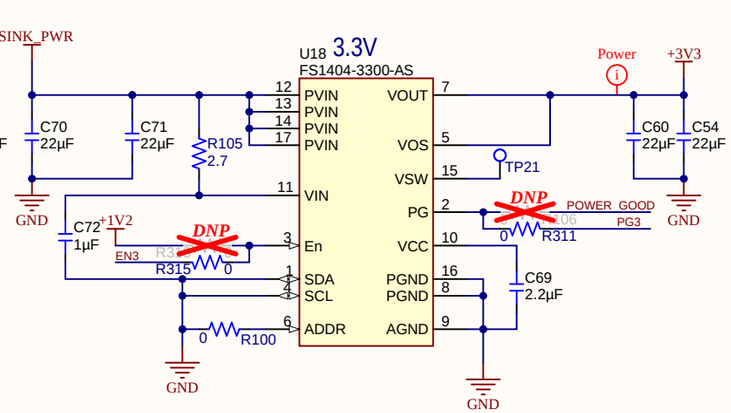

| Jumper Postion | +VCCO_HP Voltage |
|---|---|
| 1-2 | 1.2V |
| 2-3 | 1.8V |

## U13 1.1V — FS1406-1100-AS

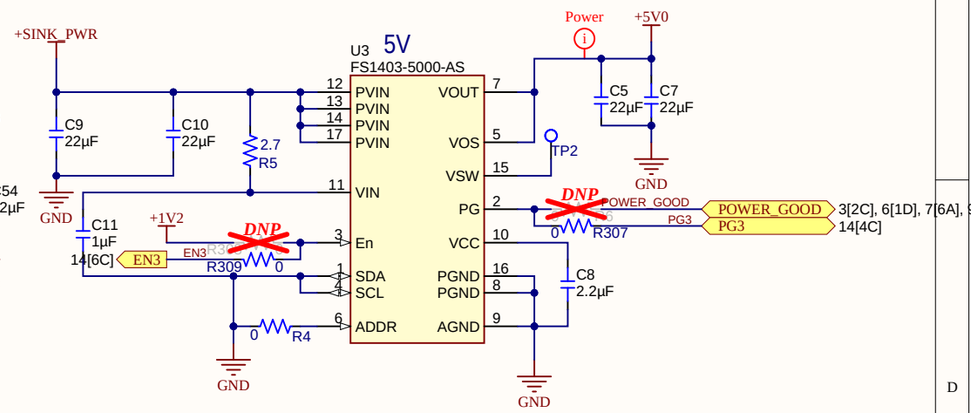
+1V1 Supplies:
VCCO_PSDDR




## U18 3.3V — FS1404-3300-AS




## U3 5V — FS1403-5000-AS




| | |
|---|---|
| AVNET | Avnet Engineering Services |
| Project Name: ZUBoard 1CG | PCB Rev: 1 / BOM: 02 / Variant: 02 |
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| Sheet Title: 16 - Power Supplies.SchDoc | Size: C / Sheet: 16 of 17 |

## Assembly:

Label1
BD-XXXX-XXXXX-G
Label, Product

Label2
XXXXXXX
Label, Serial Number

ESD1

ESD Bag

Label_ESD1


Label, ESD

SS1

Trash Can-Silk Screen

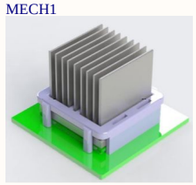
## Mechanicals:

PCB

PCB PN (In Copper)

## Heatsink

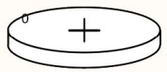
MECH1



EA-190-H095-T710

## Battery

MECH2



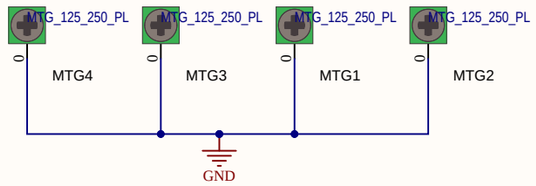
CSY-CR2032

**LAYOUT NOTE: Mech1 Keep keepout for Heatsink placement**

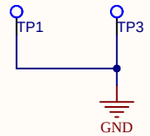
## Fiducials:

FID2 FID3 FID1 FID4 FID6 FID5

## Mounting Holes:




## GND Test Points:

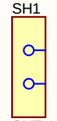



## PCB Bumpers

BMPR1 SJ61A4
BMPR2 SJ61A4
BMPR3 SJ61A4
BMPR4 SJ61A4
BMPR5 SJ61A4

## Shunt

SH1



SNT-100-BK-T

## SD Cards

SD1

S416GSEJL-U3000-3 *DNP*

SD2

SDSDQAF3-064G-XI *DNP*

## Power Supply

MECH3

PSA-A45WM-U *DNP*

## USB Cables

MECH4

C06026-00013 *DNP*

MECH5

68784-0003 *DNP*

| | | | |
|---|---|---|---|
| Avnet Engineering Services | | | |
| Project Name: ZUBoard 1CG | PCB Rev: 1 | BOM: 02 | Variant: 02 |
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