Summary of the Pisa Workshop on Precision Vertex Detectors for FCCee: Oct 30-31, 2025

Carl Haber, Christoph Paus

Program

- Group Presentations: 7 European groups + a US survey
- Constraints and Requirements: Physics requirements and Backgrounds
- Layout and Simulation: Layout comparisons, alternatives, exp from Belle II, background rejection
- Sensor R&D: ~6 different MAPS sensors/projects were discussed
- Mechanical Developments: beam pipe,
- Systems and Readout
- Discussion

The next 4 slides were shown by me concerning the US community and interests

Data

- The data is inaccurate
- The community was surveyed in an EOI process in Spring of 2024 for the MIT US FCCee Workshop
- A resurvey was performed recently with only partial responses
- The surveys overstate the actual effort underway at present
- Why?
  - Little current funding
  - Many immediate efforts – HL-LHC etc
- The data likely understates the eventual effort, once FCCee is approved
- Note: the US community just recently received guidance from funding agencies to focus on FCCee at CERN as the next major collider project

of Institutes Survey

Area of Interest	Future	Currently
MAPS Design	7	2
MAPS Test	11	
Vertex Detector Design	6	
Outer Tracker	4	2
Low Mass Mechanics	5	1
PID	3	3
Sil Wrapper	5	
S/W Tools	3	2
Simulation	5	2
Readout	3	

What are the current efforts?

- MAPS design using ASIC capabilities at national labs
- R&D on straw tubes for the outer tracker
- Low mass materials for wire chambers
- Fast timing (LGAD) developments for ATLAS/CMS/EPIC, and R&D (none of this is specifically for FCCee but is relevant)
- Development of s/w tools
- Performance simulation efforts
- All the national labs are involved in either current R&D or in organizational roles

Strengths and capabilities for longer term

- ASIC and electronics design
  - MAPS
  - dN/dx
  - AI/ML in front ends
- Readout/DAQ
- Low mass mechanics
- Tracker systems and assembly
- Powering
- Tracking software
- Physics performance simulation

Constraints and Requirements

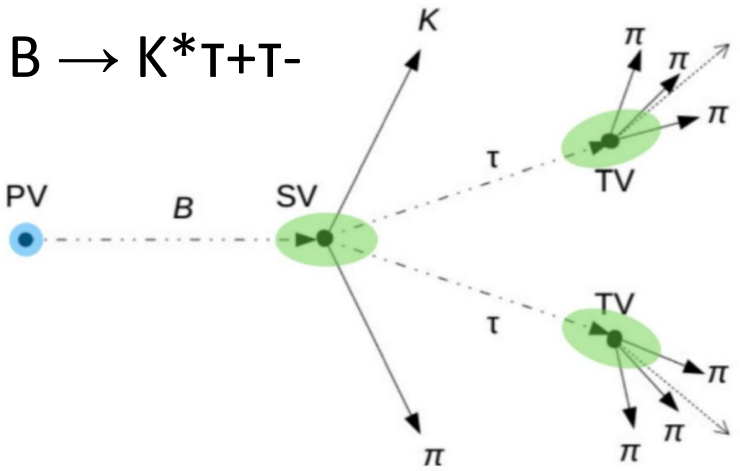
Every aspect of the Physics program needs an excellent vertex

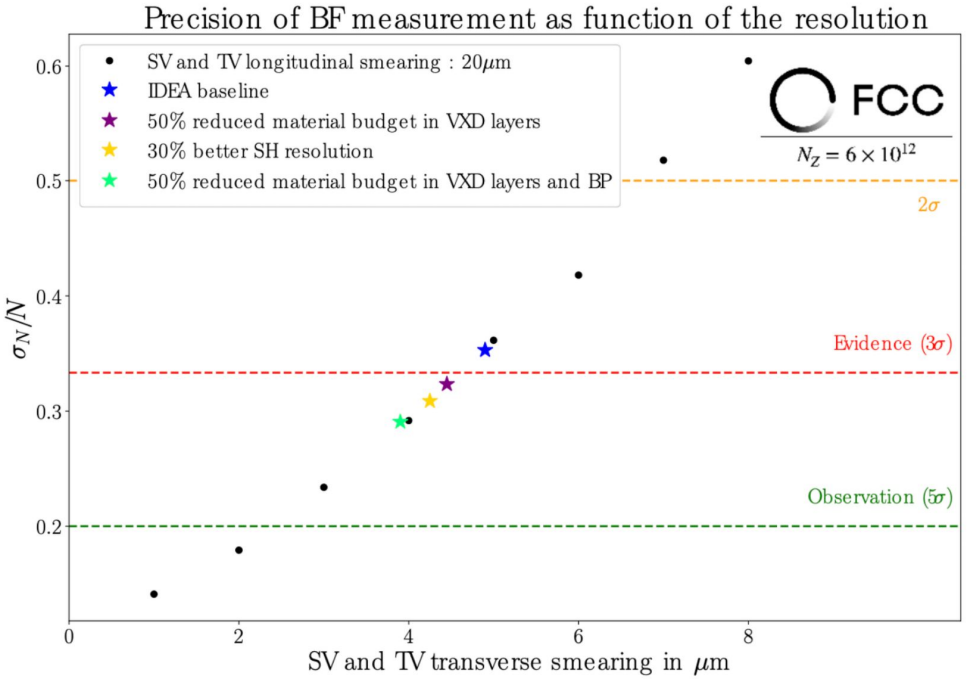
- HIGGS: Jet flavour identification (tagging) of b-, c-, g-, tau- etc… Measure of Higgs couplings
- Z: Jet flavour identification (inclusive tagging) but also exclusive tagging for HF EWK observables Rb, Rc, AFB(b,c)
- W: Jet flavour identification (tagging/calibration), CKM parameters Vcb
- FLAVOUR: precise reconstruction of PV/SV/TV for flavour physics e.g.:
  - time dependent CPV measurement
  - rare decays like $B \longrightarrow K^{*}\tau^{+}\tau^{-}$
  - τ precise lifetime measurement
- [BSM: long lived particle signatures]

Constraints and Requirements

Key elements

- low material budget
  - special lightweight and smallest possible radius beampipe ~ 10 mm
  - minimum vertex tracker material: main issue is resolution
- short distance to the beam: default location 12 mm … maybe closer?
- impact is significant
- performance goal is ±3 µm to see B ⟶ K*τ+τ-

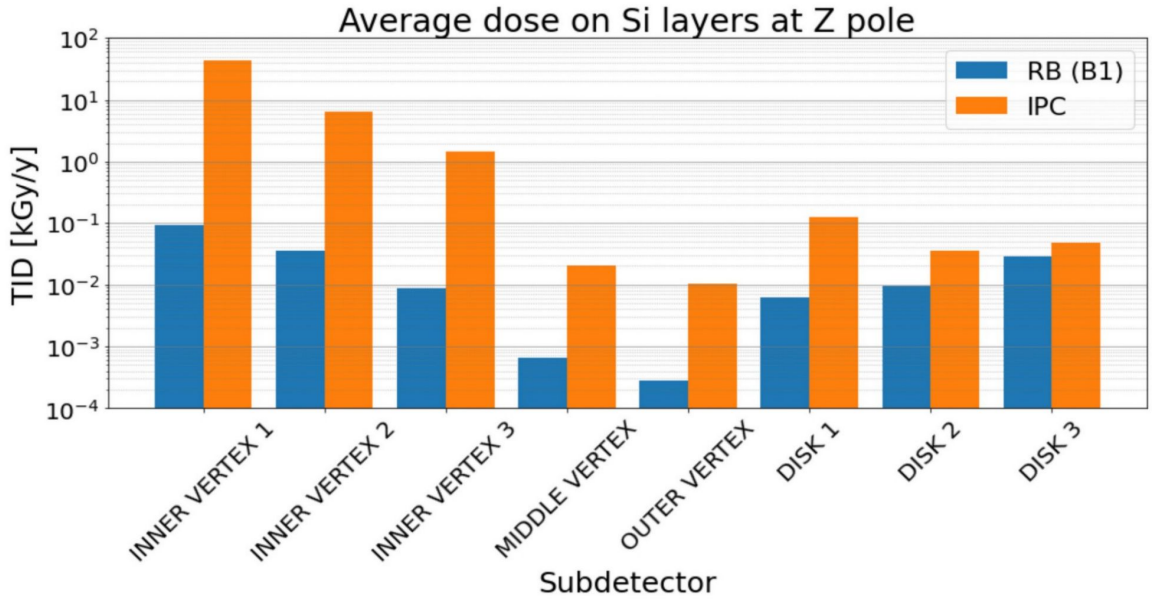




Constraints and Requirements

Most stringent constraints

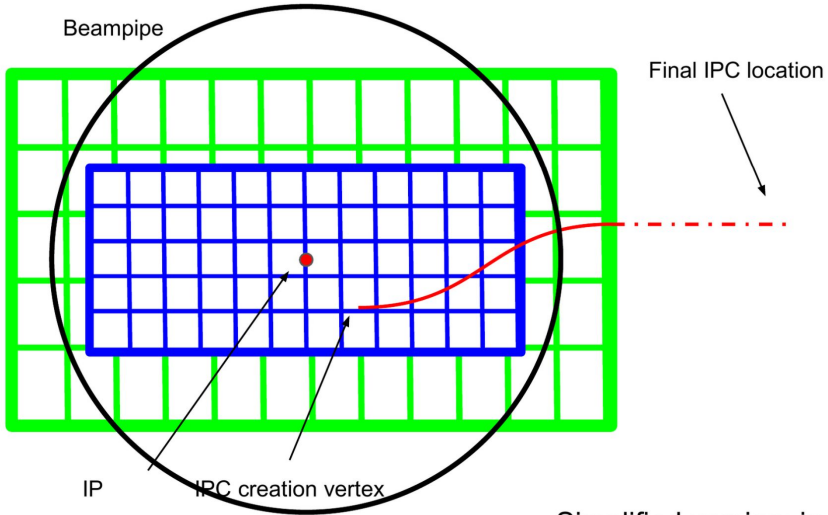
- beam induced background (BIB) dominated by incoherent pair creation (IPC) right after radiative Bhabha (RB)
- studies ongoing … standardized samples and cross check Guinea Pig versus WarpX are planned
- possibly normalize programs to LEP data?



Guinea Pig

simulation grid

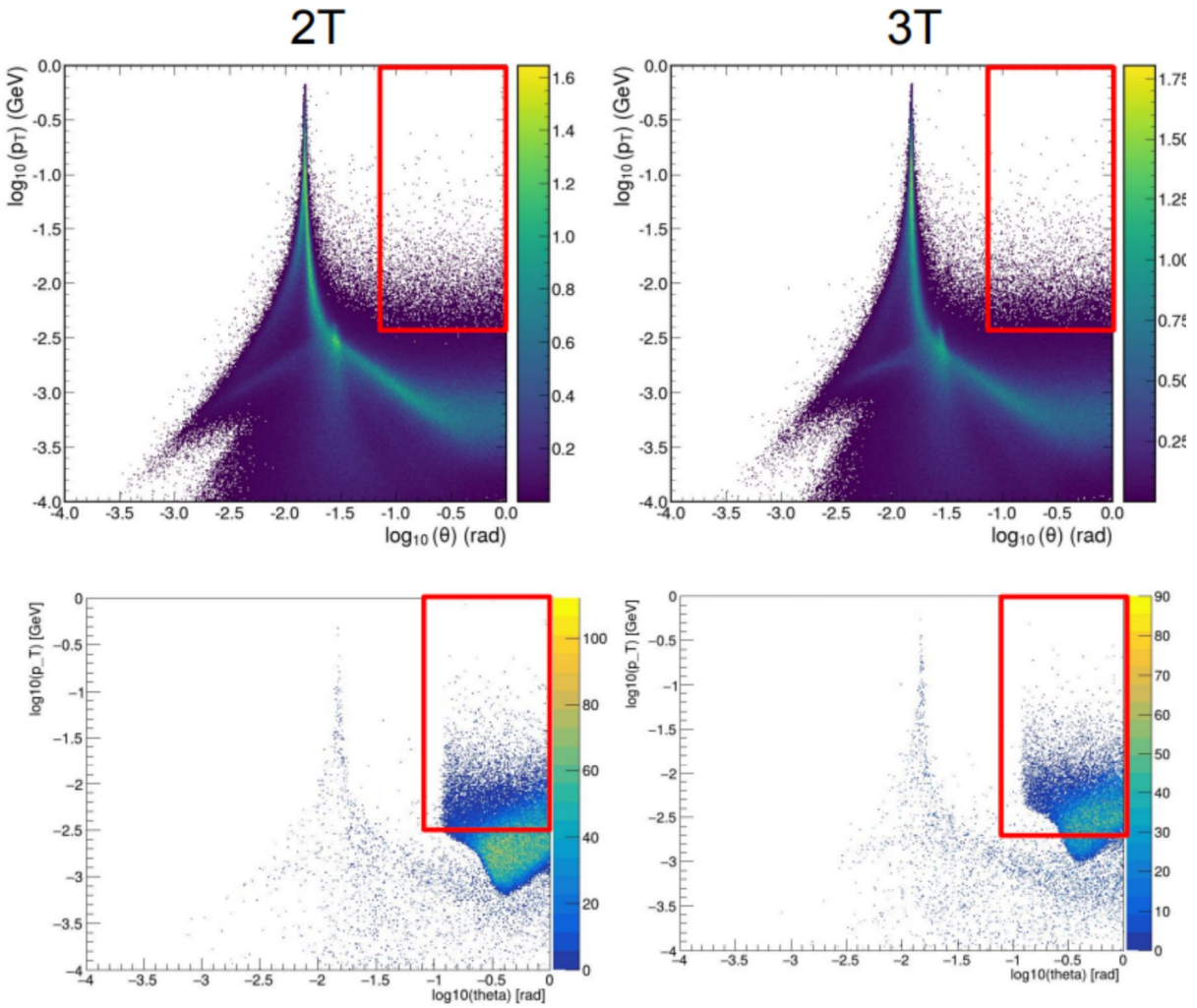
for IPC creation



Constraints and Requirements

Most stringent constraints

- present status of occupancy from full simulation not yet fully converged
- beam crossing generator under study: occupancy is at the upper end
- can we cool the power and does the chip function?



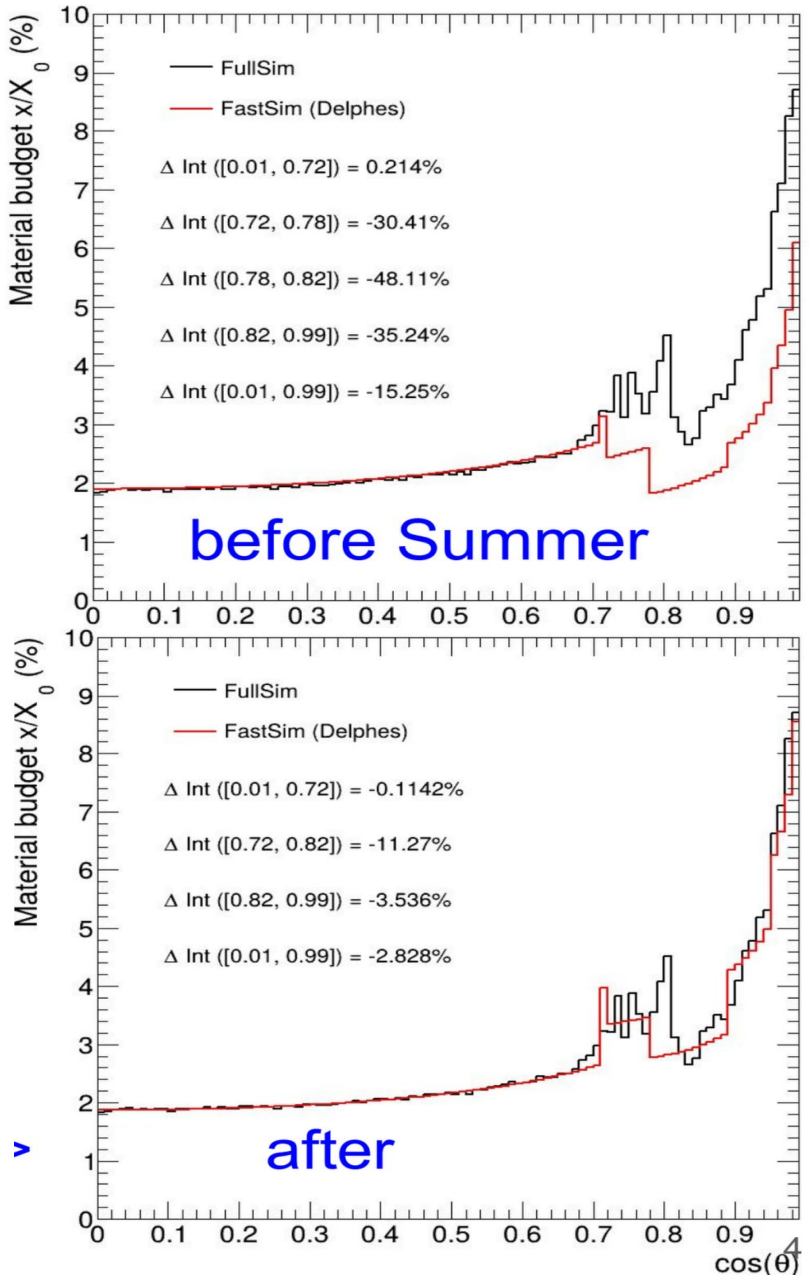
Layout and Simulation

Parametric simulation was carefully compared to full simulation and various fixes applied

Various geometries implemented and tested:

1. Short Barrel Geometry (aiming to use bent stitched MAPS)
   a. Reduced barrel length (~10 cm).
2. First Layer on Top of Beam Pipe
   a. Moves first layer closer to IP (without entering the beam pipe).
3. First Layer Inside the Beam Pipe
   a. More aggressive layout, innermost radius moved to 8–10 mm.
   b. Requires re-engineering of beam pipe and cooling strategy.

Gains are as expected: *see presentation for details*



Sensor R&D

- TPSCo 65nm imaging technology, DRD7, ALICE ITS3, advanced stitching
- Fermilab: LGADs, FCFD, Arcadia bench tests, 3D integration, Skywater
- OCTOPUS: 14 members aim at thin vtx for FCCee, DRD3 full WG structure, TPSCo 65 nm, optimized for FCCee specs,
  - Spatial resolution: 3 µm • Time resolution: 5 ns • Power consumption: < 50 mW/cm2 • Hit rate: 100 MHz/cm2
  - Novel electrode geometry
- ARCADIA and Lfoundry 110 (INFN): a broad project targeting colliders, astro, x-rays, medical; includes gain layers (LGAD), thick depletion layers
- 2nd ARCADIA talk on characterization and test beams
- NAPA: SLAC based, ~ns timing, MAPS
- CE-65 (TPSCo 65) characterization project

Sensor R&D comments

- US has good stand-alone efforts, with significant expertise, and interest, particularly related to fast timing applications
- Very significant, well funded, large collaborations in Europe on MAPS

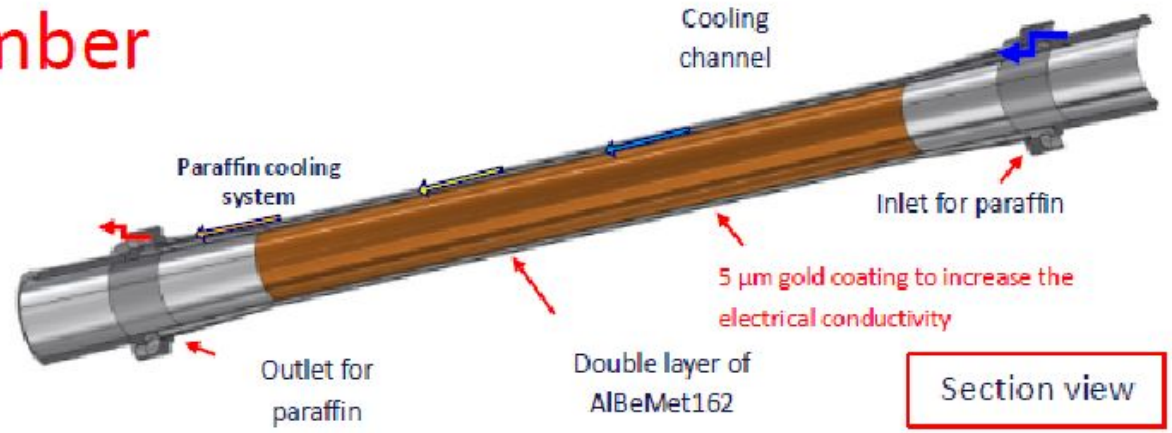
Mechanical

- INFN LNF and Pisa are undertaking detailed studies and prototyping of the vertex region including
  - Beam pipe: design, mockup of IR, paraffin cooling
  - Cooling
  - Services
  - Support tube
- Air cooling study: prototype system at INFN-Pisa (lab tour)
- Curved MIMOSIS: French project to gain direct experience with sensor bending using existing MIMOSIS sensors, aimed at FCCee

FCC-ee IR central chamber

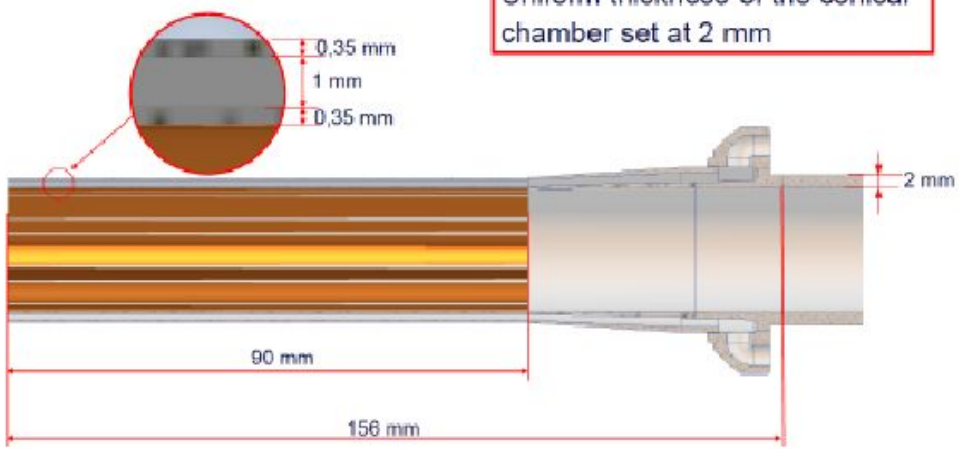
- AlBeMet 162 (62% Be, 38% Al)
- 180 mm long centered at the IP

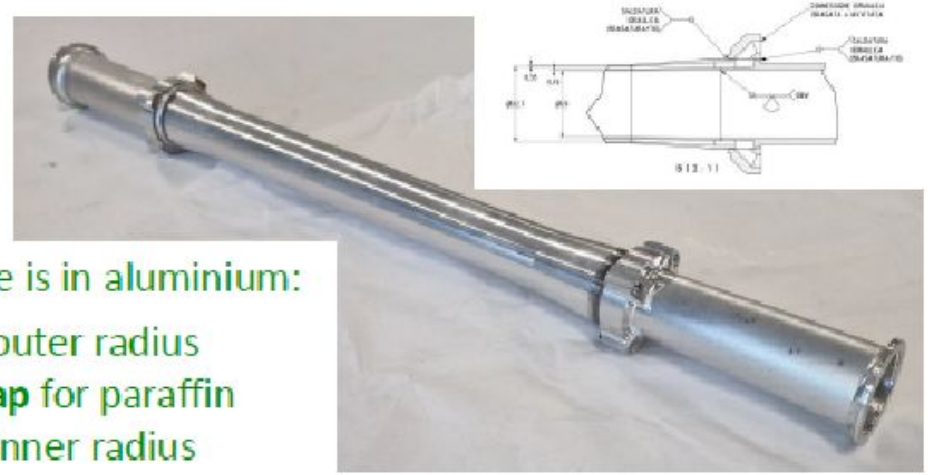
- **0.35 mm** outer radius AlBeMet162
- **1 mm gap** for paraffin
- **0.35 mm** inner radius AlBeMet162



Thickness of the chamber

Uniform thickness of the conical chamber set at 2 mm





The prototype is in aluminium:

- **0.35 mm** outer radius
- **0.9 mm gap** for paraffin
- **0.45 mm** inner radius

Leveraging Belle-II beam pipe design (0.4 mm Be +0.6 mm Be + 1mm paraffin)

Current vertex layout

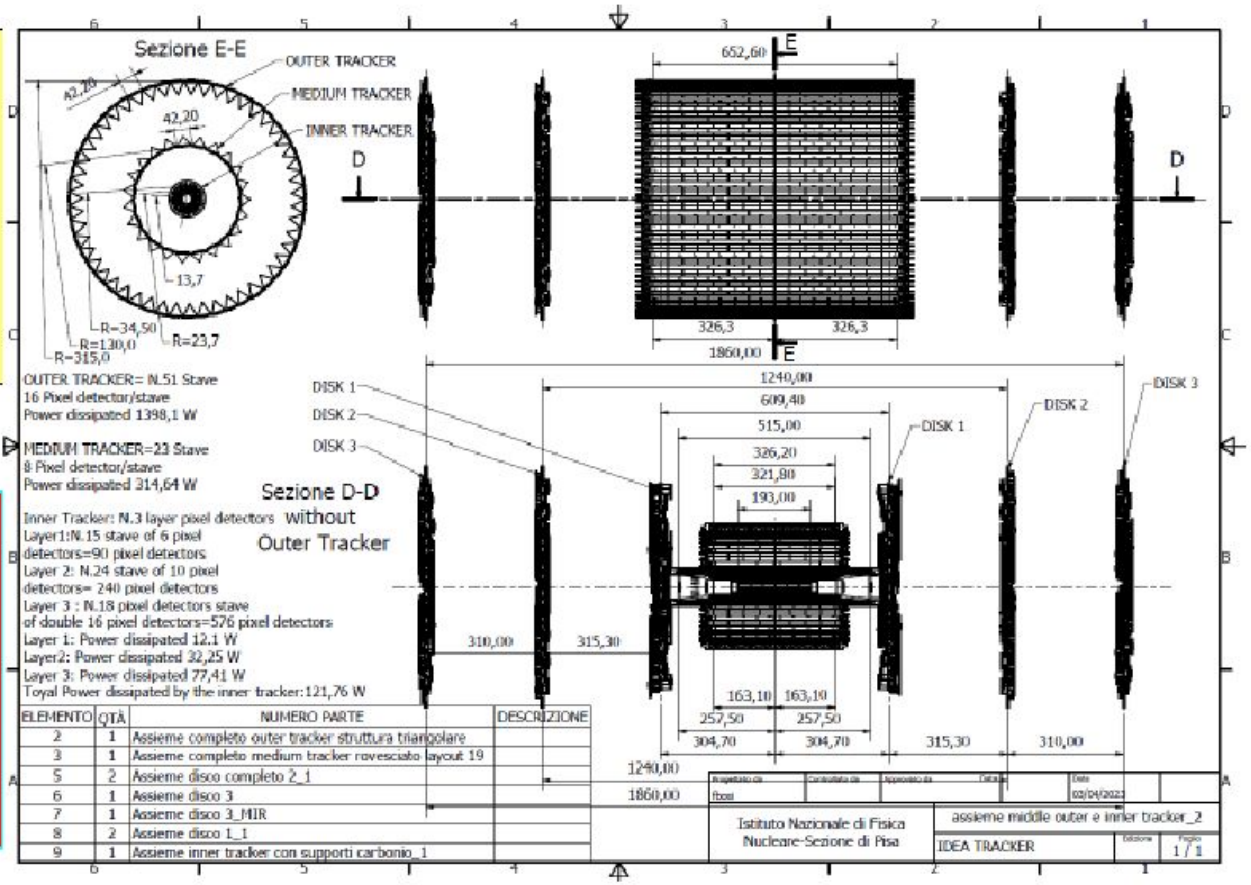
Outer vertex tracker:
ATLASPix3 based

Modules of $50 \times 150\ \mu m^2$ pixel size
- Intermediate barrel at 13 cm radius
- Outer barrel at 31.5 cm radius
- 3 discs per side

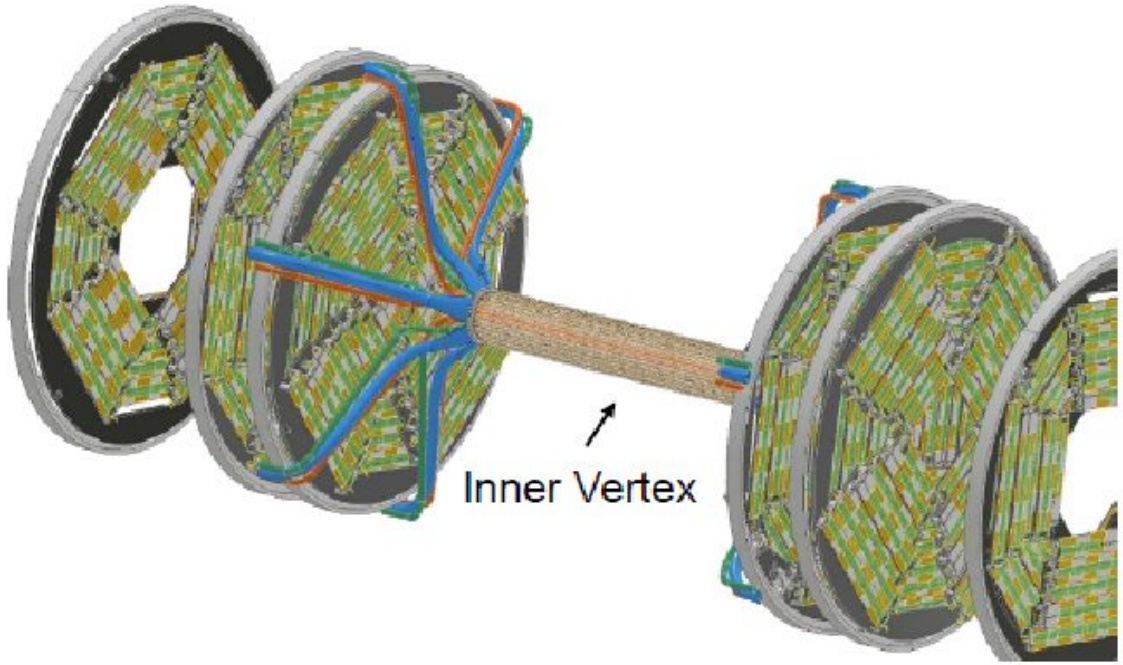
Inner Vertex detector:
ARCADIA based

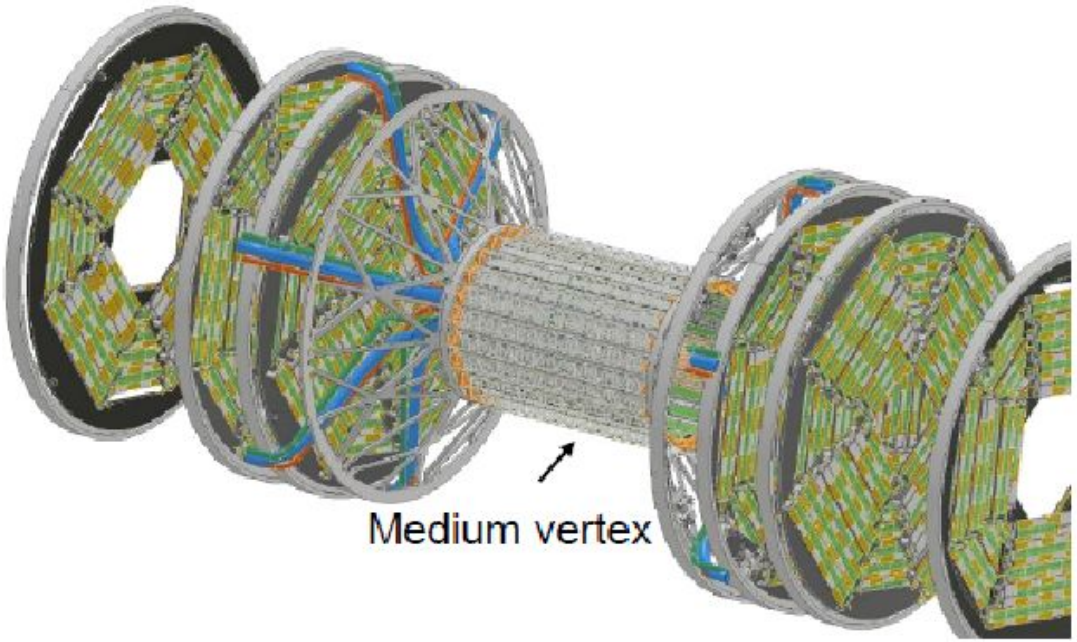
Modules of $25 \times 25\ \mu m^2$ pixel size

3 barrel layers at
- 13.7, 23.7 and 34/35.6 mm radius



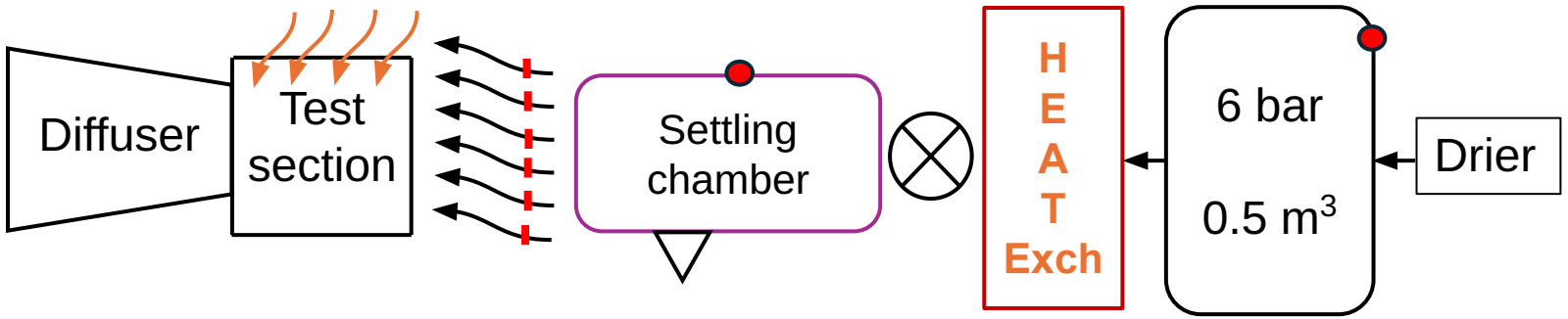
Radial inlet/outlet



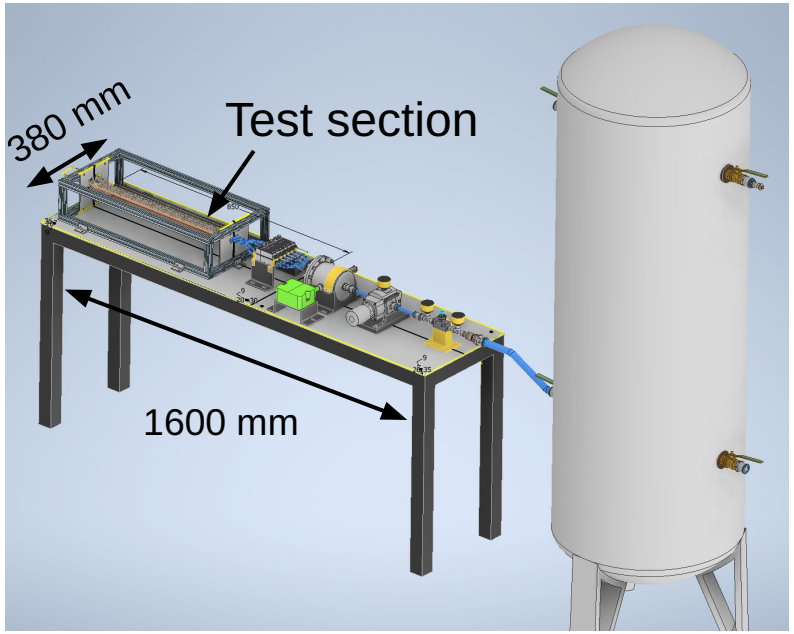


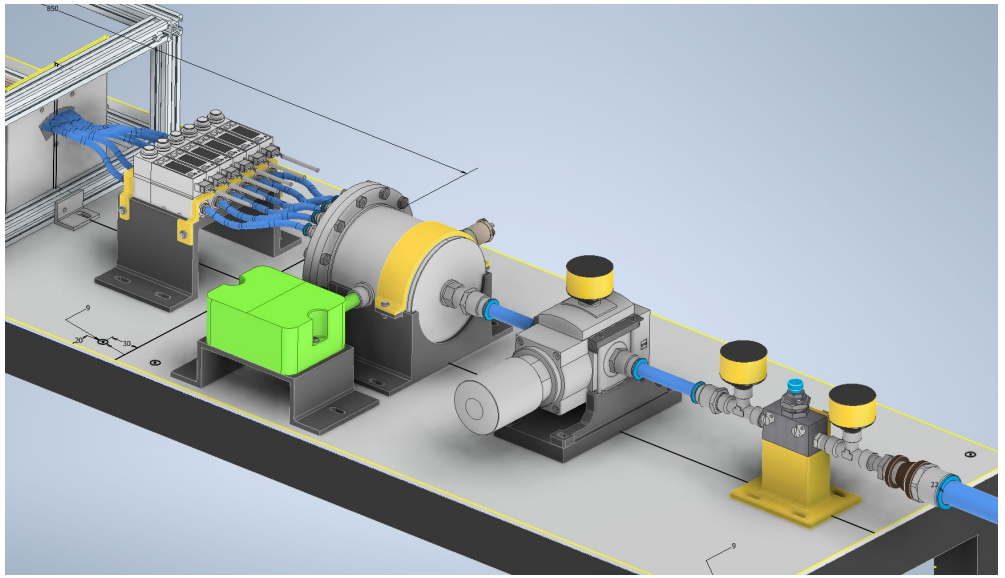
In this solution the Pipe system and cables wraps around the innermost disk.
This:

- Minimize the effect on the other disks
- But need an adequate assembly procedure.



- Flowmeters
- Absolute Pressure sensor
- Temperature/Humidity sensor
- Valve group
- RTD





Designed to:

- Be **adaptable**
- Be **controlled**
- Allow **CFD result verification**

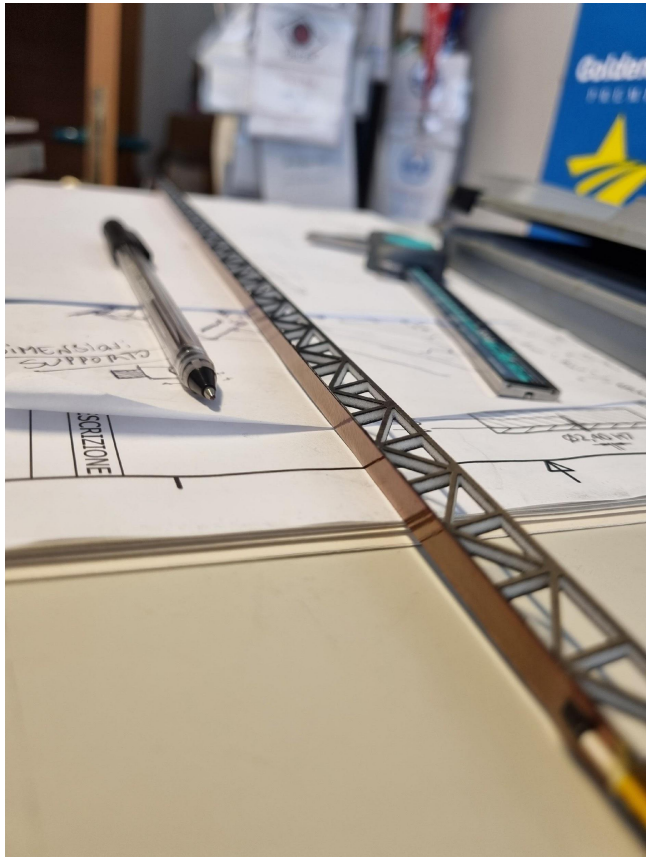
CONCLUSIONS:

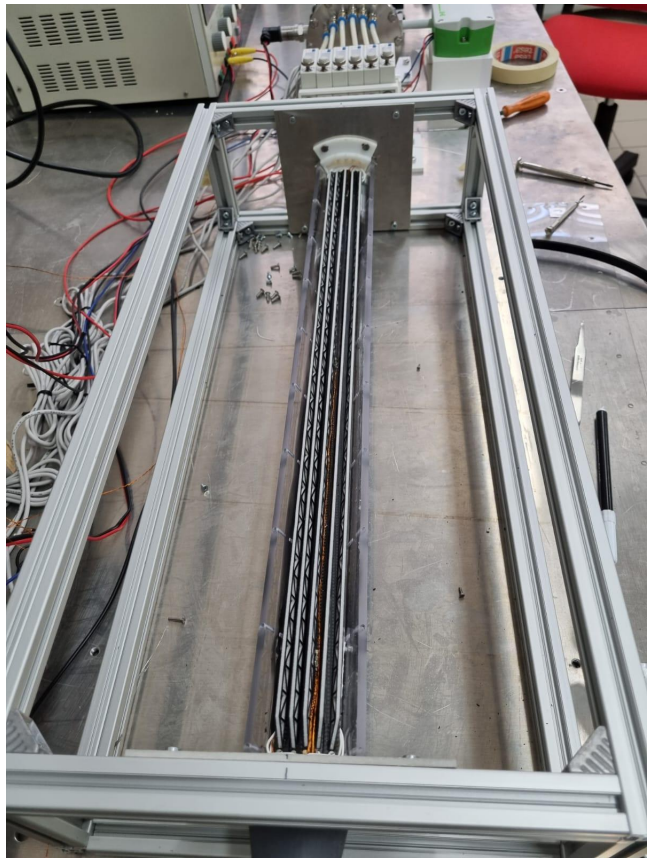
1. The air cooling system seems to be adequate for the case study

2. The compressed air system is stable and dynamic, allowing continuous testing for different solutions

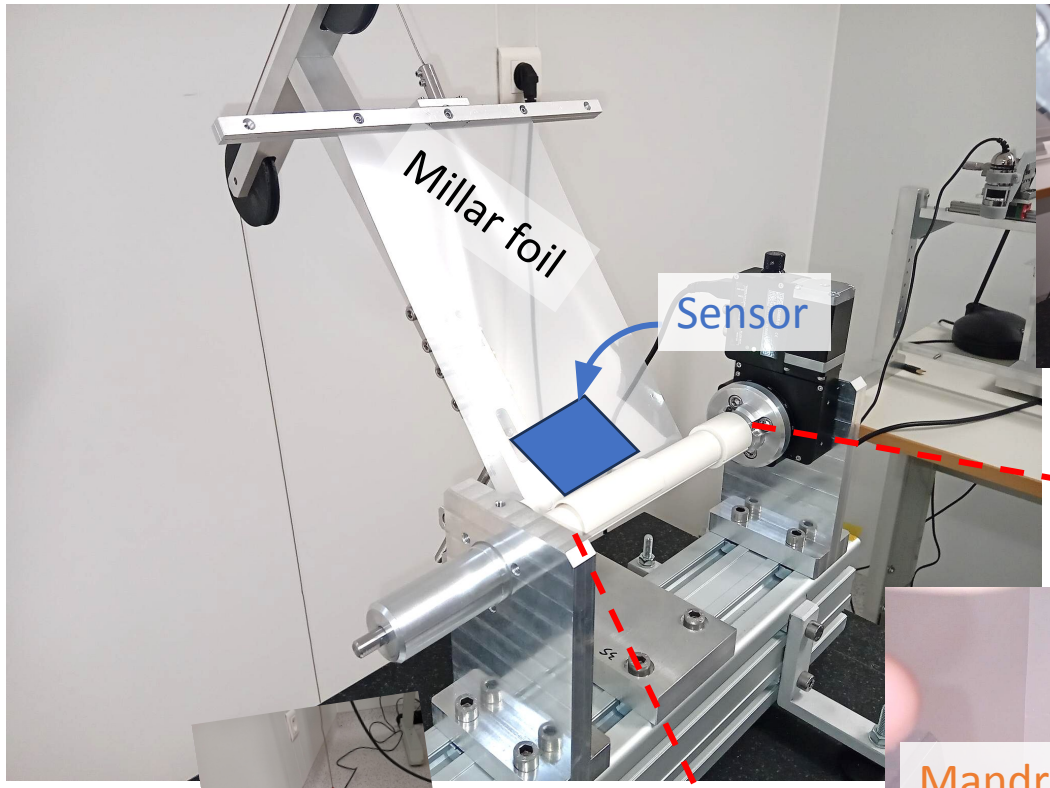
3. It's possible to control and monitor the properties of the air being introduced into the test section in terms of:
   - ***Flow rate (Pressure)***
   - ***Humidity***
   - ***Temperature***

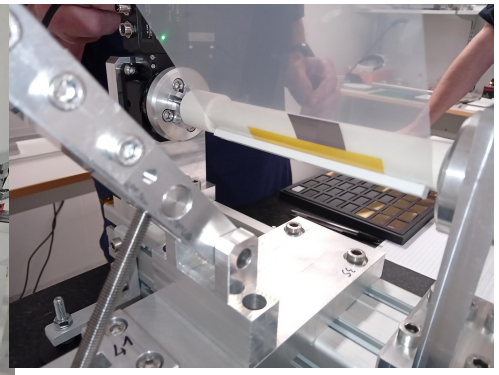
4. The maximum flow rate required for cooling is determined by the vibration allowed by the structure

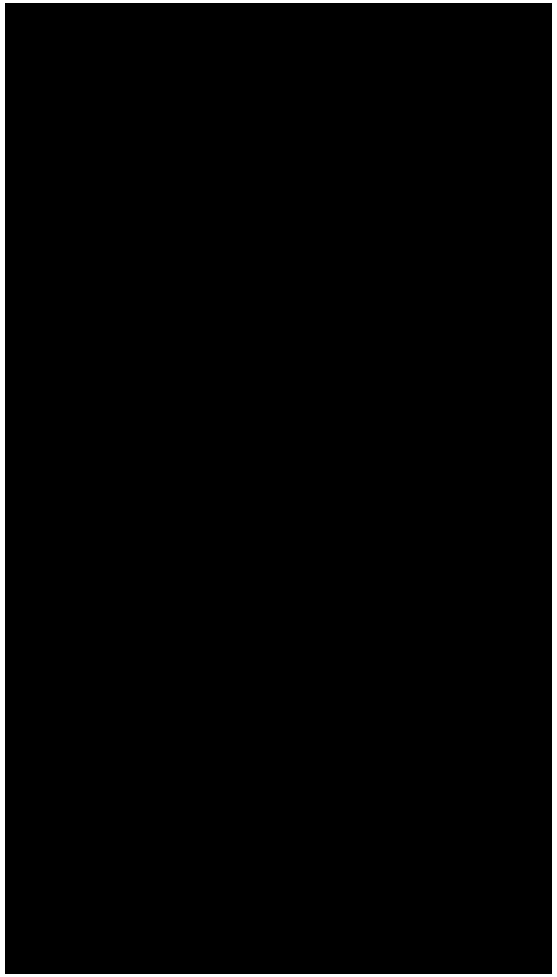




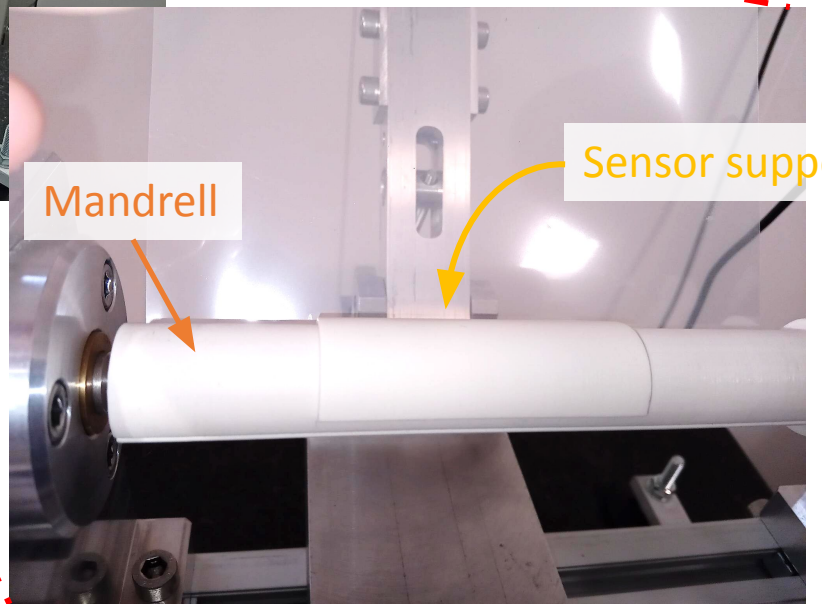
Sensor Bending







counterweight



System and Readout

- ATLAS pixels serial power (cancelled)
- EIC serial power (cancelled)
- Serial power and flex R&D: CCF + Oxford consortium looking at low mass flex, system design and test, novel in-house PCB fabrication, leveraging ATLAS pixel chip efforts
- Low mass packaging R&D: Trento/Torino/FBK: Al PCB integrated with ALPIDE, HEP and space applications, hi-freq design and test, low mass in-house process
- Wireless communications
- Trigger vs triggerless readout (Christoph)
  - bottomline: triggerless is desired and potentially possible, but more studies needed

Developments in serial powering and light flex PCB for future Higgs Factories

FCC-ee vertex detector R&D workshop
Pisa, 30-31 October 2025

Attilio Andreazza

Università di Milano and INFN

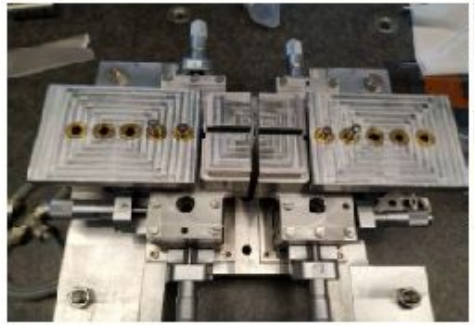
On behalf of:

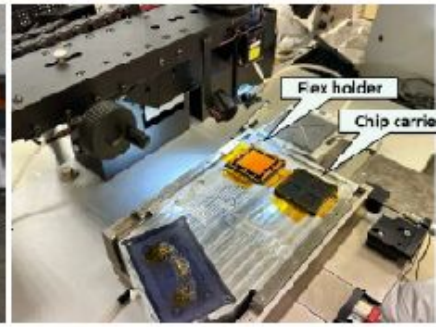
- **DRD3 CCF Project Proposal** Birmingham, Bristol, Edinburgh, FBK, Heidelberg, Hochschule RheinMain, IHEP, KIT, Lancaster, Milano, Pisa, Torino, Trento
- **Oxford** (D. Bortoletto, R. Plackett, DMS Sultan)
- and with addition of stolen slides from DRD3 and DRD7 workshops...

UNIVERSITÀ DEGLI STUDI DI MILANO
DIPARTIMENTO DI FISICA

Al power and data bus

- Assembled modules with ATLASPIX3.1 chips
  - ~7 full modules with 150 µm sensors probed by Milano/Edinburgh
  - Dedicated jig and pick and place available

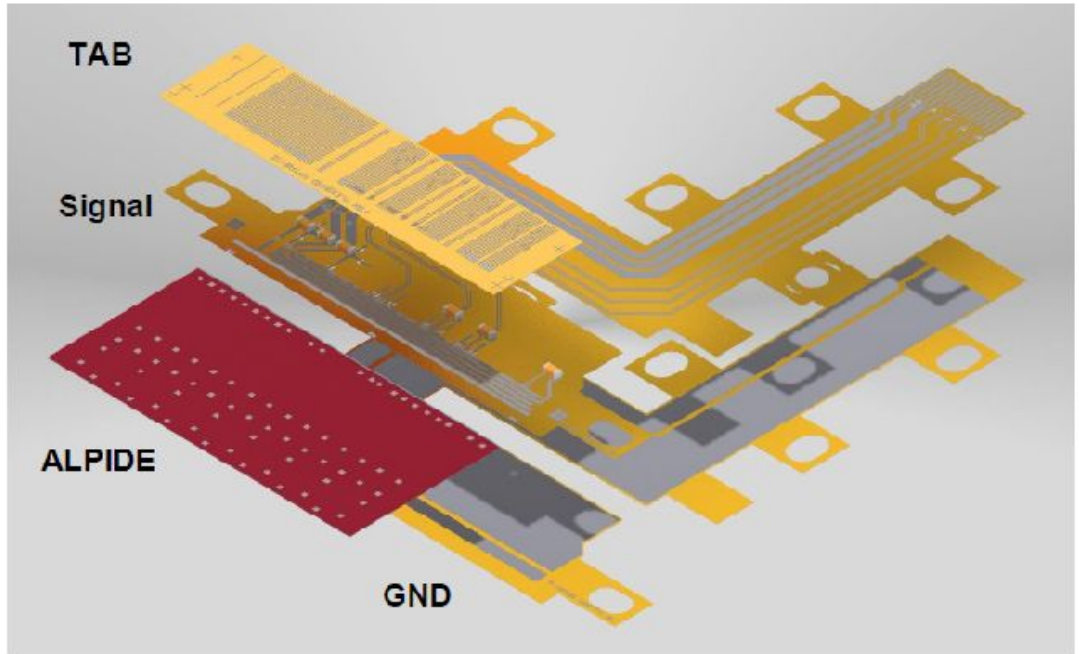




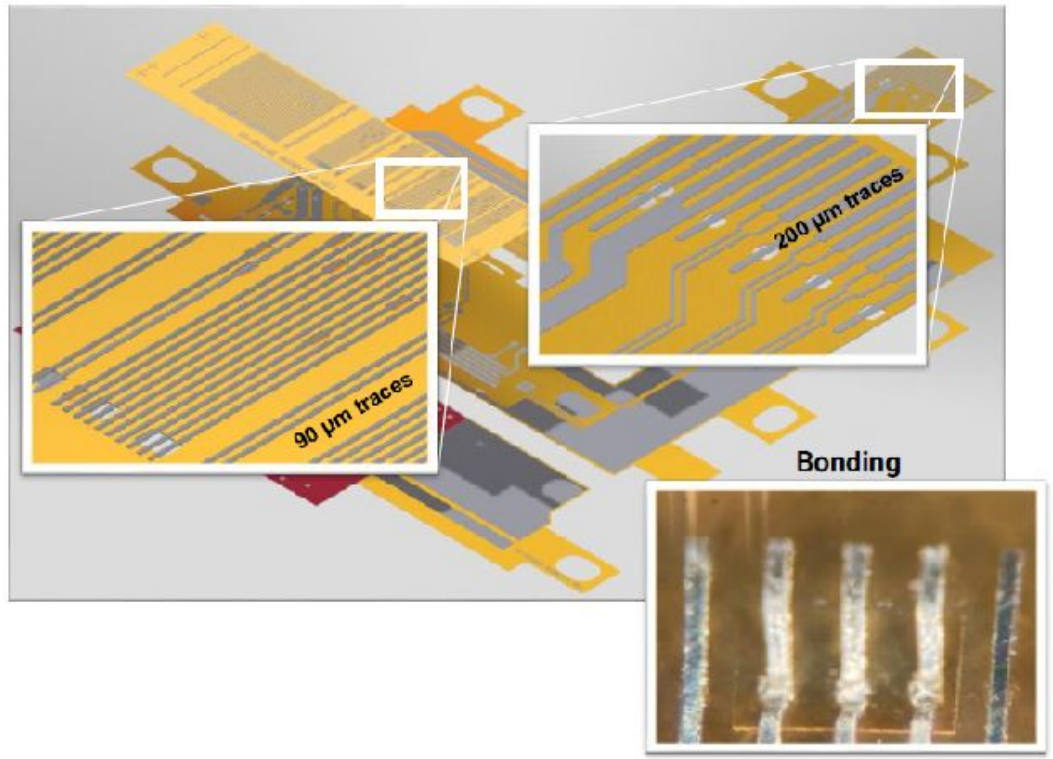
- Designed a power bus to test a multi-module serial power chain
  - Aluminium conductor to reduce thickness in radiation lengths
  - Connecting to modules by pigtails
  - 4 cm × 60 cm size to match CERN Microfabrication Lab capability
  - In production at **CERN** (Rui De Oliveira)

- Loading of cold plate (half stave with 3 modules + heaters)
  - CEPC long-stave design protype available in Pisa

Low mass Aluminium Flex Platform
ALPIDE integration with TAB

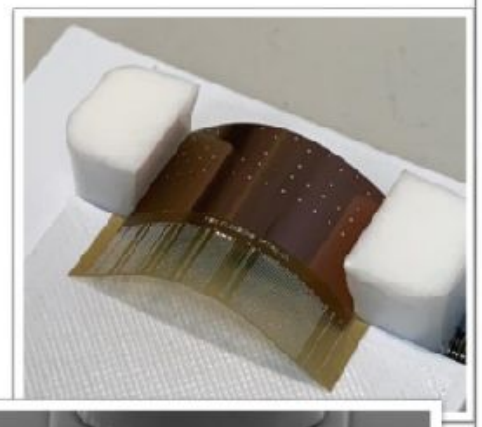


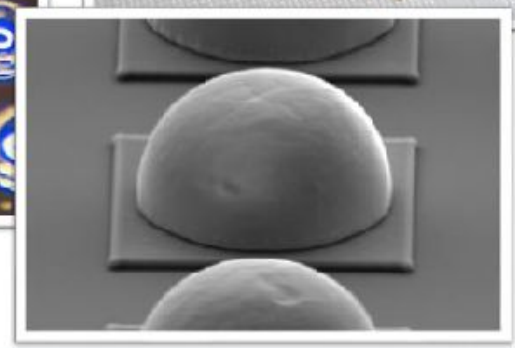
!! Design inspired from ITS3 tests with bent ALPIDE [1] and adapted for spTAB !!

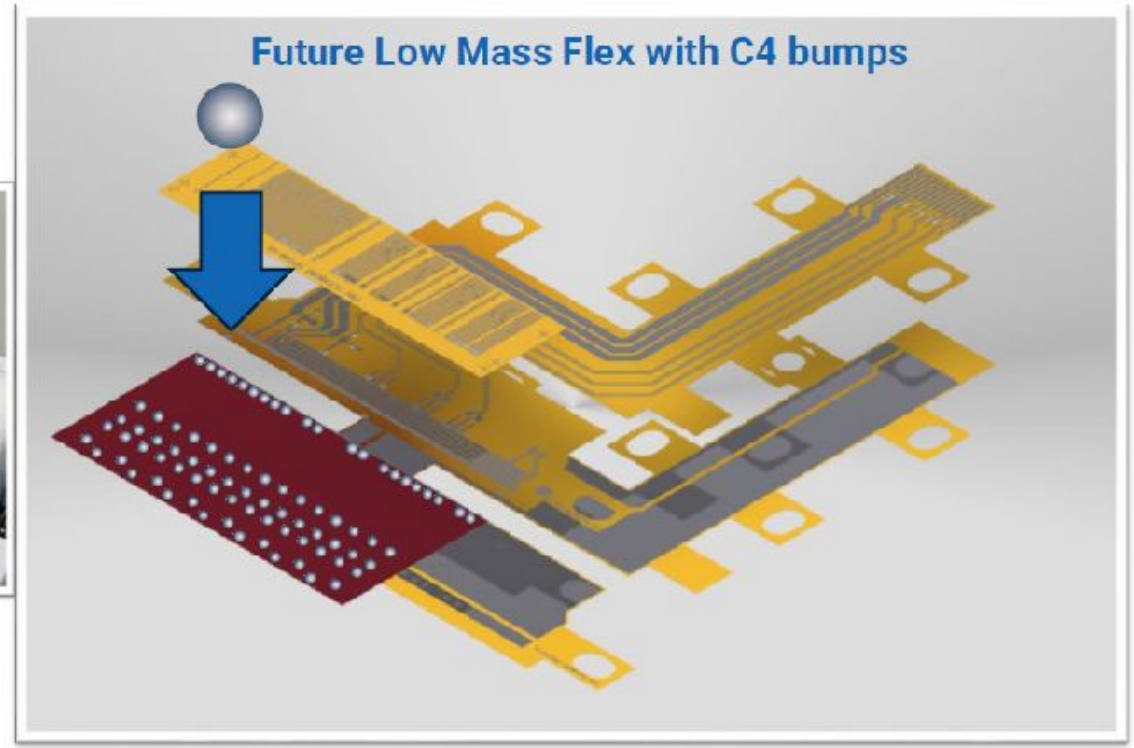


[1] Langøy, R., Mager, M., Nguyen, A. T. T., & Lien, J. A. (2020, September). Thinning and readout during bending of a custom silicon IC. In 2020 IEEE 8th Electronics System-Integration Technology Conference (ESTC) (pp. 1-5). IEEE.

Future Developments
Current Roadmap







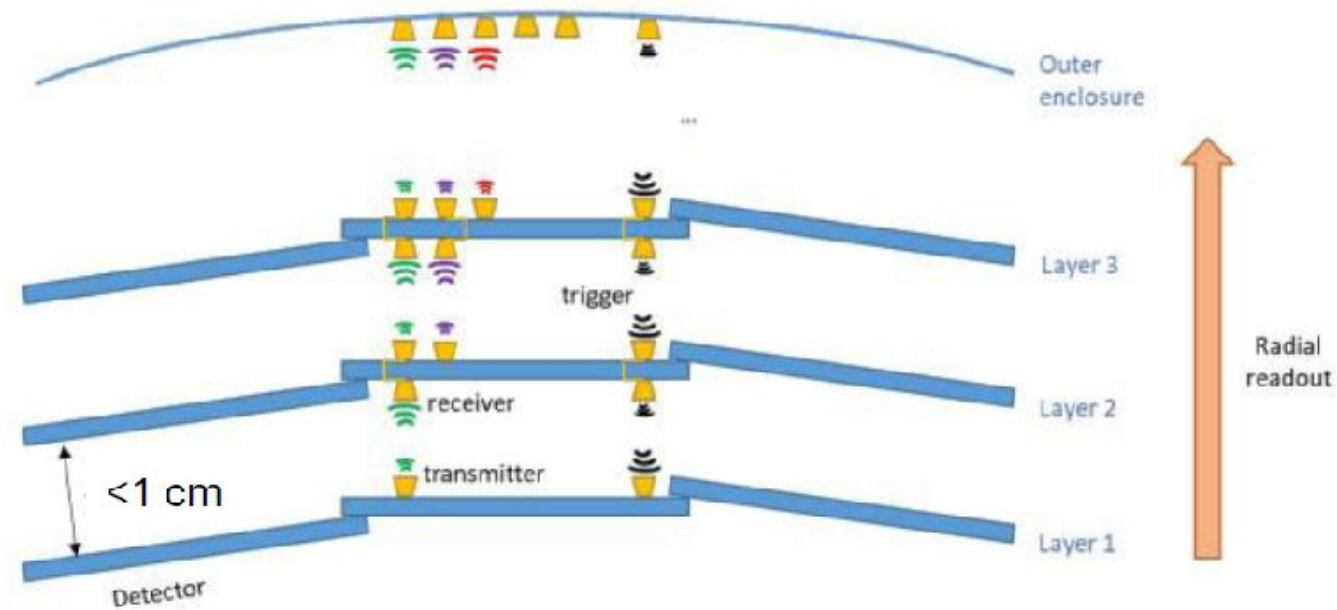
Current Tech Roadmap priorities

- Stacking
- Plating (Ni, ENIG)
- Space qualification
- Low X/X_0 Flip-Chip on Flex
- Signal integrity
- High data rates (few GHz)
- Multi-chip modules

Wireless Communications for FCC-ee

Mainly a summary of the activities of the **WADAPT Collaboration** from the DRD7 Annual workshop presentation and a report of initial tests at UZH

UZH group: Kimia Mirbaghestan, Ben Kilminster, Stefanos Leontsinis, Vagelis Gkougkousis, Armin Ilg, Anna Macchiolo
ZHAW group: Luciano Sarperi, Teddy Loeliger, Marc Kuhn

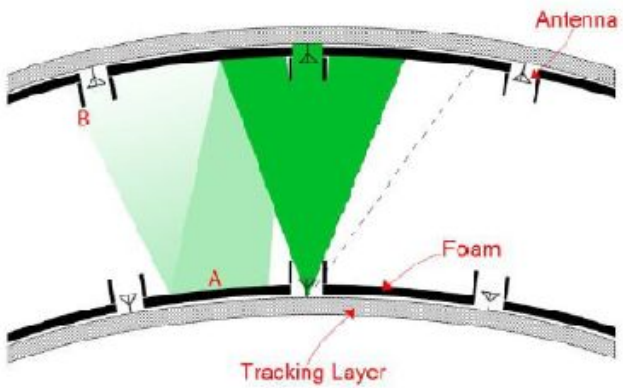


Vertex detector simulation

K. Mirbaghestan, UZH and ZHAW

60 GHz setup with Patch antennas

- Test the new setup with 2 small patch antennas
- Aluminum layer to mimic layers in monolithic sensors
- Added foam to reduce reflections
- Measured the RSSI (Signal Strength)



- Need flexes instead of rigid boards to insert the antennas in the Vertex mock-up

Conclusions and outlook

- **First steps towards a feasibility study**
  - 60 GHz wireless links achieve multi-Gb/s rates over few cm distances
  - compatible with FCC-ee vertex geometry.
- **Crosstalk mitigation:**
  - Orthogonal polarizations and small carrier offsets may effectively isolate adjacent channels within the 60 GHz band.
- **Integration potential**: RF transceivers in 65 nm–28 nm CMOS enable compact, low-power, low-mass data transfer
  - Will it be possible to implement these design feature in the CMOS technology used for MAPs?
- **Next steps:**
  - Extend tests with realistic sensor stack (Al layers + carbon support).
  - Characterize BER stability and timing jitter under varying conditions.
  - Explore TSV-based vertical feedthroughs for signal routing across layers.
  - Estimation of the required power for wireless transmission once embedded in the MAPs
  - Qualify radiation tolerance of RF CMOS front-ends.
  - Full system design and test
- **Goal:**
- Establish feasibility of wireless readout as a viable low-mass interconnect technology for the FCC-ee vertex detector.

Discussion

- The workshop concluded with a discussion session. The notes are posted at https://docs.google.com/document/d/1ulksumSiOGZRIyY9EpyfTOrVTL4iTLWTgo3P353giDA/edit?tab=t.0
- Requirement and Constraints
- Layout and Simulation
  - 1st layer VTX on the beam pipe? Heat, vibrations, inside not favored by accelerator
  - Reconstruction software for integrated study of vertex+gaseous tracker + silicon wrapper around the corner
    - Need to develop this centrally, together
    - Compare VXD layouts in full simulation e.g. also in terms of jet flavour tagging
  - Final uncertainty on physics observable to actually compare layouts
  - Need PhD students to contribute to high-level reconstruction and case studies
  - $B^0 \longrightarrow K^{*0} \tau^+\tau^-$, strange Yukawa, …?
  - Integrated optimization of inner vertex + beam pipe (maybe it's overall better to be at larger radius but have a lower-X_0 beam pipe instead?)
  - Issues around larger B field, wrapper layer

Discussion continued

- Sensors
- Inner vertex
  - achieving 3-5 micron resolution
  - 100 MHz/cm^2
  - time resolution actually needed inner layers vs power budget?
  - dead space from stitching
- Outer vertex
  - timing layer here considering higher B field etc
  - could pixelated LGADs be an integrated solution?
- Impact of (unknown?) foundry schedules
- 3D is it a real possibility? FCCee time frame, cost? value added?

continued

- **Mechanical**
- beam pipe mock-up: carbon fiber outer shell could be very interesting
- beam pipe mock-up: vibrational studies
- beam pipe mock-up: how to connect the inner Vertex
- beam pipe mock-up: how to connect properly support the lumical and stability measurements
- beam pipe mock-up: installation sequence
- service integration: again vibration studies, interplay between relatively heavy and rigid services with very light mechanical structure and air flow
- service integration: sequence of installation and service connection
- curved sensors: more experience is needed also from other institutes
- curved sensors: study different support structures and installation sequence
- air cooling: vibration and stability studies, different types of fluids (air, nitrogen, helium), temperature of the air etc.

continued

- **Systems and Readout**
- Al tapes attractive for mass but a niche technology
- 20-25 year time frame, vendor stability? In-house?
- Serial systems shown were small scale, need to “get serious” about engineering a large scale system
- Serial protection, bypass, monitoring, low noise operation, etc
- Are there radiation issues for wireless systems?

Opportunities or strategy points

- Layout and simulation - already starting up
- MAPS effort to ramp up
- 3D?
- wafer bending technology, develop US experience here
- Fast timing, a US area of expertise
  - Inner timing layer?
  - role of LGADs in outer vertex
- Large serial demonstrators, system design, protection etc
- Advanced packaging
- Mechanical prototyping