

**CAEN @ Annual APP and HEPP Conference 2026**

# **Benchmarking SRO Performance of CAEN Digitizers**

*Impact of Protocol and Data Processing Techniques*

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# Outline

## Key points we will cover

- **Product Overview**

Introduction to the CAEN digitizer family.

- **Latest Developments**

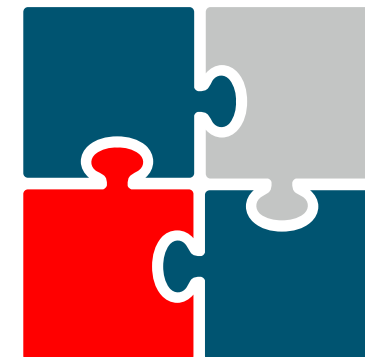
Highlights of new firmware updates and advancements introduced this year.

- **Hardware Benchmarks**

Performance testing of the acquisition system with a focus on data transport limits and network optimization strategies.

- **Software Benchmarks**

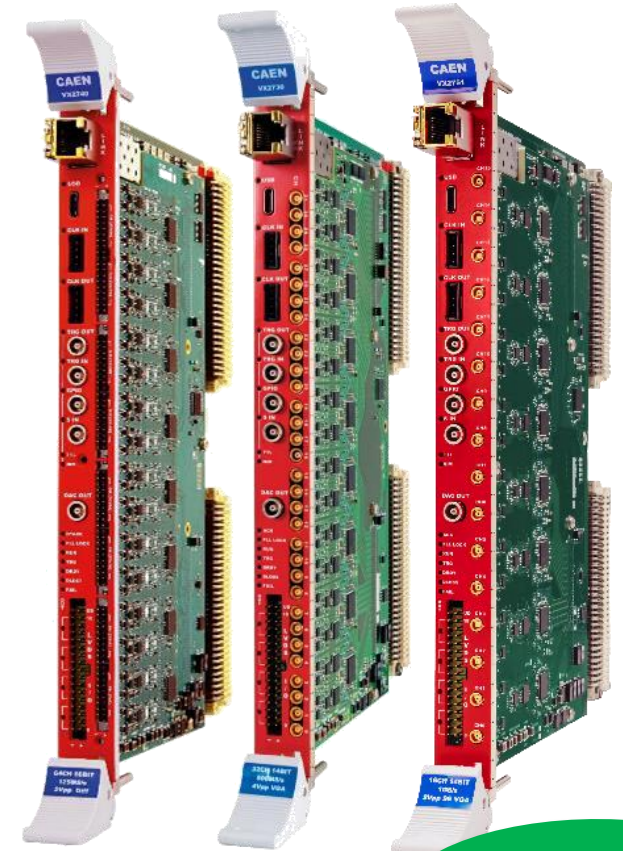
Analysis of software-side performance, processing bottlenecks, and solutions for efficient data decoding and handling.



# Digitizer 2.0

## Many flavors — VME & Desktop

	2740/2745	2730	2751
Channels	64/8	32/8	16/4
Sampling	125 MS/s @ 16 bit	500 MS/s @ 14 bit	1 GS/s @ 14 bit
Variable Gain Amplifier	x100 (2745 only)	x20	x10
Max record length	84 ms per channel		
Communication Interfaces	<ul style="list-style-type: none"> <li>• USB 3.0</li> <li>• 1 GbE TCP</li> <li>• 10 GbE UDP</li> </ul>		

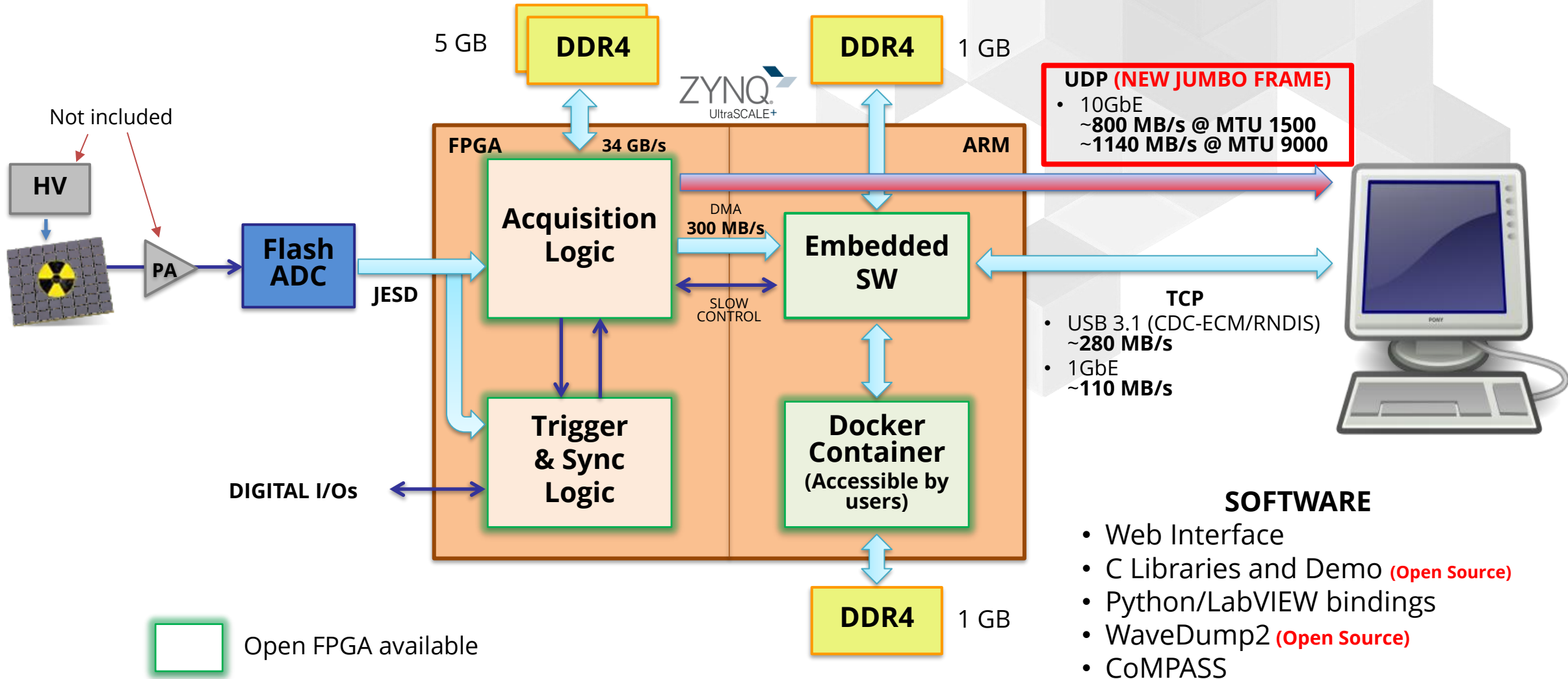


New compact desktop version coming soon.



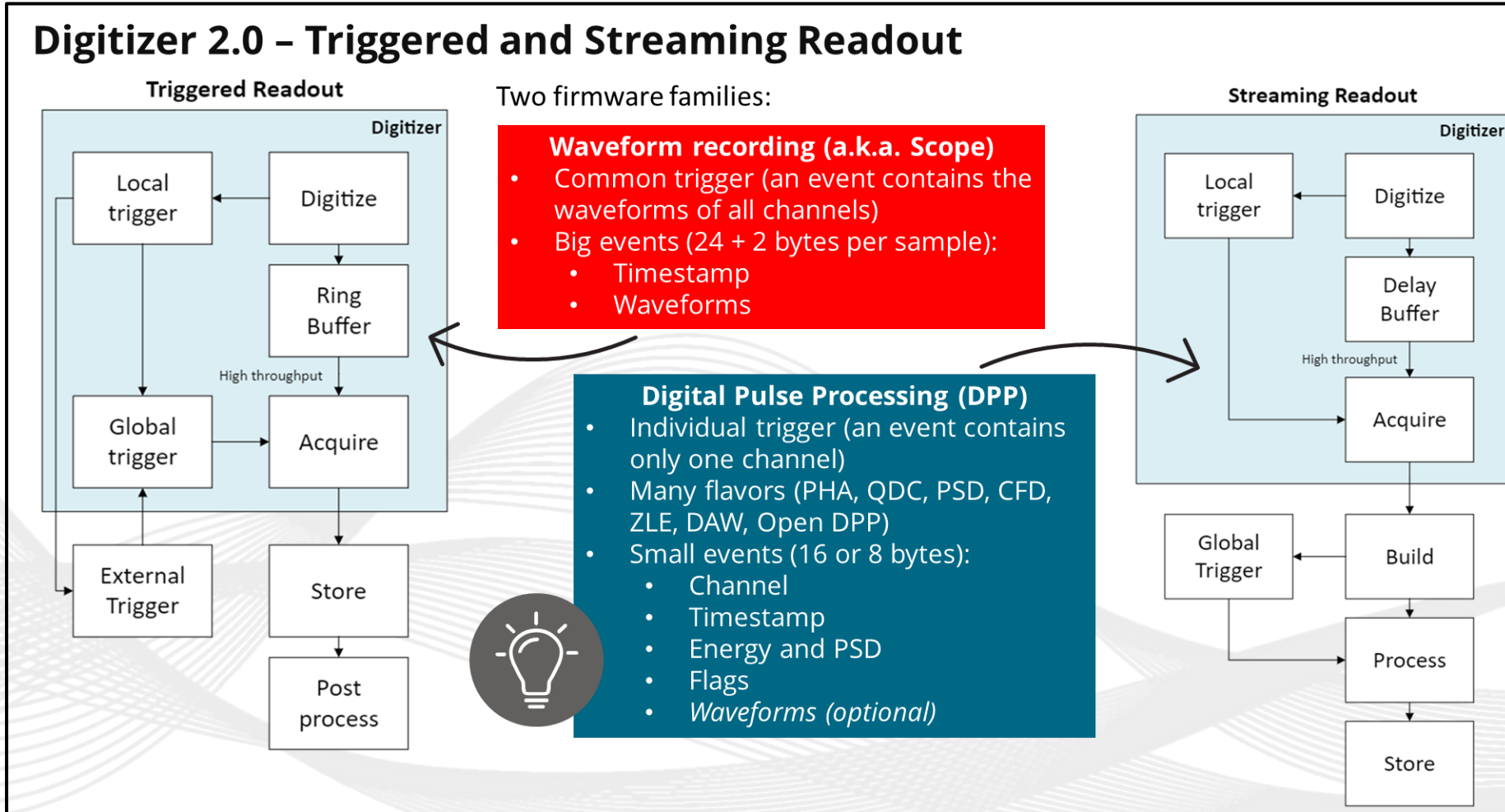
# The Challenge

## From Gbit to 10Gbit: Architecture of a Streaming Readout Setup



# Context

## Readout Paradigms: Triggered vs Streaming



# The Role of Jumbo Frames

## Impact on 10 GbE Streaming

### The Standard MTU (1500 B), default for all devices in all network

- To maximize throughput and minimize interrupts, the application must process large UDP datagrams (up to ~64 kB).
- On standard MTU (1500 B), sending datagrams larger than the MTU requires IP fragmentation.

### But fragmentation is dangerous

- Reassembling fragments is CPU-intensive for the OS.
- If a single fragment is lost in the network, the OS drops the entire UDP datagram.
- In high-throughput UDP streams, this amplifies data loss significantly.

### The Jumbo Frame Solution (9000 B)

- Allows sending ~9 kB payloads in a single, unfragmented frame.
- Balances datagram size to keep application wake-ups at a reasonable rate, drastically lowering OS workload.
- Fully compatible with modern 10GbE network infrastructure.

Jumbo Frames are not just about bandwidth: they are about CPU efficiency and link reliability.

# Methodology

## Measuring readout throughput on two possible scenarios

In the next slides, we present results acquired with both the following experimental setups, using a minimal demo software based on the **CAEN FELib**, the official C library to interact with digitizer:

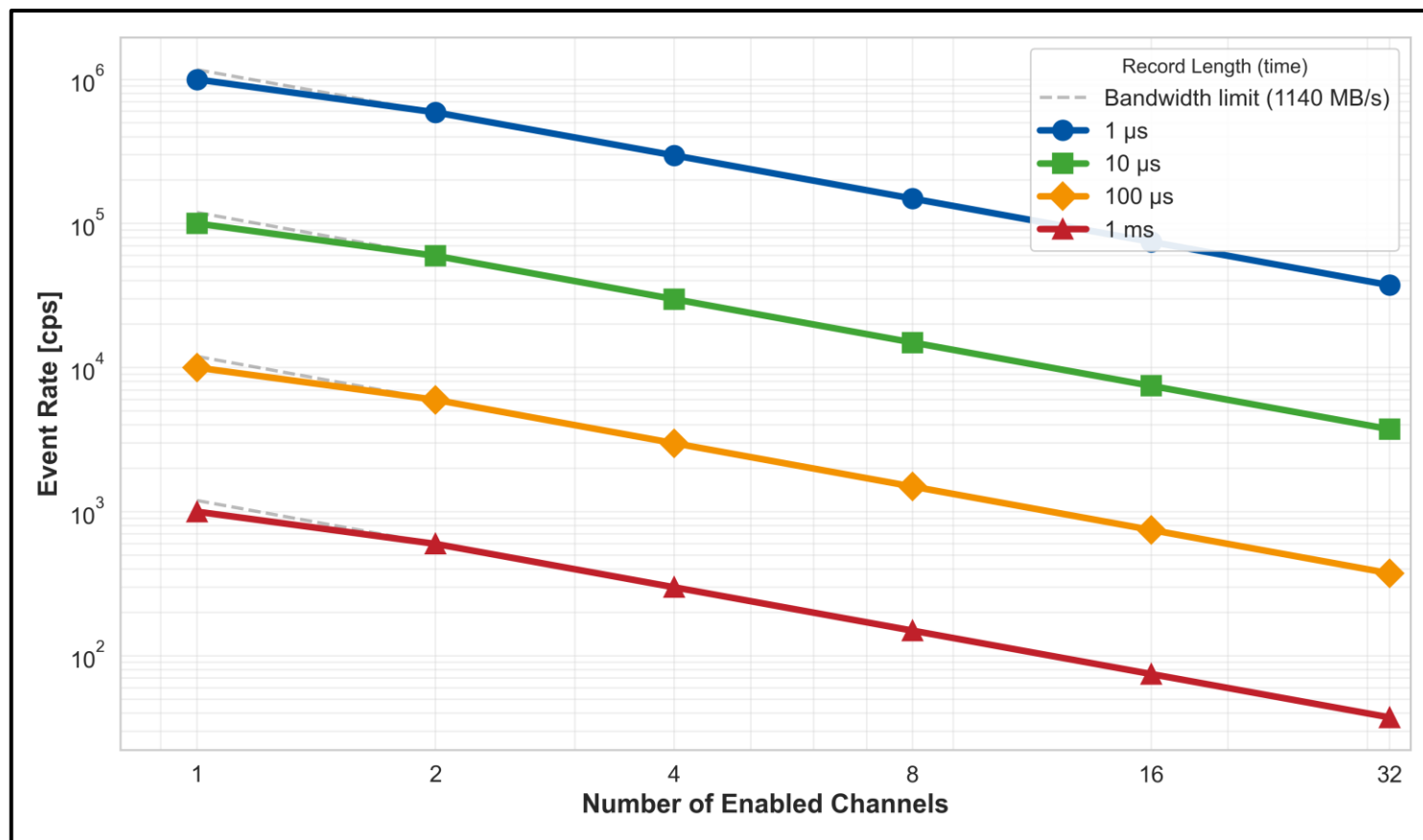
	<b>Setup #1</b> <i>Triggered Readout</i>	<b>Setup #2</b> <i>Streaming Readout</i>
CAEN Digitizers	1 x VX2730 (Triggered Readout)	1 x VX2730 (Streaming Readout)
Readout Mode	Triggered (Scope firmware)	Streaming (DPP PSD firmware)
RAM	32 GB	32 GB
Network interface	Intel XL710-BM1 (4 SFP+ link)	Intel XL710-BM1 (4 SFP+ link)
OS	Ubuntu 24.04	



```
# Increase OS receive buffer
sysctl -w net.core.rmem_max=2000000000
sysctl -w net.core.rmem_default=2000000000
# Increase OS queue size
sysctl -w net.core.netdev_max_backlog=65536
# Maximize NIC receive ring buffer
ethtool -G <interface name> rx 4096
# Enable OS Jumbo frame support
ip link set eth1 <interface name> 9000
```

# Triggered Readout: Results

## Saturation Analysis (Raw Waveform recording, external trigger)



Experimental setup:

- Scope 10GbE UDP firmware
- $24+2*N\_CH*N\_SAMPLES$  bytes/event

Measured data throughput:

- Board: **~1140 MB/s**

Additional consideration:

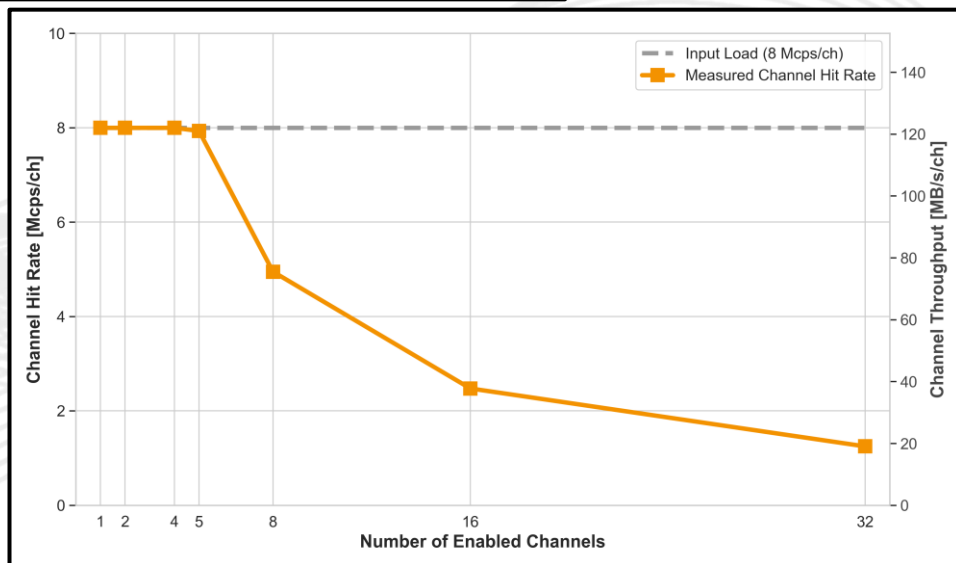
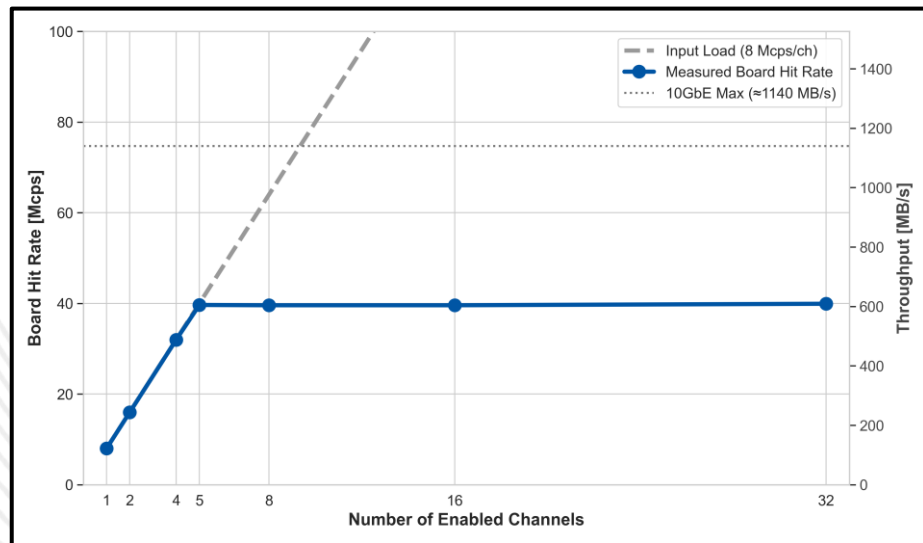
- Possibility to stream 1 ch @ 500 Msps
- Limited by UDP throughput
- No UDP data losses detected

How to further increase event rate:

- Reduce record length
- Decimation
- Move to DPP streaming readout, with onboard data processing

# Streaming Readout: Results

## Saturation Analysis (List Mode, self-triggered)



Experimental setup:

- DPP-PSD 10GbE UDP firmware (streaming readout)
- 16 bytes/hit (channel, timestamp, energy and PSD, flags)
- External trigger @ 8 MHz

Measured throughput:

- Channel: **8 Mcps/ch**
- Board: **~40 Mcps**

Additional consideration:

- Single channel throughput **up to ~8 Mcps/ch**, but board still limited at **~40 Mcps**
- Not limited by 10GbE UDP bandwidth
- Rate limited by event sorting algorithm within the FPGA
- No UDP data losses detected

# Readout Software

## The online decoding bottleneck of CAEN FELib

Depending on acquisition configuration, `CAEN_FELib_ReadData` may return:

- **Raw data:**
  - Binary blob directly from FPGA, to be processed online or offline with custom algorithms  
→ no bottleneck
- **Decoded data** (asynchronously decoded in a library thread, buffered internally):
  - **Triggered readout:** Single event per trigger (timestamp + all waveforms)  
→ no bottleneck, tested up to 1 Mcps
  - **Streaming readout:** Single hit per event (timestamp, energy, PSD, flags, optional waveform)  
→ bottleneck at 5.6 Mcps (~85 MB/s with 16-bytes hits)

Possible improvements:

- Implementing batch processing on Raw data (multiple hits per API call) to reduce context switch overhead
- Adopting a multi-threaded producer-consumer architecture for parallel event processing
- Using a CPU with higher single-thread performance (e.g., higher clock frequency)



# Readout Software

## An overview on CoMPASS performances

CAEN also provides CoMPASS, a multiparametric DAQ software for multi-board streaming acquisitions.

CoMPASS is built on top of CAEN FELib and is significantly more complex than raw readout, as it handles advanced features including:

- Multi-board event synchronization and ordering
- Hardware coincidence detection across boards
- Software-level event filtering and cuts
- Real-time data visualization and monitoring

Due to this additional processing overhead, CoMPASS exhibits a software-level bottleneck limiting throughput to approximately **~1 Mcps per setup**.



# CoMPASS



# Summary

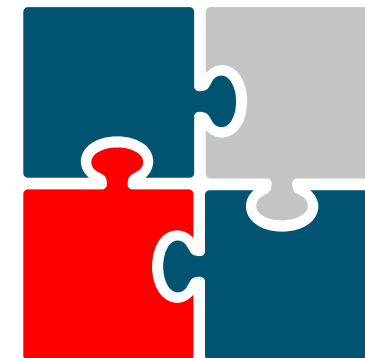
## Conclusions and possible future developments

### Jumbo Frame Support

Added support for MTU 9000 bytes, reducing per-packet overhead and improving 10 GbE readout efficiency.

### Throughput Analysis

Characterized performance across triggered and streaming readout firmwares, identifying bottlenecks and opportunities for further optimization.



	Max board Rate	Throughput	Bottleneck
Triggered Readout Scope, decode ON	Depends on record length	~1140 MB/s	10GbE UDP (physical layer)
Streaming Readout DPP, decode OFF	40 Mcps	~600 MB/s	Firmware (event sorting algorithm)
Streaming Readout DPP, decode ON	5.6 Mcps	~85 MB/s	Software (context switches)
CoMPASS	~1 Mcps	~15 MB/s	Software (complex data processing)

# Thank you

# Backup Slides

# Streaming Readout: Results with waveforms

## List Mode + Waveforms Saturation Analysis

We assumed 16 bytes per hit in previous slides, but the size could be optionally increased with additional information:

- Waveforms
  - 1 8-bytes header word, followed by up to 4095 8-bytes waveform words
  - Available both in official CAEN DPP firmware and Open FPGA
- User words:
  - 8 bytes per word
  - Open FPGA only

This increase a lot the size of a hit. For example, a hit with 1024 16-bit samples takes 2072 bytes.

In these conditions, the board hit throughput is drastically reduced because it is dominated by the **1140 MB/s** 10GbE UDP bandwidth and depends on the acquisition configuration.