# RadPix

## A High-Voltage CMOS Sensor for the LHCb Upgrade

**Karol Hennessy**
on behalf of the Mighty Tracker and RadPix collaborations

2026-04-09

UNIVERSITY OF LIVERPOOL

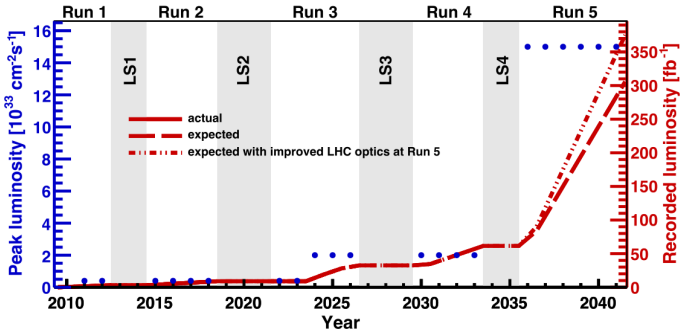
LHCb

# LHCb Upgrade II

- Physics programme limited by detector, NOT by LHC

⇒ upgrade to get the maximum physics LHC can deliver

- **Full motivation for LHCb physics programme in Harry's talk after the break, and Silvia's upgrade talk tomorrow**

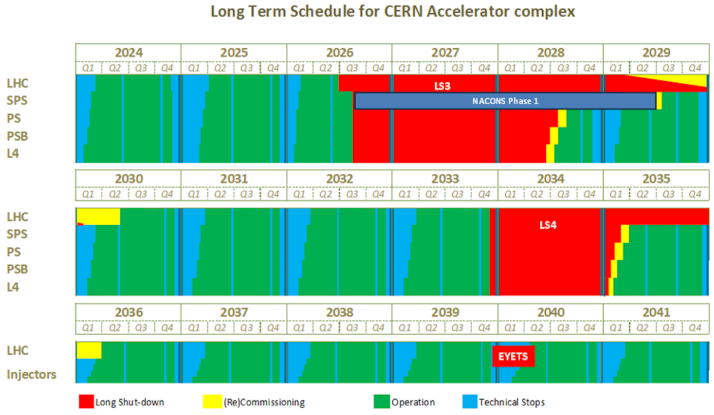



## Upgrade I

- $L_{peak} = 2 \times 10^{33} cm^{-2} s^{-1}$

## Upgrade II

- $L_{peak} = 1.5 \times 10^{34} cm^{-2} s^{-1}$
- $L_{int} = 300 fb^{-1}$ during Runs 5 & 6. Installation in LS4



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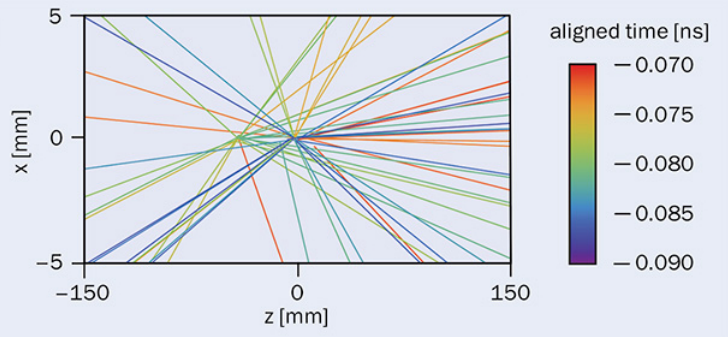
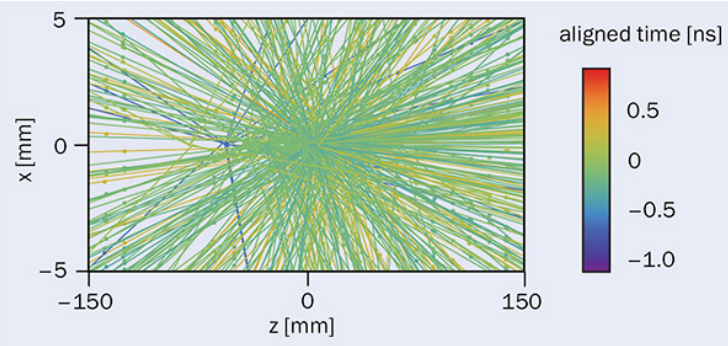
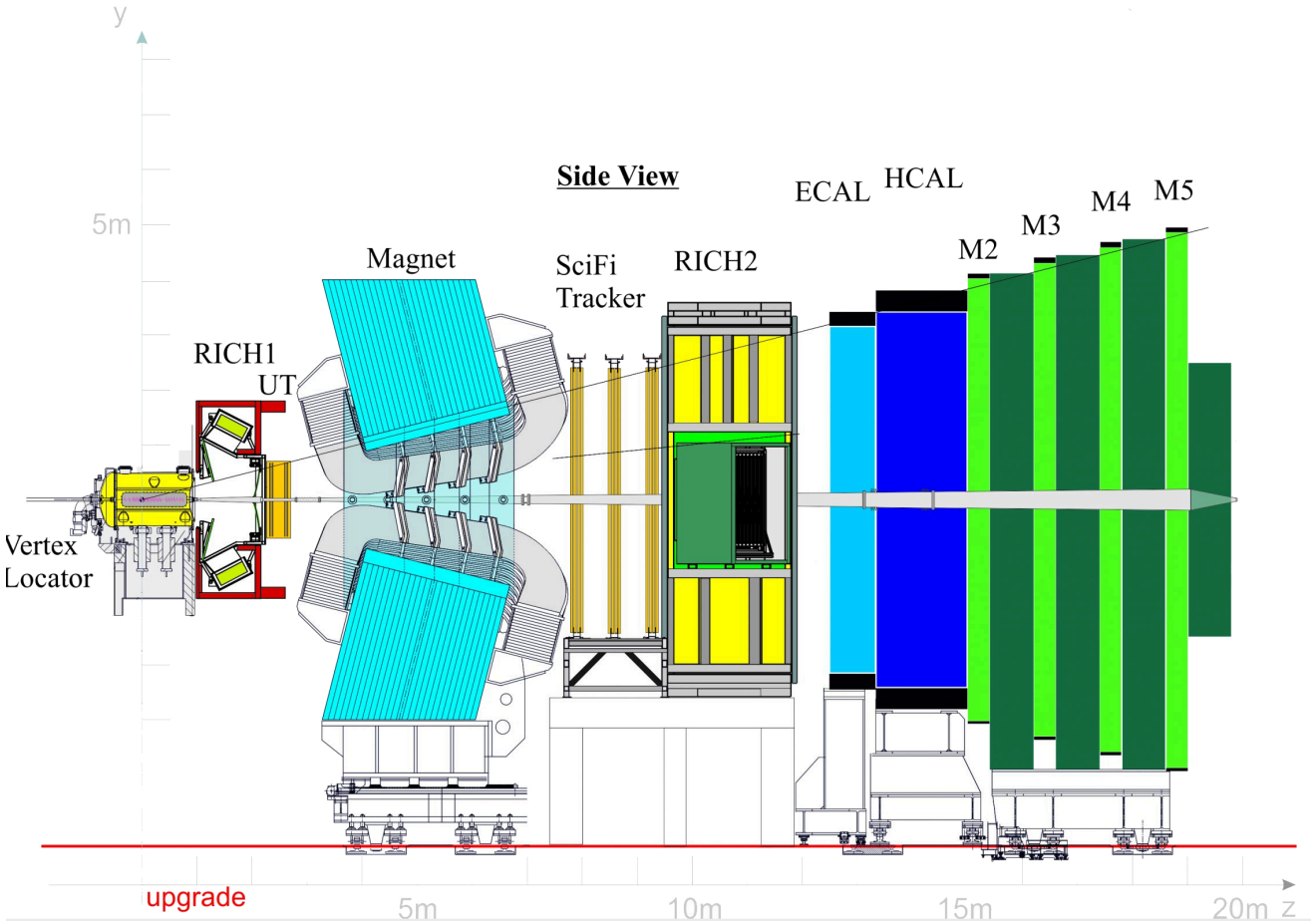
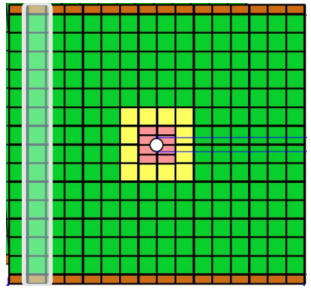



Tracks at Upgrade 2 luminosities:

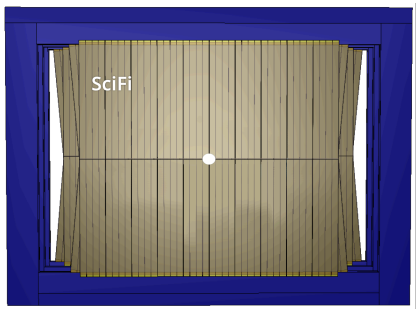


# LHCb Upgrade I - today



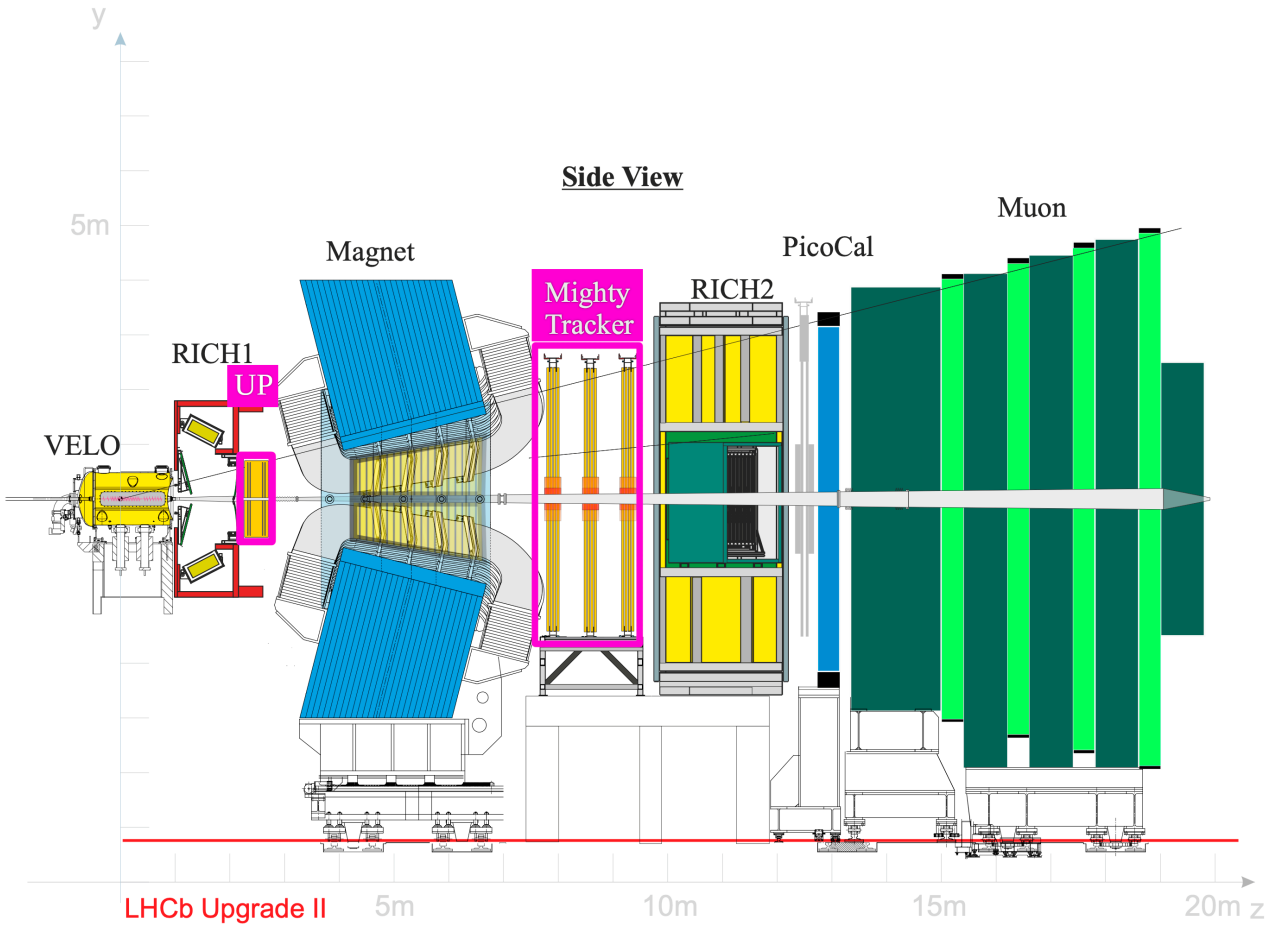



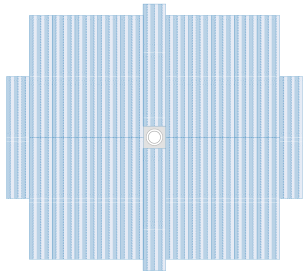
UT - Si strips



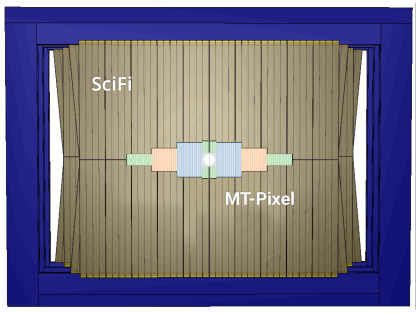

Sci-fi - Scintillating Fibres

# LHCb Upgrade II



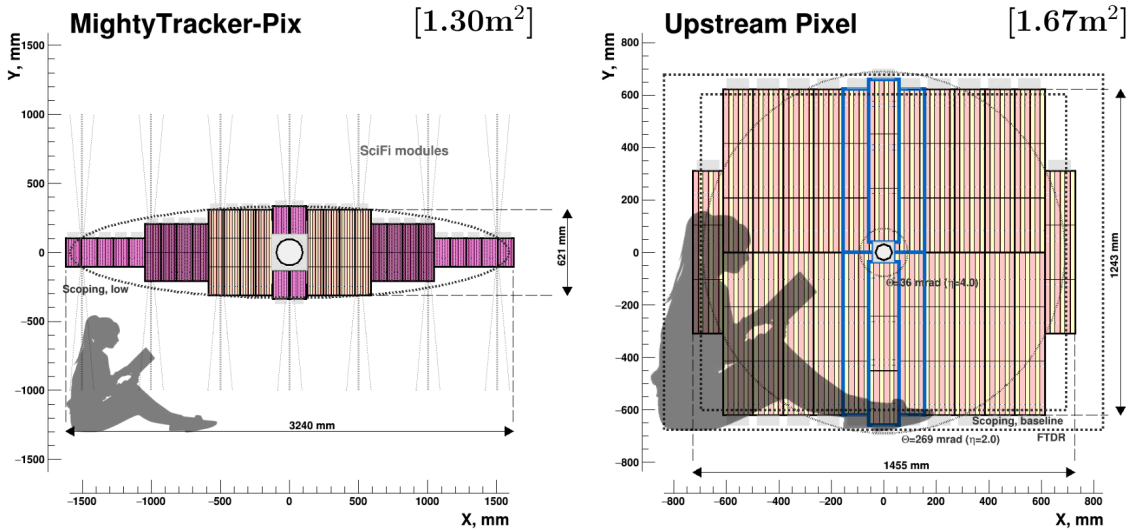



UP - **Pixels**




Mighty Tracker - Scifi + **Pixels**

# Mighty Tracker (MT) & Upstream Pixel (UP) Detectors




- Both **pixel** detectors with similar needs
- Hit efficiency > 96%
- Low power, high radiation tolerance

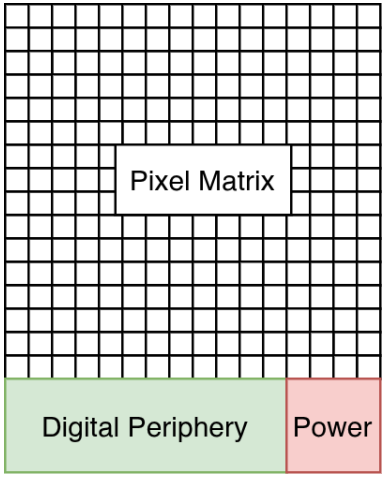
| Parameter | MP specification | UP specification |
|---|---|---|
| Pixel size (x) | $\leq 100\,\mu$m | $\leq 100\,\mu$m |
| Substrate thickness | $100 - 200\,\mu$m | $100 - 200\,\mu$m |
| Max. Particle Rate | $37.6\,\mathrm{MHz/cm^2}$ | $80\,\mathrm{MHz/cm^2}$ |
| Max. Hit Rate | $18.8\,\mathrm{MHz/cm^2}$ | $45.6\,\mathrm{MHz/cm^2}$ |
| In-time efficiency | $> 99\%$ within 25 ns | $> 99\%$ within 25 ns |
| NIEL | $2.4 \times 10^{14}\,n_{\mathrm{eq}}/\mathrm{cm^2}$ | $3 \times 10^{15}\,n_{\mathrm{eq}}/\mathrm{cm^2}$ |
| TID | 24 MRad | 187.5 MRad |
| Power consumption | $\leq 150\,\mathrm{mW/cm^2} + 30\%$ overhead for serial powering | $\leq 200\,\mathrm{mW/cm^2} + 25\%$ overhead for serial powering |

Safety factor of 2 applied
Safety factor of 3 applied

# Let's make a chip!

It needs to be :

- Radiation Hard
- Low Mass
- High Data Rate
- Low power consumption
- Low Cost



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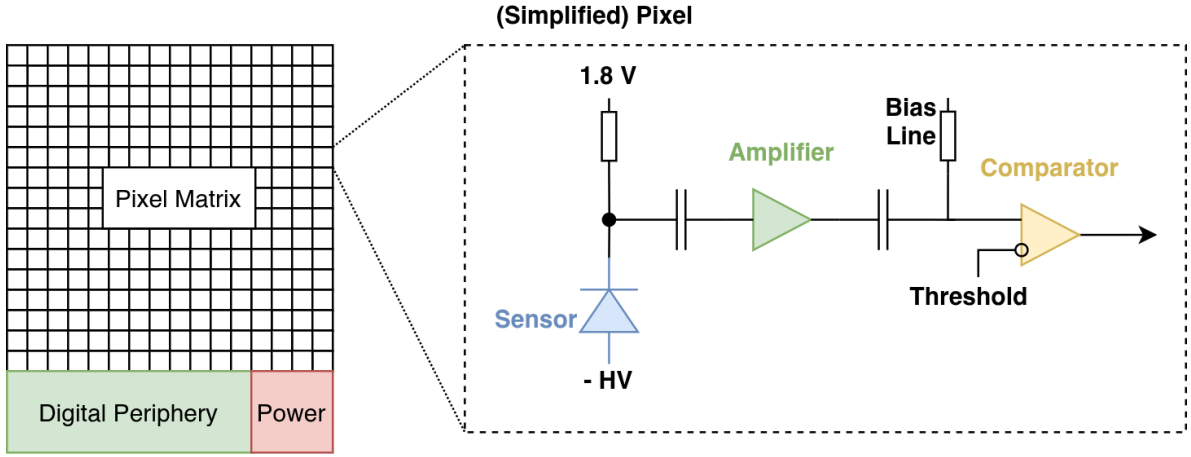

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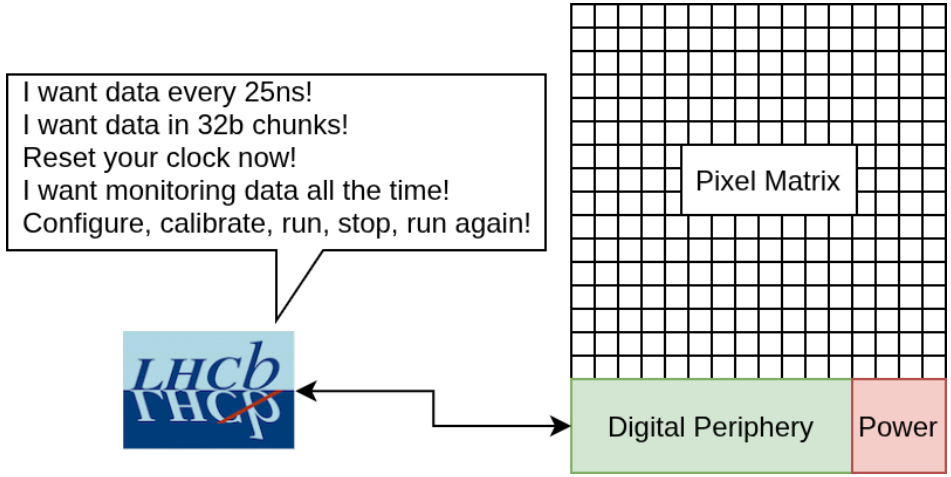
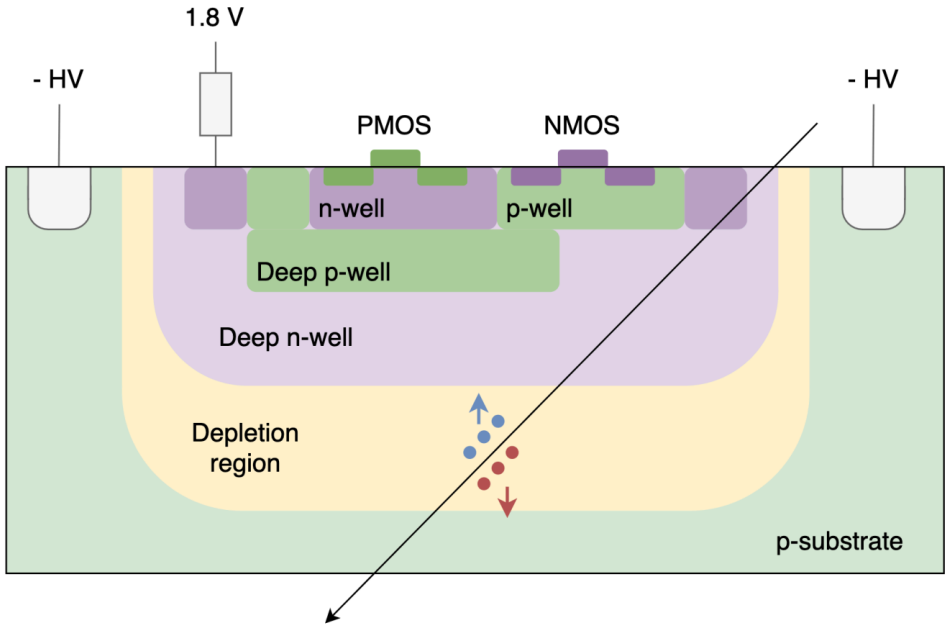


# HV-CMOS

- Good candidate solution
- Sensor and readout chip in one



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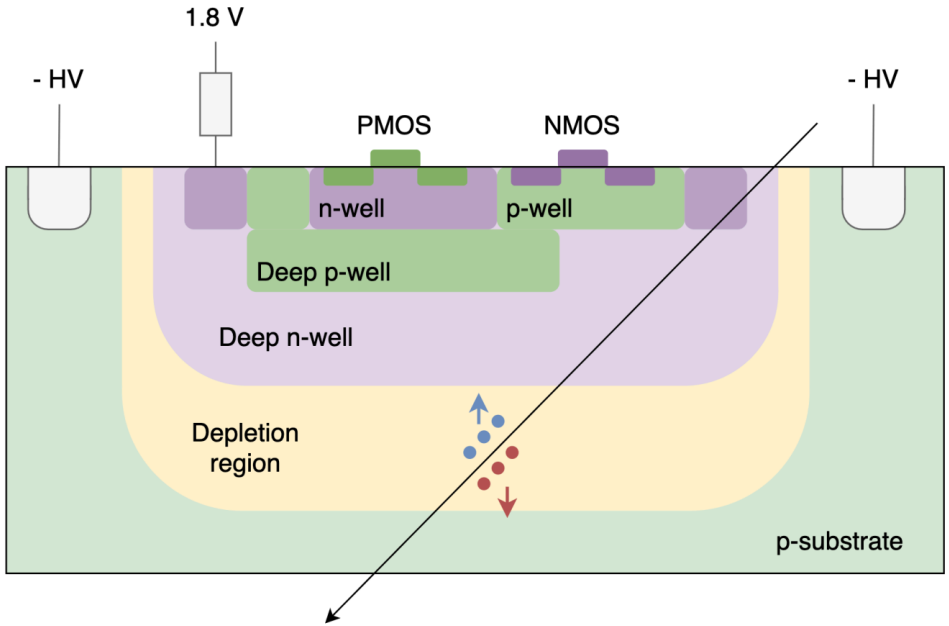


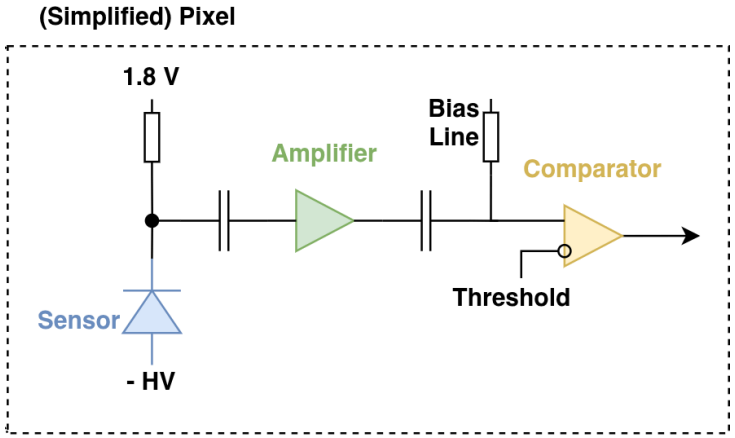

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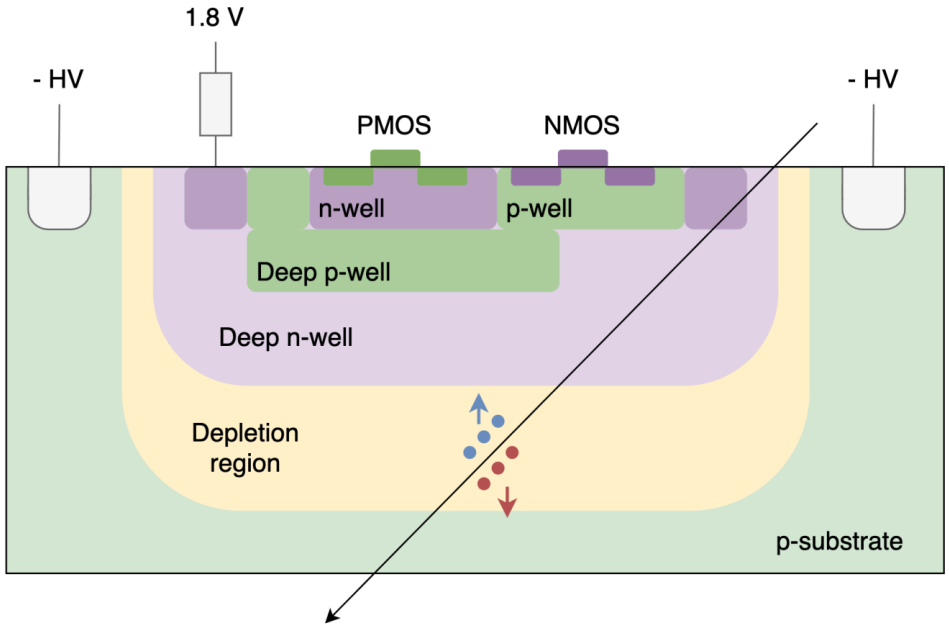
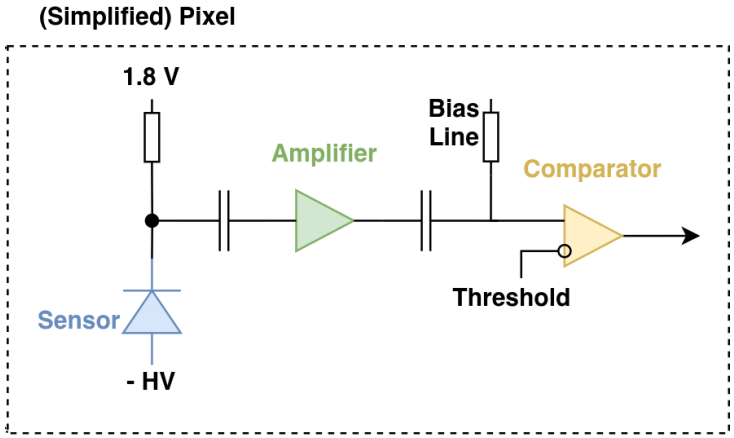
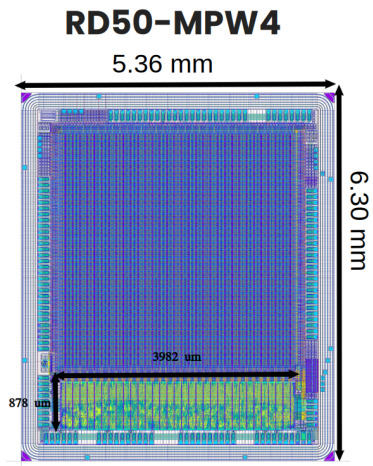



RD50 collaboration studies

*"Radiation hard semiconductor devices for very high luminosity colliders"*





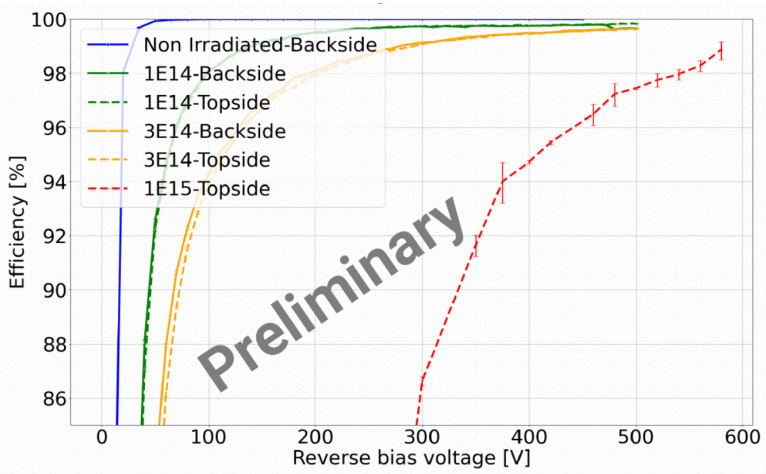

- 62 µm x 62 µm pixels
- 64 x 64 pixels matrix
- In-pixel low-noise
- Backside HV biasing
- VBreakdown > 600 V
- small leakage current

## Unirradiated

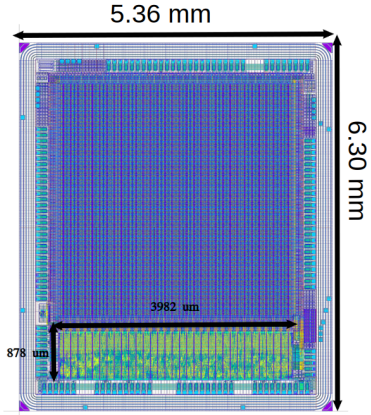
- Efficiency measurements show full efficiencies > 99% up to thresholds of 200mV (HV = 190 V)

## Irradiated

- Test-beam for irradiated sensors and increase of Vbias
- 99% efficiency up to $1 \times 10^{15} n_{eq} \cdot cm^{-2}$ @ HV = 580 V, T = −20°C



**RD50-MPW4**

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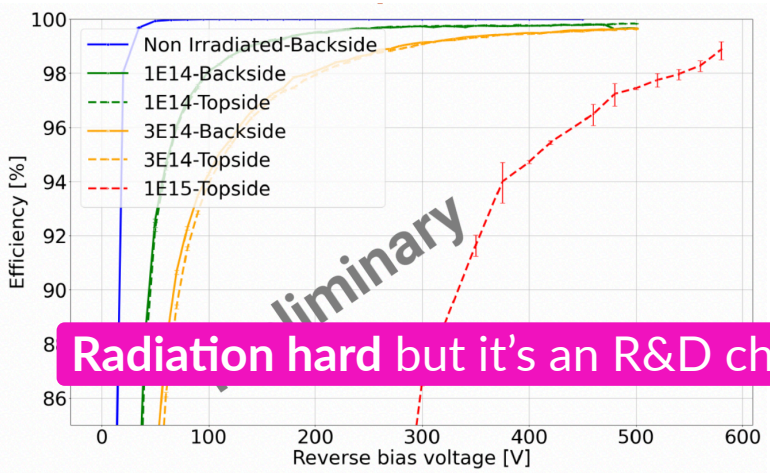
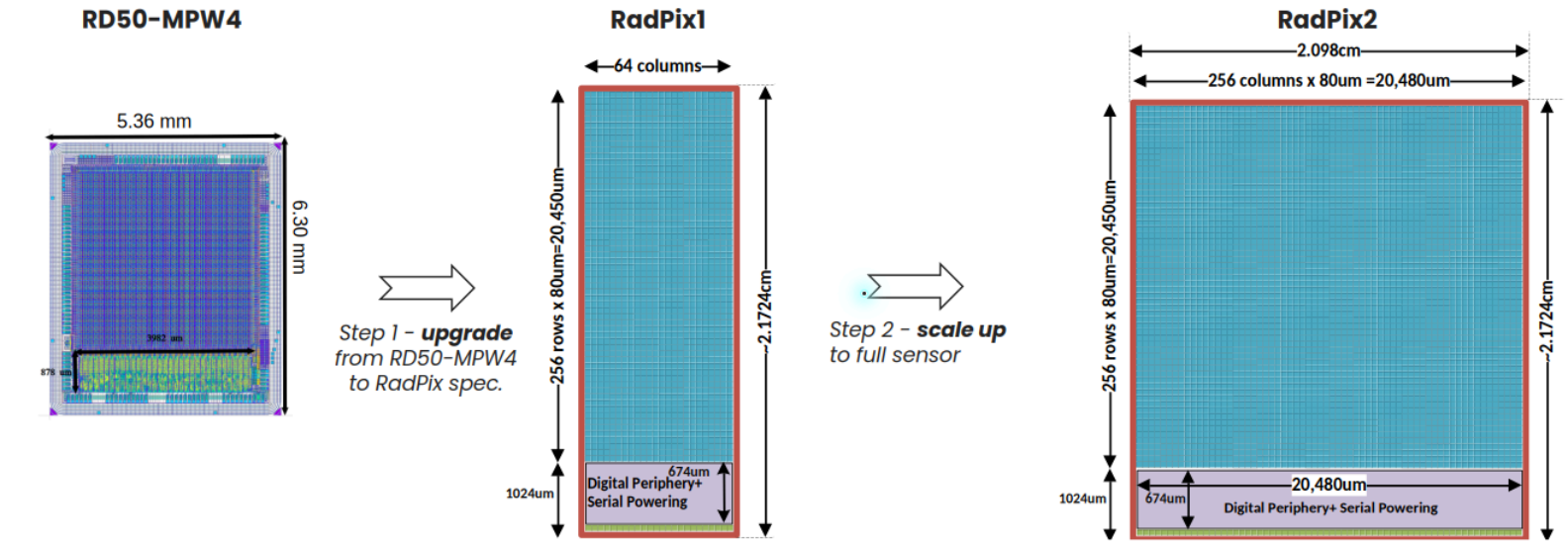


# RadPix

- Let's scale it up and make a proper readout




- Prototype : 64 × 64 pix.
  - 62 x 62 µm²
- Tested, **meet RD50 requirements**

- ¼ of the final size : 256 x 64 pix.
  - 80 x 80 µm²
- Submission Q2 2026

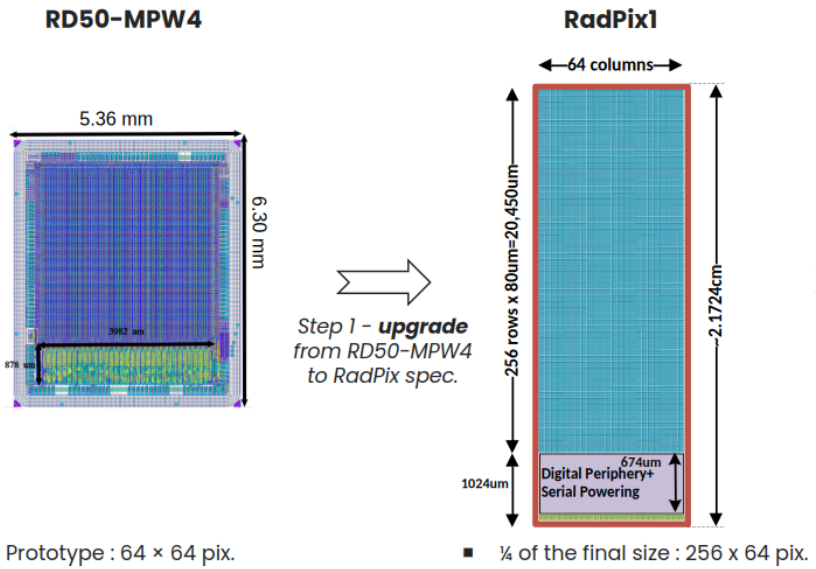
- Full size : 256 x 256 pix.
  - 80 x 80 µm²
- Submission 2027

- **UK driven development!** (Liverpool, RAL, Cambridge, Glasgow, Paris-Saclay, Barcelona )

# Main objectives for RadPix1

## A more LHCb compatible chip

- **Power density**: Power (150 mW/cm2), while keeping 99% in-time efficiency within 25ns.
- 95% sensitive area: Careful floor planning
- **Upgrade digital periphery**:
  - LHCb communication protocols.
  - sensible approach reduce power consumption




- **Porting and developing necessary IPs**: Serial powering, LVDS drivers and receivers, Power-on-Reset.

# Top Level Diagram - sensor design

## WP1 - Pixel Matrix

- Optimisation of the Pixel array size and power consumption.

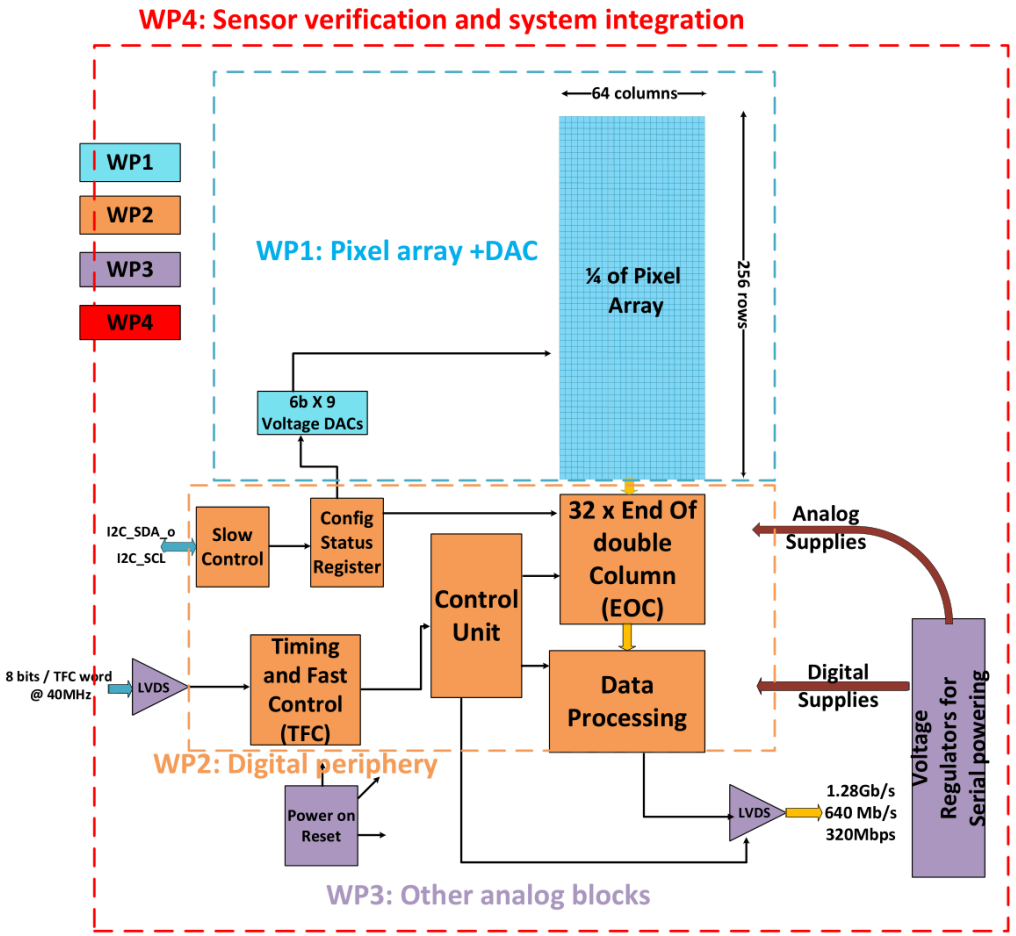
## WP2 - Readout Periphery

- RTL description of the digital readout periphery + Place&Route

## WP3 - Analog blocks

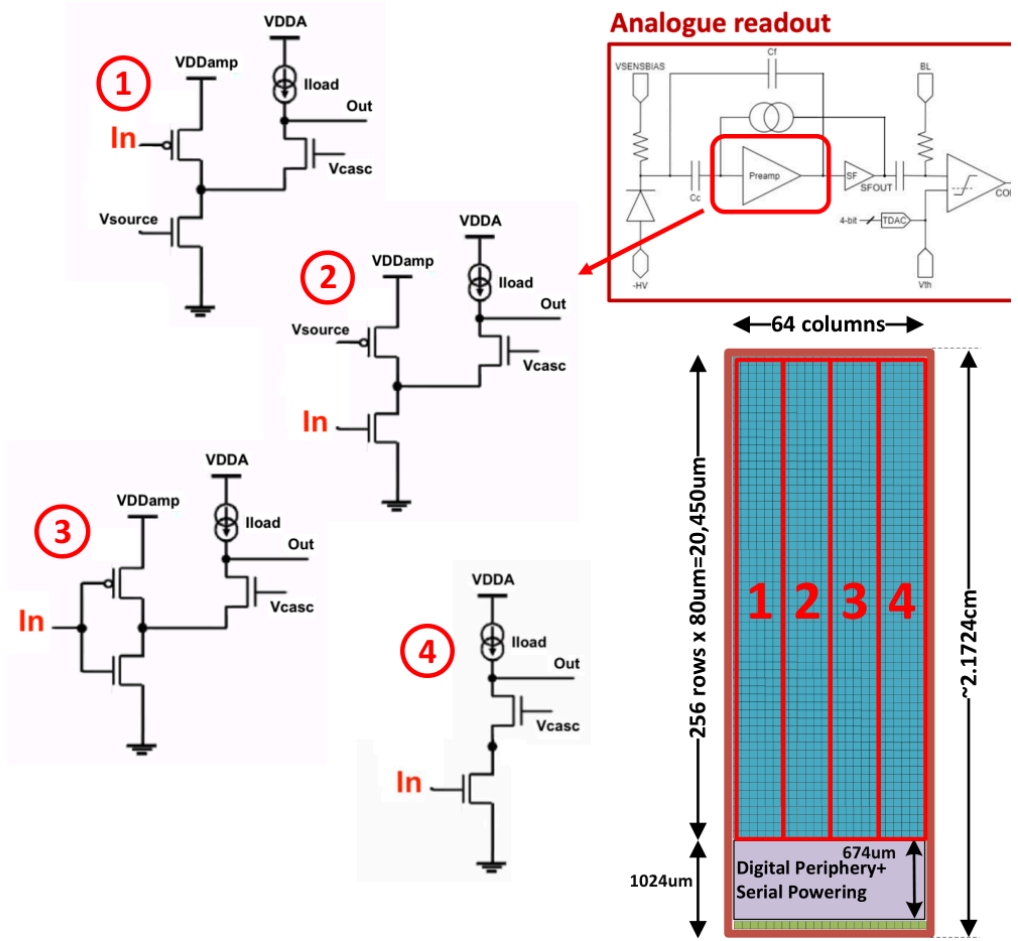
- Design of Shunt LDOs for serial powering.
- LVDS drivers and receivers
- Power On Reset

## WP4 - System verification and integration



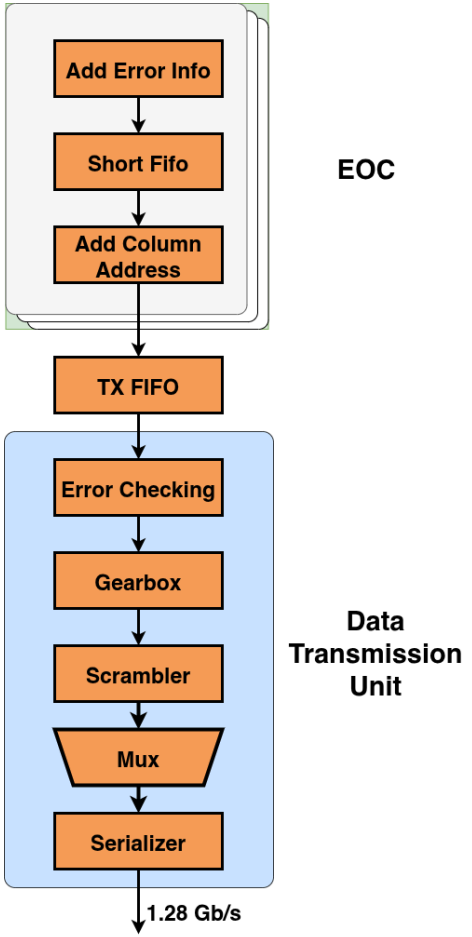
# 1. Pixel Matrix

- **Pixel** = $80\mu m \times 80\mu m$
- **Analog**: Charge Sensitive Amplifier (CSA) - 4 flavours
  1. PMOS (based on RD50-MPW4)
  2. NMOS (based on Monopix)
  3. CMOS (based on Monopix)
  4. Trans-impedance amplifier
- All optimised for **99% in-time efficiency and $150mW \cdot cm^{-2}$ power**
- Simulation shows *rise-time*: 11-14ns, *time-walk*: $1.5ke^- - 15ke^-$
- **Digital** (not shown): adds timing and address info



# 2. Digital Periphery

- **End-of-Column (EOC) logic**
  - add error info
  - buffer
  - add column address info
  - driven by a state machine
- **Data transmission unit**
  - prepare data for transmission in 32b chunks
  - scramble data for DC balancing
  - add header
  - serialise and send out: up to 1.28 Gb/s
- Verification: unit and system tests



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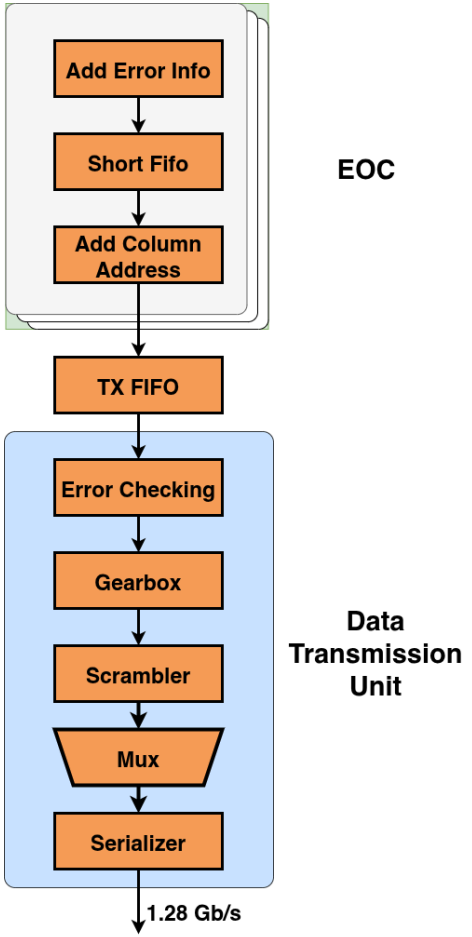
- **High data rate?** - RadPix1 data transmission is designed for fidelity first. Once we know we have good data from the matrix, we will optimise the data formats.



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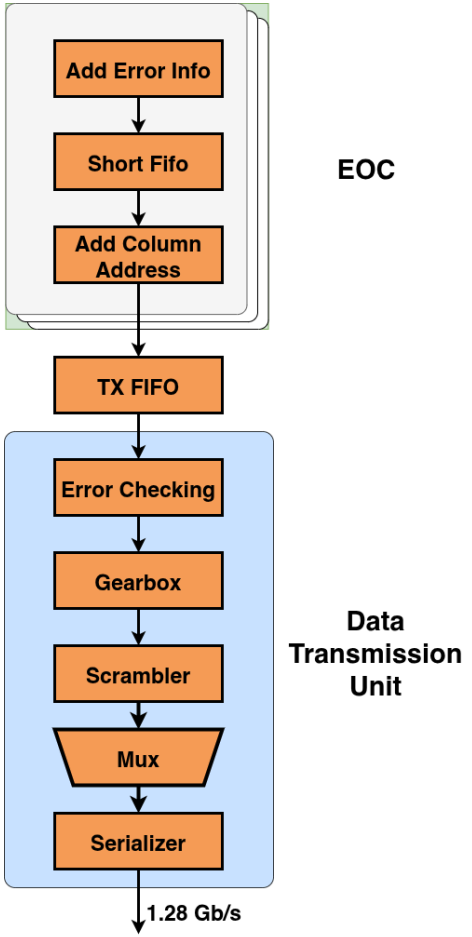
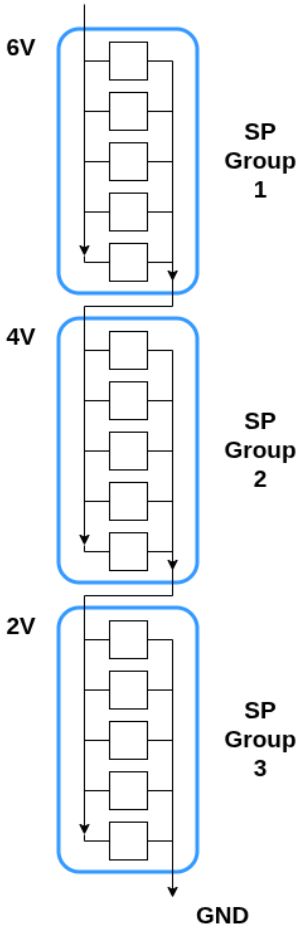
- **LHCb compatible?**
  - Slow Controls will be I2C for first version (too slow for final system)
  - TFC (Timing and Fast Control) are shared with other systems (well tested)



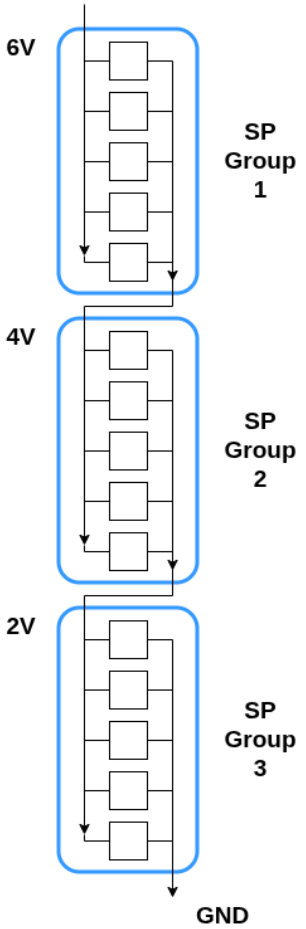
# 3. Serial Powering

- For reasons of space, power, and material budget, serial powering was chosen as preferred option for Mighty Tracker
- Shunt Low Drop Out (**SLDO**) Voltage regulator design
  - Shunt regulator - regulates current to the chip
  - LDO regulator - generates the voltage
- Simulated failure conditions: over-voltage, over-current, short-circuit
- For RadPix1, the serial powering will be a separate ASIC wire-bonded to the main pixel chip



# 3. Serial Powering

- **Implications**
  - Each chip sits on a different ground
  - Data must be A/C coupled
  - Can cope with up to 3 failures per group
  - Critical component must be tested early and extensively
    - Recent review dedicated to Serial Powering and Grounding on Feb 10-11.



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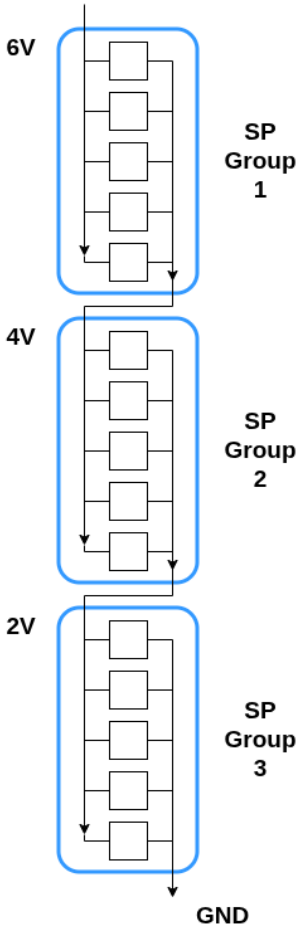
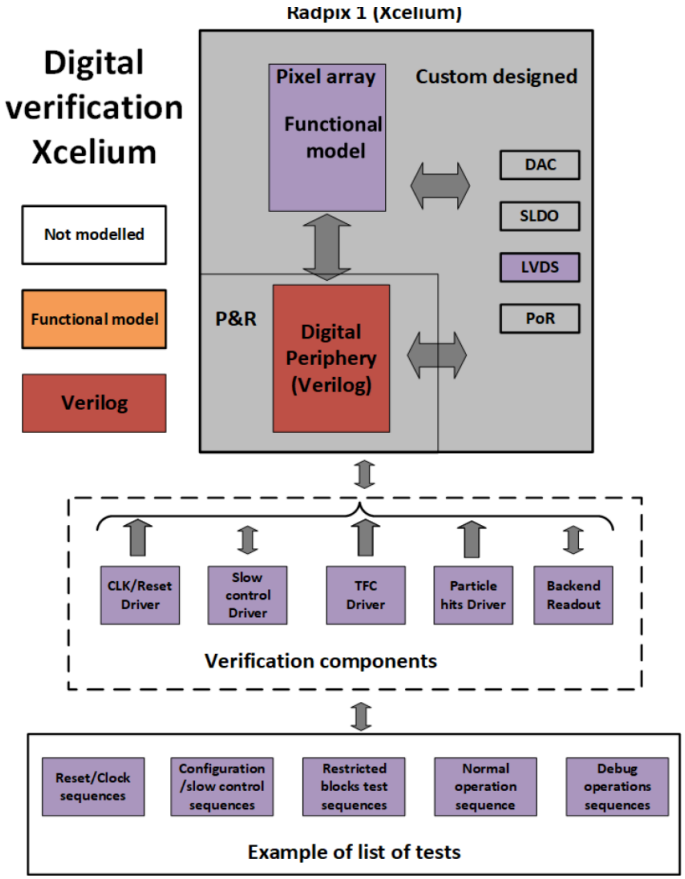
**Low Power?** - need to measure with the real chip



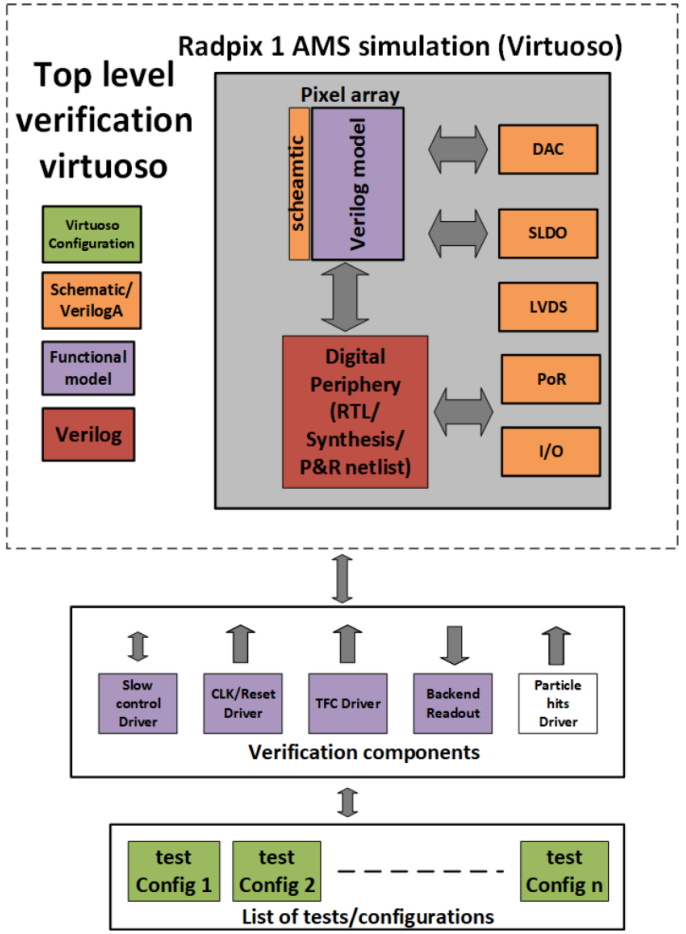
# 4. Verification

- **Functional verification**
  - verify **all digital readout functionality with models for the rest** (pixel matrix and transceivers)
  - Verification components : slow control, fast control, backend readout…
  - **Reuse**: backend can use some test components (descrambling, decoding…)
  - FPGA emulation - use models to create a fake chip and test with real readout



# Verification

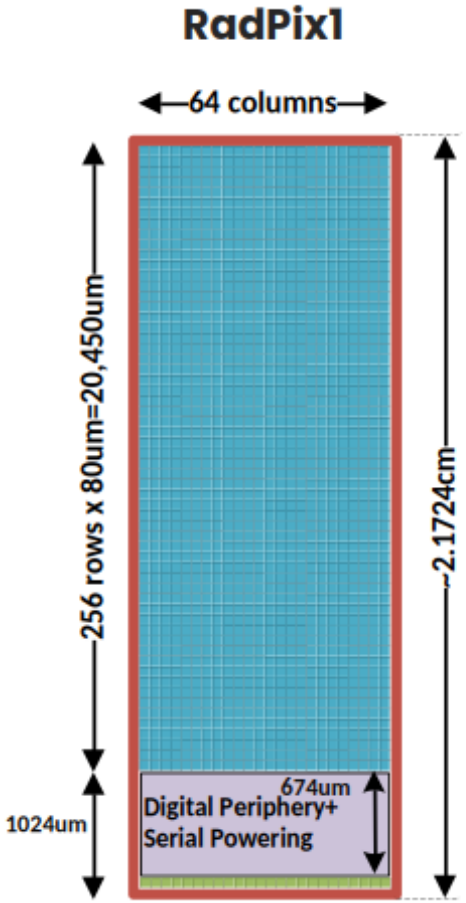
- **Mixed-signal verification**
  - Validate Place&Route with delay models
  - Verify **blocks not covered by functional verification** (matrix, SLDOs…)
  - Simulation sign-off



# How does our chip fare?

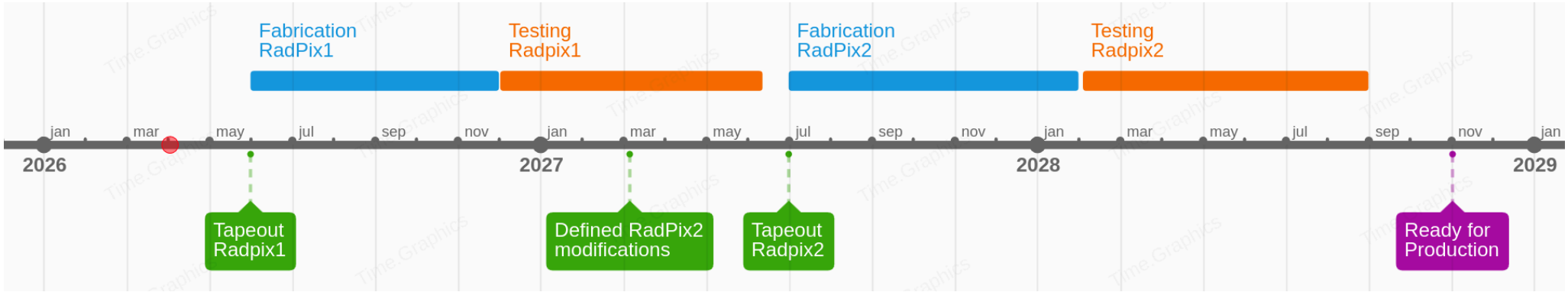
It needs to be :

- Radiation Hard
  - RD50-MPW4 matrix
  - new digital components to be tested
- Low Mass - by design
- High Data Rate - RadPix2
- Low power consumption - in design but needs measurement
- Low Cost - by design



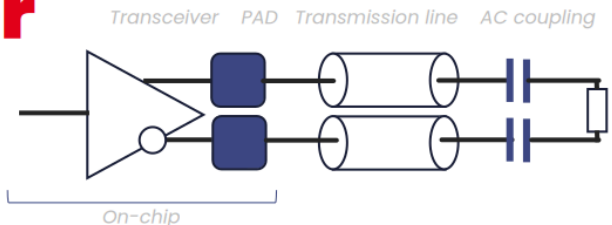
# Summary

- 👑 🇬🇧 **UK-driven** 🇬🇧 👑 pixel chip for LHCb Upgrade 2
  - Strong candidate for two subdetectors - UP and MT-Pixel
- Realisation of the cutting-edge detector work of RD50 collaboration
- Emphasis on verification & simulation with goal of fewer chip iterations
- Almost ready to submit RadPix1



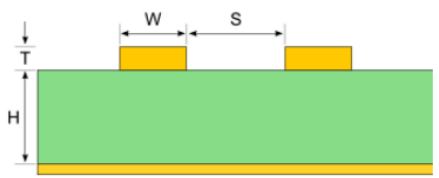
# Backup

# WP3- LVDS Transmitter and Receiver

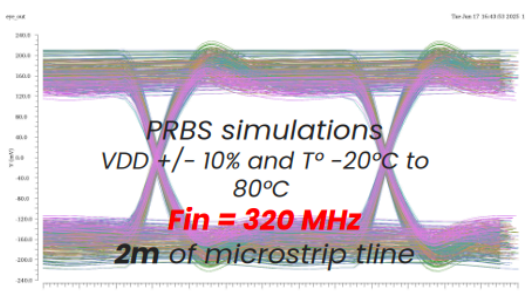


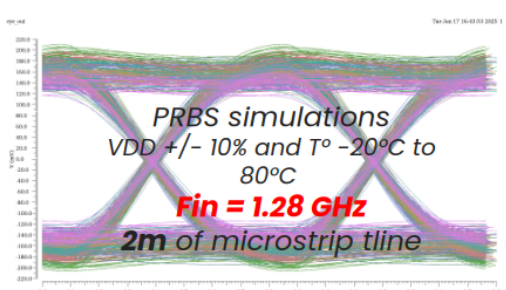

- **Transmitter**
  - Description : LVDS transmitter (Vocm = 0.9V)
    - Adjustable output current : from 1 mA to 8 mA
    - Up to 1.28 GHz bandwidth → I average = 5.9 mA
    - Pre-emphasis for long transmission line (2m) → Simulations with a realistic flex stack
      PE width and current adjustable for different signal frequencies and signal line impedance
    - Rad-hard design tested in TSMC 130nm
  - Status: schematic & Corners simulations **Done**, layout & extraction **on-going**

**Differential Microstrip**

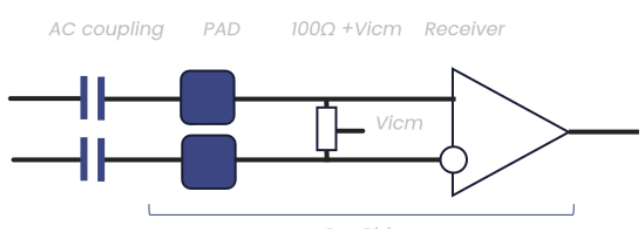



*W:105µm T: 25 µm (copper)*
*S: 100 µm*
*H: 75 µm (kapton)*
*Ground plan : 25 µm (copper)*



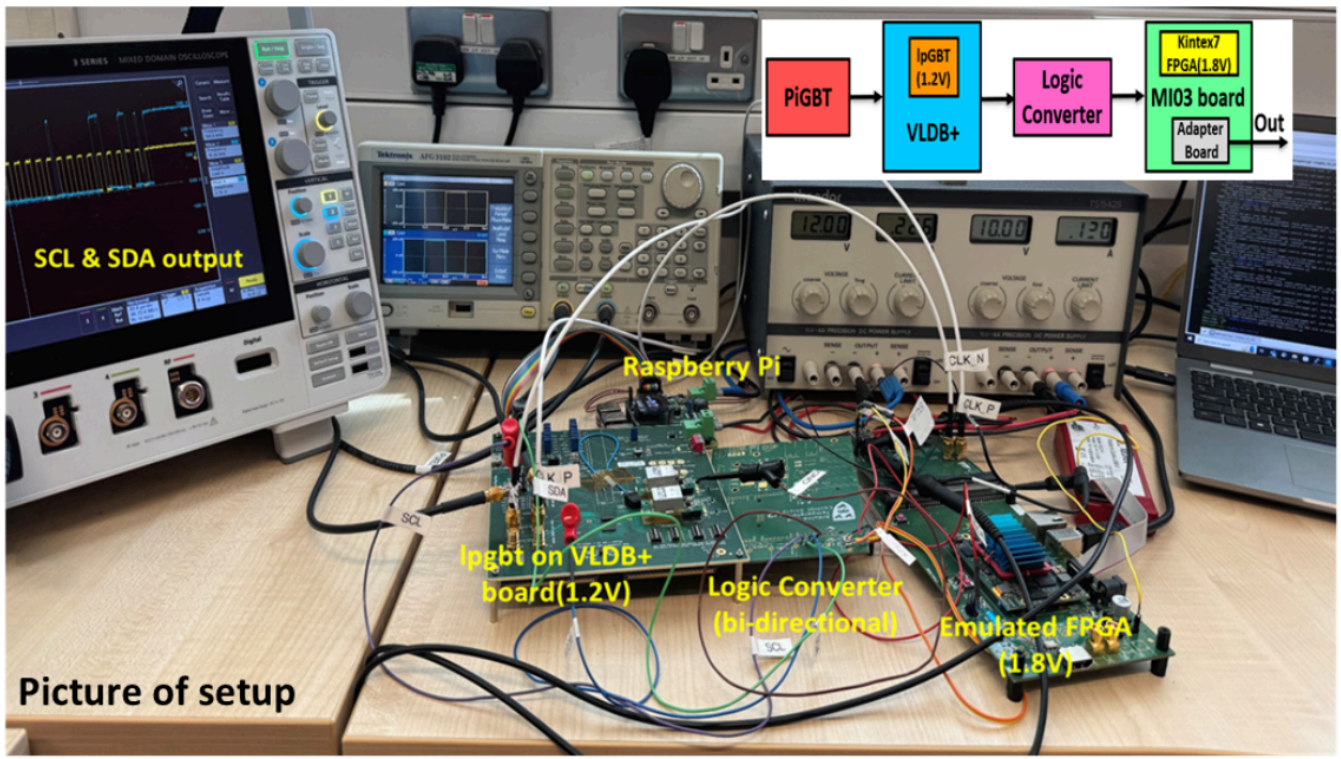




- **Receiver**
  - Description : LVDS receiver (Vocm = 0.9V)
    - Optional internal input resistance
    - Up to 1.28 GHz bandwidth
    - Rad-hard design tested in TSMC 130nm
  - Status: Schematic, corners simulations, layout & extraction **on-going**



# WP4-FPGA Emulation

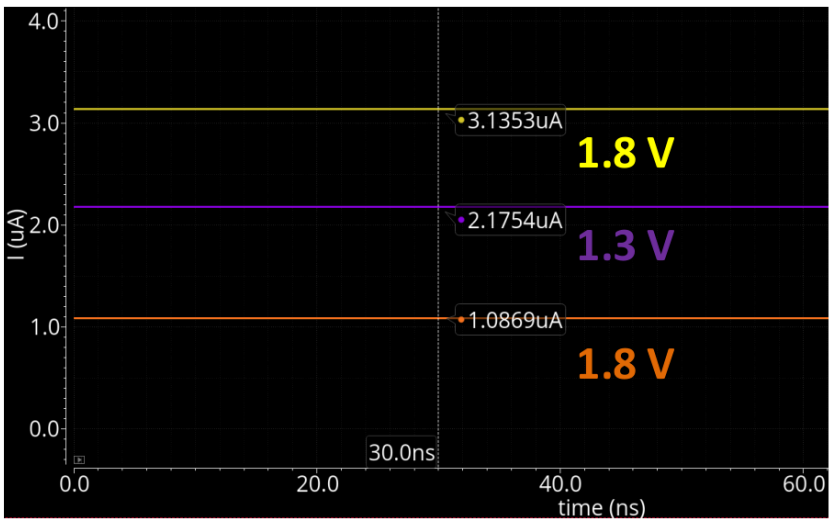
- **Goal:** To use an FPGA to emulate digital features of the chip- using Kintex 7 Mercury FPGA



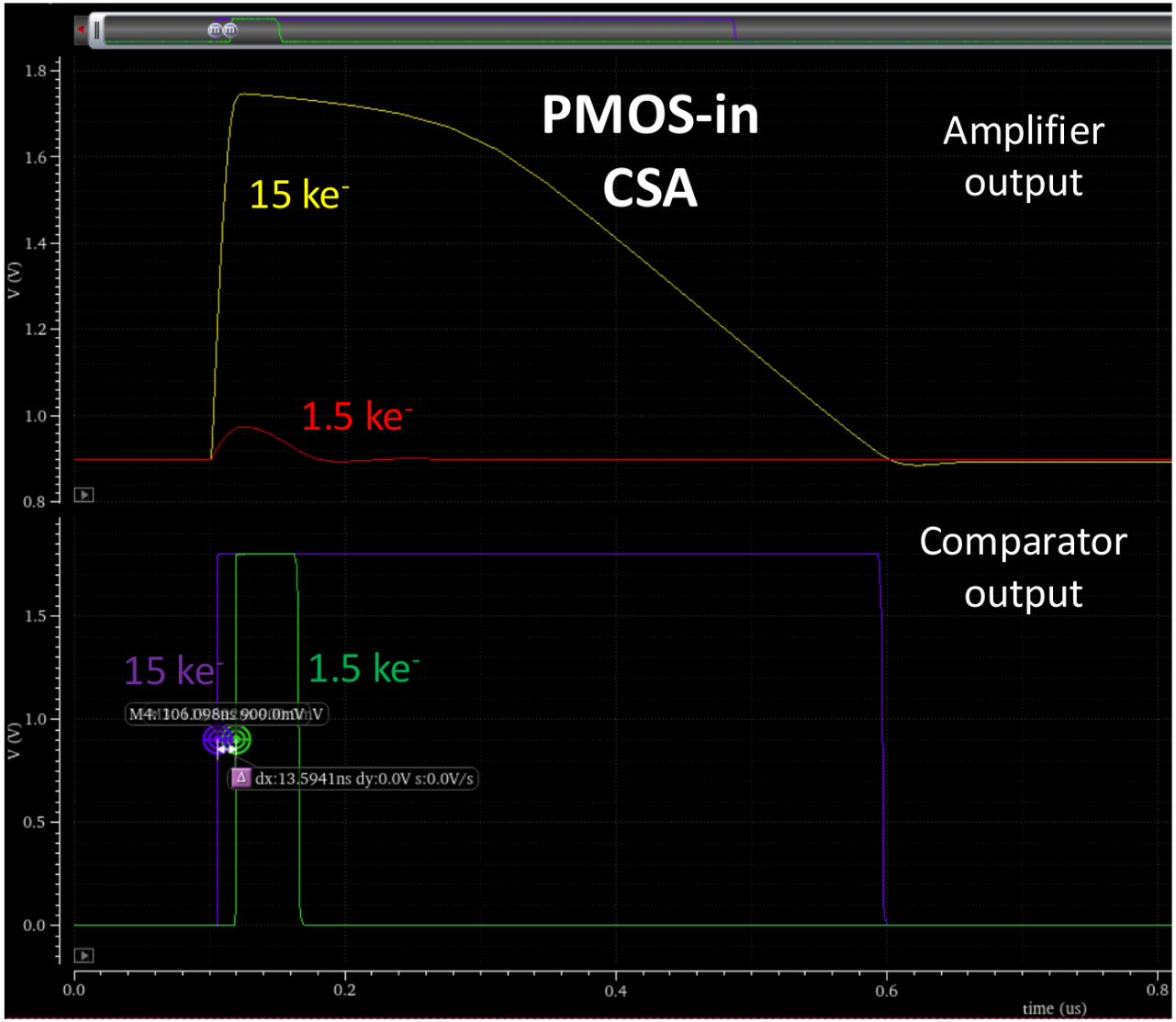

- To ***initiate the communication*** between lpGBT and chip emulator over I2C for sending and receiving data. - **DONE**
- To ***configure the emulated chip*** using I2C interface. **DONE**
- To ***verify behavior of the chip*** in LHCb environment with LHCb protocols via lpGBT (low power gigabit transceiver) using VLDB evaluation board. **ONGOING**

# WP1 - Pixel matrix

- All pixel flavours:
  - ~ 10 µW/pixel -> ~ 150 mW/cm$^2$



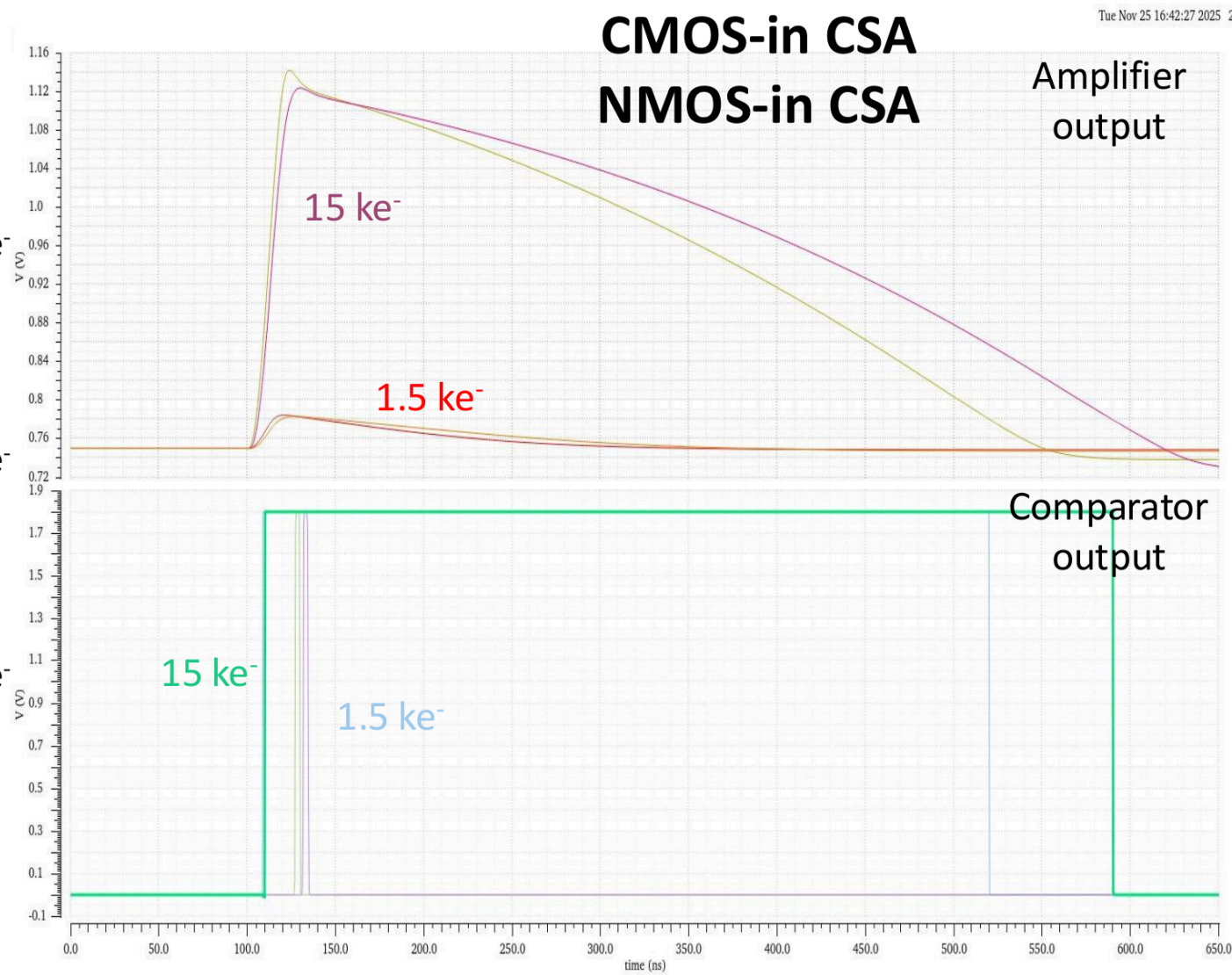

1. Pixel with **PMOS-in CSA**:
   - Rise time: 11 ns
   - Time walk between 1.5 ke$^-$ and 15 ke$^-$ input signals: 13.6 ns (Vth -> 5 x ENC)



# WP1 - Pixel matrix

2. Pixel with **NMOS-in CSA**:
   - Rise time: 13 ns
   - Time walk between 1.5 ke⁻ and 15 ke⁻ input signals: 21.8 ns (Vth -> 1.5 ke⁻)
3. Pixel with **CMOS-in CSA**:
   - Rise time: 11 ns
   - Time walk between 1.5 ke⁻ and 15 ke⁻ input signals 18.5 ns (Vth -> 1.5 ke⁻)
4. Pixel with **Trans-impedance amplifier**:
   - Rise time: 12 ns
   - Time walk between 1.5 ke⁻ and 15 ke⁻ input signals: 8 ns (Vth -> 5 x ENC)

- **Status:**
  - pixel schematic & simulations **Done**
  - pixel layout & extraction **Finishing**



# DAQ development and evaluation plan

- Use **MARS** as the DAQ system to maximise compatibility between institutes

- **Lab measurements**
  - I-V curves, with controlled temperature
  - Standalone chip block performance against chip specifications
    - Pixel matrix with test pulses and with radioactive sources (analogue output, S-curves, in-pixel trimming DAC optimisation)
    - Chip periphery functionality (TFC, LVDS at required speed)
    - Voltage regulators (as a function of temperature, VDD and process variations)
  - Full chip (pixel matrix + digital periphery powered with voltage regulators)
    - Time resolution (with scintillator setup)
    - Power consumption
    - Hit rate
  - Serial powering with > 1 RadPix chip

| | |
|---|---|
| **Chip thickness [µm]** | 100, 200 |
| **NIEL [$n_{eq}/cm^2$] at Ljubljana** | Several steps until 4E15 |
| **TID [Mrad] at Oxford or RAL** | Several steps until 250 MRad |

- **Irradiation studies and test beam evaluation**
  - NIEL, TID, SEEs and test beams (efficiency, time resolution as a function of HV, comparator threshold…)

- **Multi-chip operation (*e.g.* RadPix on on-module hybrids/flexes)**