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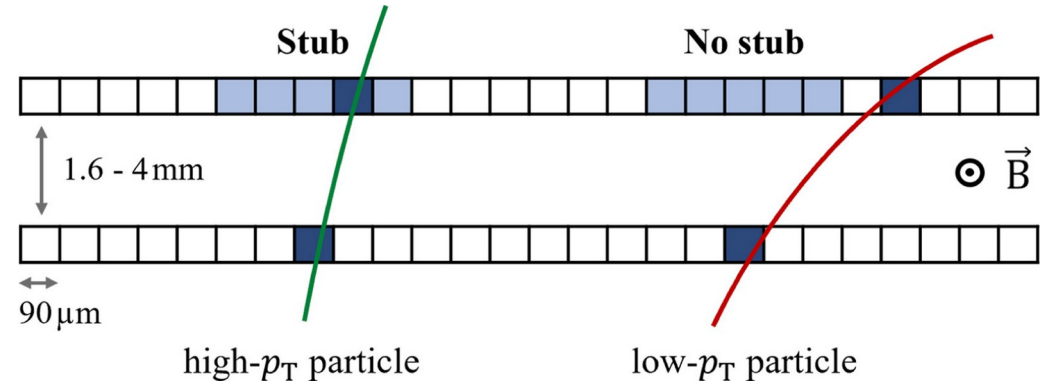
Commissioning of the CMS Phase-2 Tracker Cosmic Test Stand

April 8th 2026

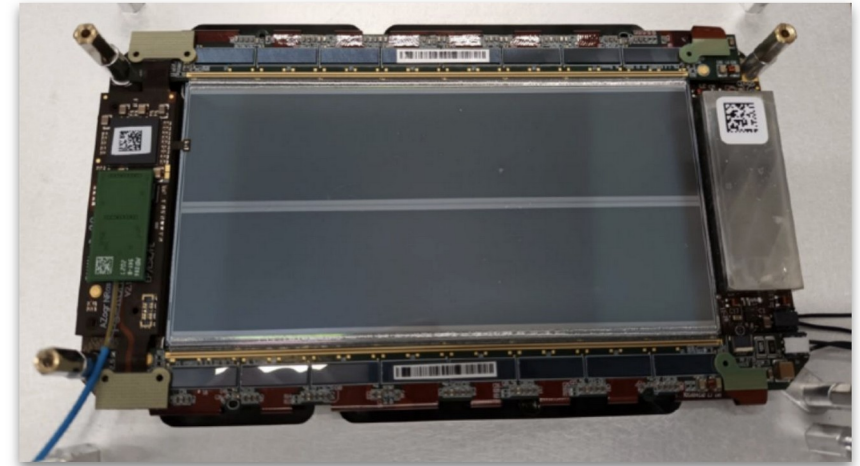
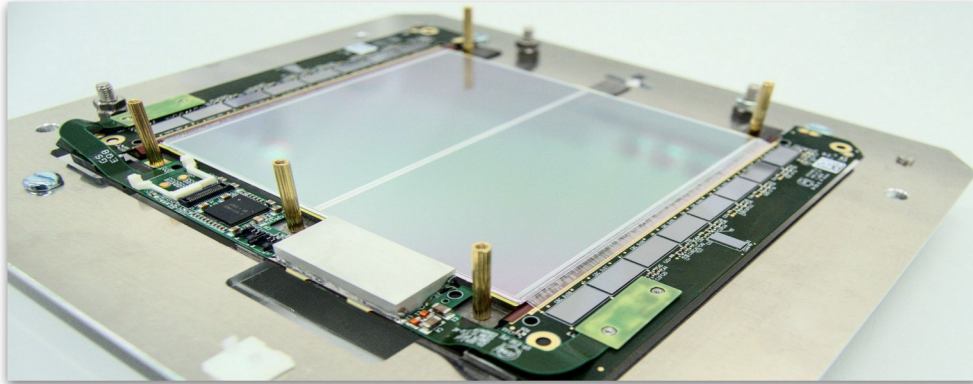
Andrew Mastronikolis

Introduction to CMS Phase 2 Outer Tracker

- The Phase 2 Outer Tracker systems consists:
 - 13,200 Silicon pT Modules.
 - 2S-Modules & PS-Modules
- Transmit two types of objects: Stubs and Clusters.
- A “Stub” is simply a set of 2 clusters within a window
- Modules transmit stubs at 40MHz
- Modules send full cluster data upon L1A
- New Upgrade Feature: Tracks Reconstructed Online!



2S pre-production module

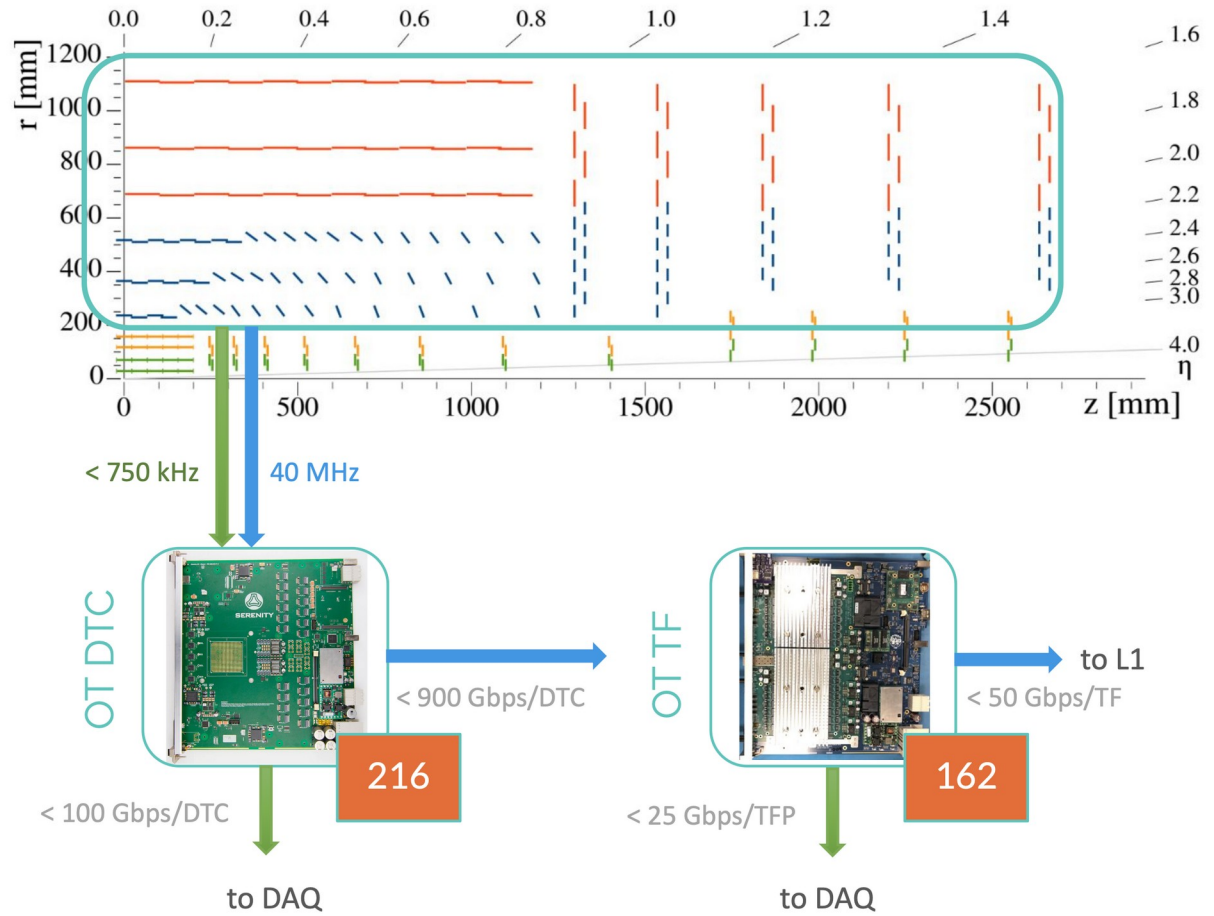


PS pre-production module

Introduction to CMS Phase 2 Outer Tracker Backend Systems (I)

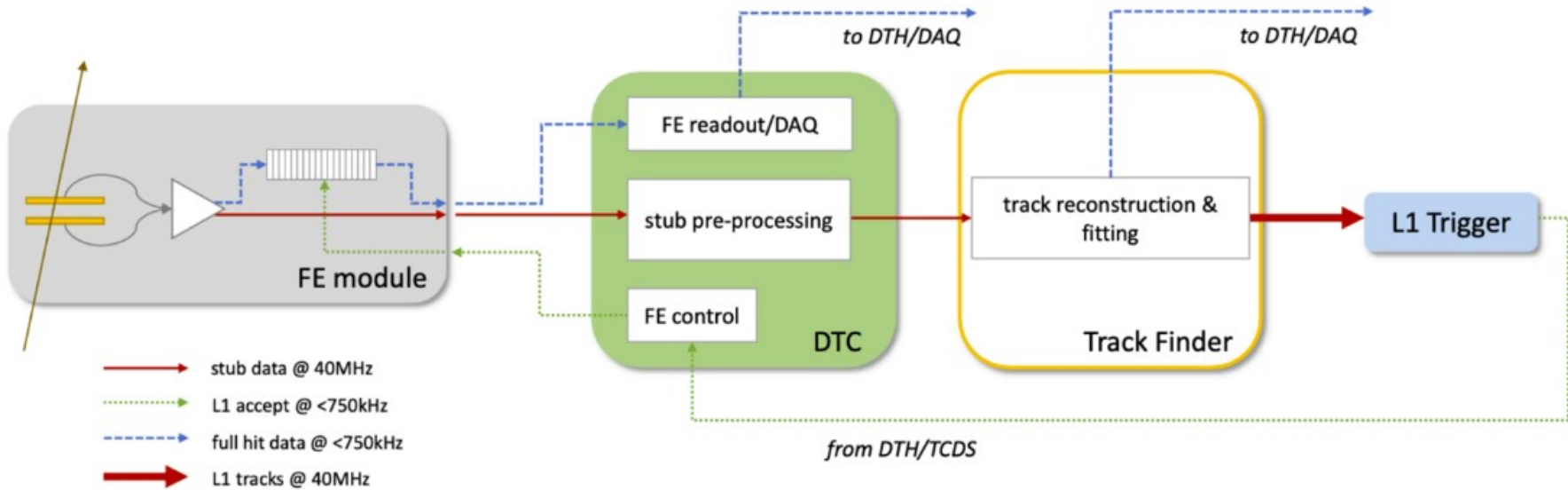
Outer Tracker Backend composed of two stages:

- Data, Trigger and Control (OT DTC) Boards.
 - Uses **Serenity** Platform
 - Employs 128 Channels for Optical I/O
 - Single FPGA on Board.
- Track Finder System (OT TF)
 - Uses **Apollo** Platform
 - Employs two FPGAs on Board.
- Total of 378 Blades needed @ P5 in ATCA Crates.
- **A 738 Gb/s event processor (Output to L1) !**



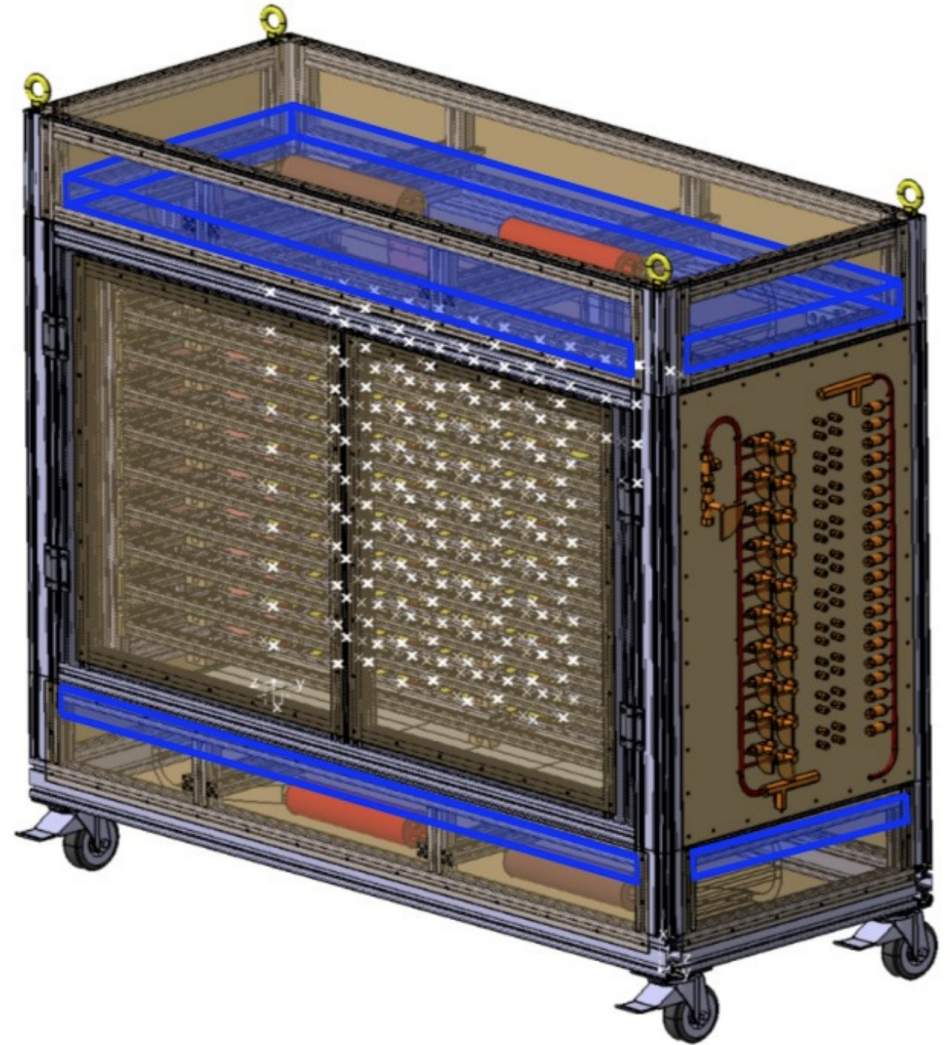
Introduction to CMS Phase 2 Outer Tracker Backend Systems (II)

- L1 builds physics objects.
 - e.g. **Vertex Finding** and **Jet Clustering**
- Global Trigger issues an L1A for a specific event.
- L1A arrives at the DTC boards, which forwards the signal to front end modules.
- Front Ends have a SRAM memory that saves 512 BX (25 ns) of information.
- This implies that computing has to happen within 12.5 microseconds from the original event.
- Upon reception of L1 packets from the front ends, **DTC performs event building** and routes everything off to DAQ.
- Full Trigger & DAQ Chain was never exercised before 2026 (with physics).



Introduction to the CMS Phase 2 Cosmic Stand (Front End)

- CMS Cosmic Stand (or Rack) or **CRACK**
 - **Fundamental Goal:** Exercise the Full TDAQ Chain.
 - Use Cosmic Muons to do this.
- Components (Front End)
 - Vertical assembly of **72 2S Modules** (currently 48 only)
 - Two plastic scintillators (**blue**, top and base)
 - Four PMTs (**red**, top and base)
 - The top and base scintillators are connected to their two respective PMTs.
 - Electrical signals from PMTs fed to the CRACKs backend system (next slide)



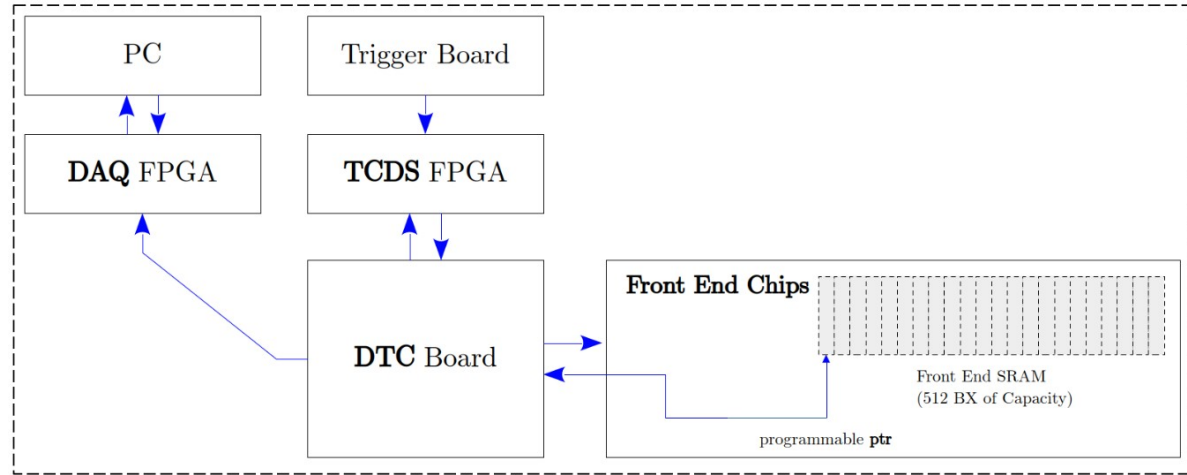
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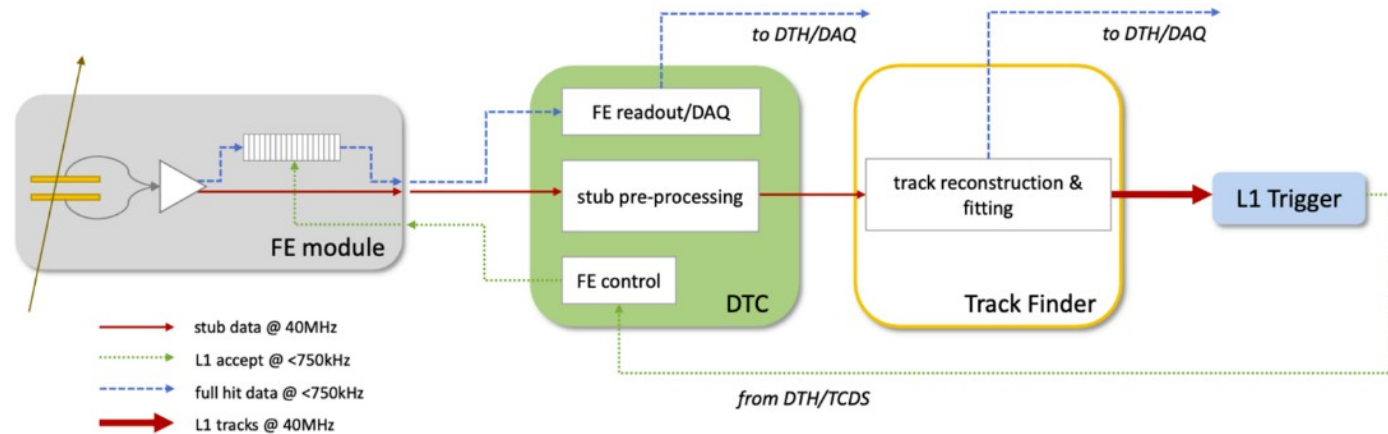


Introduction to the CMS Phase 2 Cosmic Stand (Backend)

- CRACK Backend (Top Picture)
 - Two Types of Boards: Serenity and DTH P2
 - Trigger Board (Input from CRACK PMTs)
 - TCDS FPGA (**DTH Board**, Trigger Handling and Clock Distribution)
 - DTC Board.
 - DAQ FPGA (**DTH Board**, Further Event Aggregation)



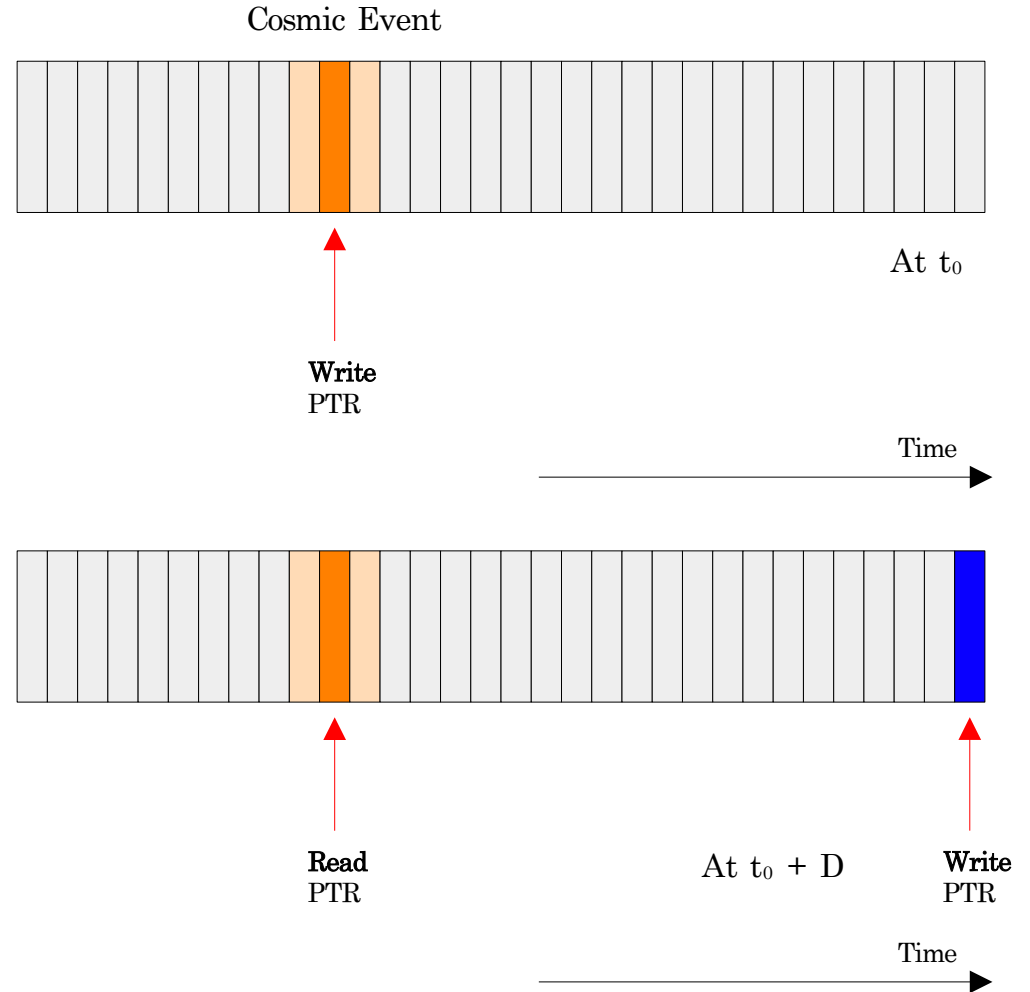
CRACK TDAQ Architecture



CMS TDAQ Architecture

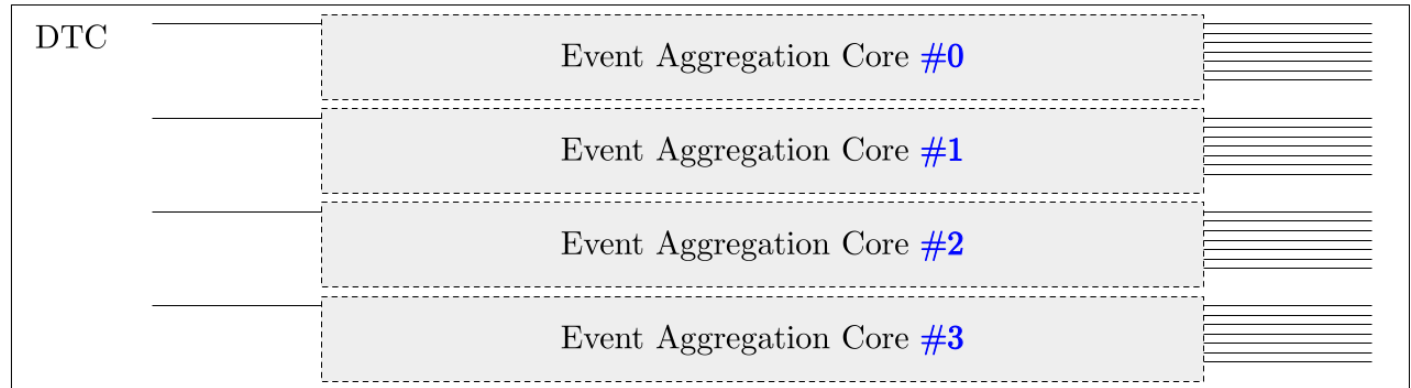
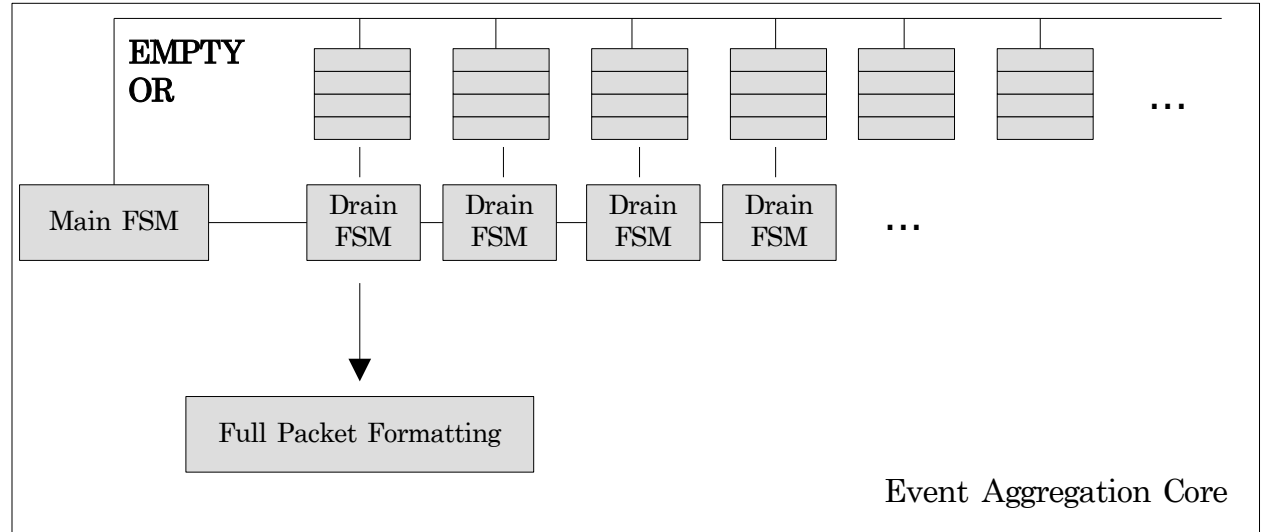
Brief Review of Front End Chip Architecture

- Each front end chip contains a buffer SRAM that can save up to 512 Events (BX := 25ns) worth of data.
- When a cosmic passes through, it leaves detector hits (**orange**) and at the same time, triggers the PMTs.
- By the time the L1A reaches the front end, write slot has drifted to the right (**blue**)
- Read PTR is programmable and can be set to be any value in $[0, 512]$ BX.
- A “Latency Scan” should yield a peak, since physics event and the delay are correlated.



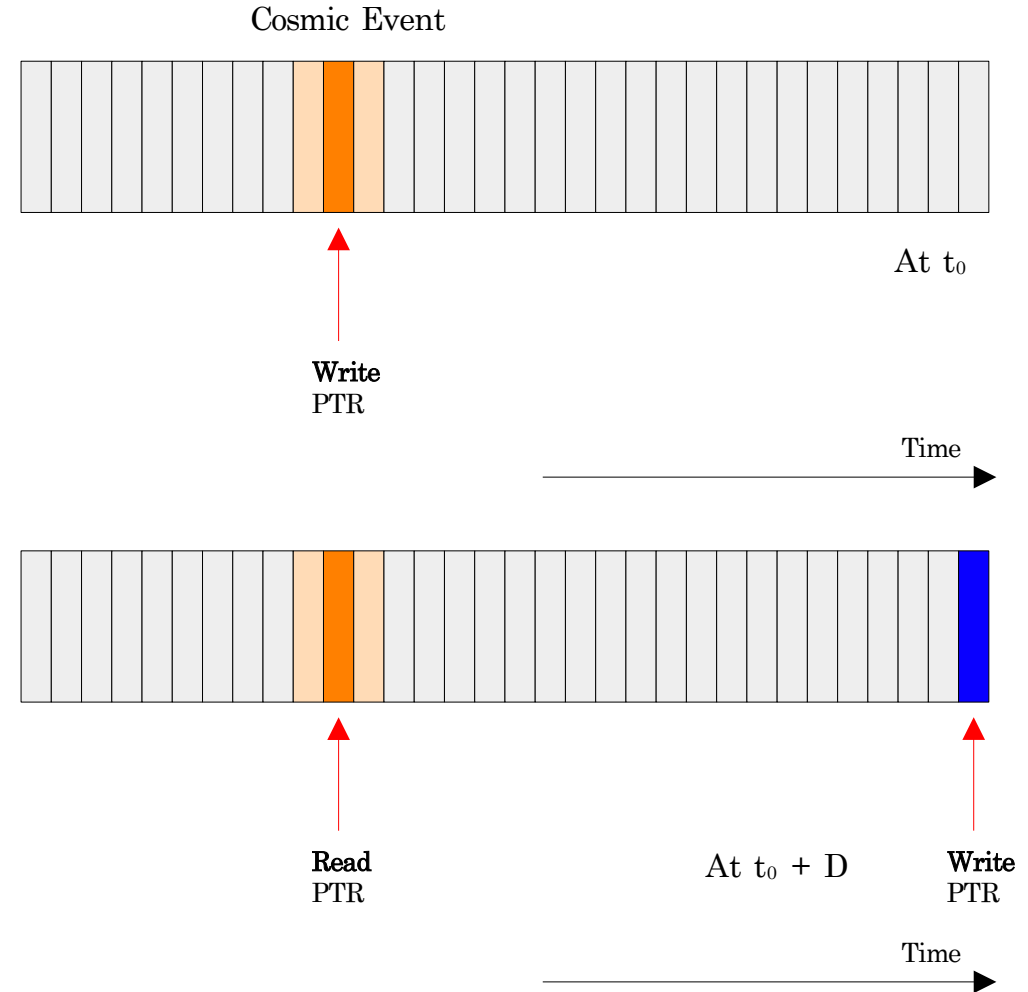
Brief Review of DTC DAQ Firmware Architecture

- For event building on the DTC, a **token ring** is implemented.
- Token is passed around each Front End FIFO on the FPGA, collecting data for that event from that link.
- Each firmware unit that performs aggregation over N links is called a **Event Aggregation Core**.
- OTC DAQ is implemented in 4 distinct Cores that aggregate 18 Front-End links each (72 in total)



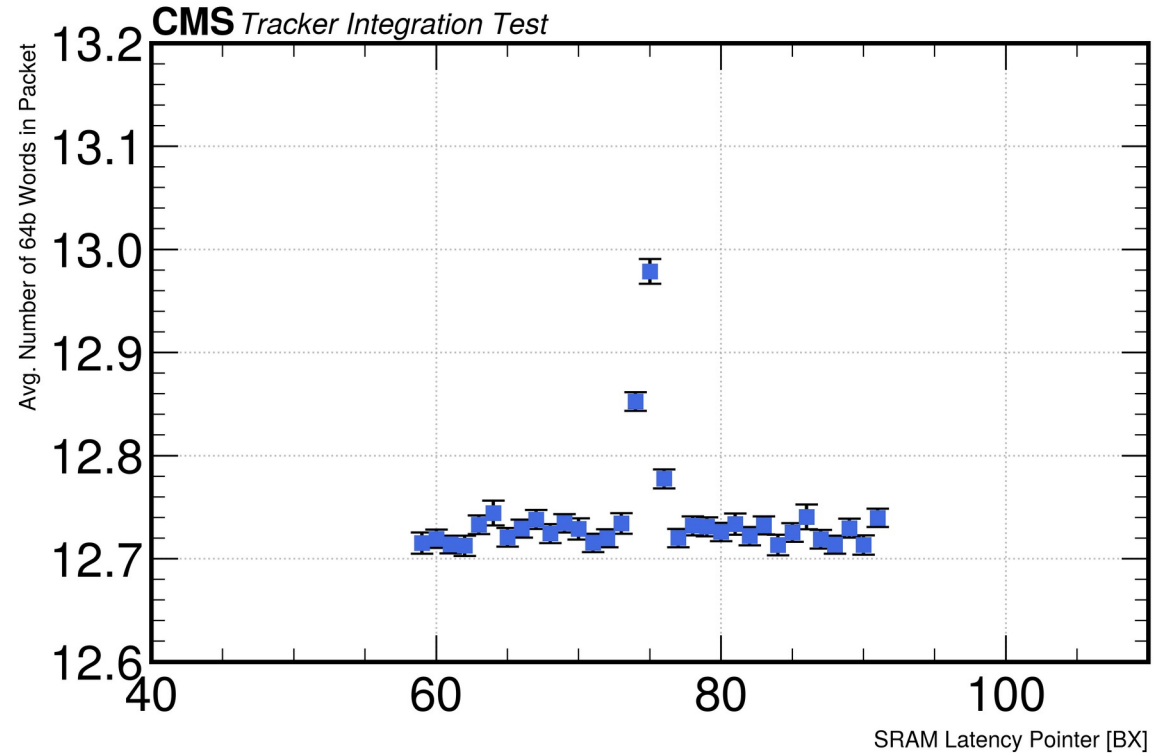
Quick Review of TDAQ

- ✓ We can send triggers to the front ends via PMT trigger signals
- ✓ We can perform event based aggregation on the returned packets from the front end, in a scalable manner.
- One thing left to do:
Directly measure the packets sizes (as a proxy for detector activity) vs. latency read addresses in the SRAM.
- If things were done right, we should observe a clean peak at one address, that corresponds to physics.



Calibrating the Cosmic Stand with Physics

- Procedure:
 - Look at an average of # of 64b words @ each SRAM address.
 - Plot the entire spectrum.
- Peak observed in latency scan @ 75 BX behind the write pointer.
- Plotting purely average packet size at each point.
- Read out from 3 Event Aggregation Cores, each one aggregating 12 Links.
- Covers 50% of the DTC.



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Thank you

And many thanks to:

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