Frontend Electronics and DAQ for AC-LGADs

Status and Plans

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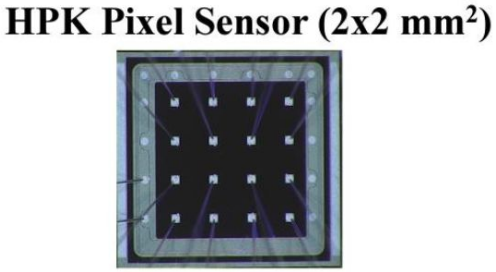
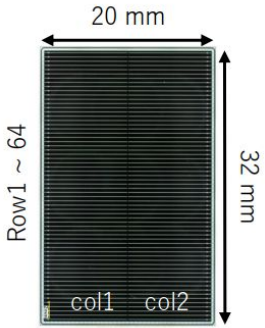
Overview

- AC-LGAD sensors & associated EPIC detectors
  - pixel and strip AC-LGADs
    - strips: Barrel TOF
    - pixels: Forward TOF, Roman Pots, B0 Tracker, Off Momentum Detecttors, Luminosity Monitors
- Common Readout Scheme
  - Control & Data Aggregation ASIC (lpGBT, CERN), optical transceivers (VTRX+, CERN)
- Readout ASICs
  - EICROC (OMEGA, France) for pixel AC-LGADs
  - FCFD (Fermilab, USA) for strip AC-LGADs
- Service Hybrids
- Detector Aggregation Module (DAM) aka Receiver Board
  - FELIX (ATLAS, CERN) chosen for the full EPIC DAQ
  - AXAU15 (commercial FPGA board) for prototyping, testing, beam tests, commissioning…
- Streaming Readout
- Backend Processors (PCs)
  - online processing & calibration
- Readout Chain
  - BTOF, FTOF
  - Components on hand
- Conclusion

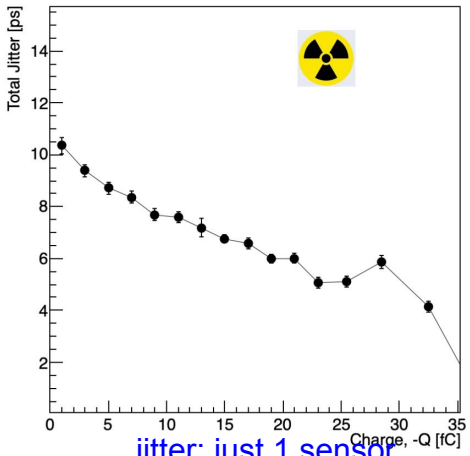
AC-LGAD silicon sensors

- "AC-coupled Low Gain Avalanche Diode"
  - similar to standard LGAD's but AC-coupling adds charge sharing between sensor elements which in turn improves positional resolution using e.g. center-of-gravity calculations
- Different pixel and/or strip sizes and geometries possible
  - in EPIC:
    - BTOF: 500 um X 1 cm strips
    - FTOF, FF: 500 um X 500 um pixels
- Advantages
  - excellent timing resolution (20-50 ps)
  - excellent position resolution (<30 um)
  - various sensor geometries possible
  - low power
  - radiation tolerant
- Disadvantages
  - relatively novel technology (R&D still required to optimize design parameters)
  - preamplifiers and digitizers are located in external ASICs w associated mounting complications
    - tricky bump-bonding or wire-bonding sensor⇔ASIC

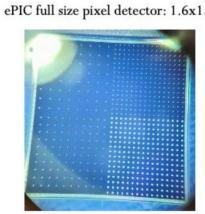




AC-LGAD Cont'd



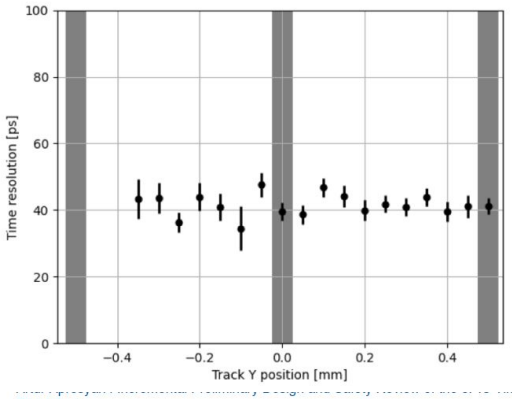
jitter; just 1 sensor

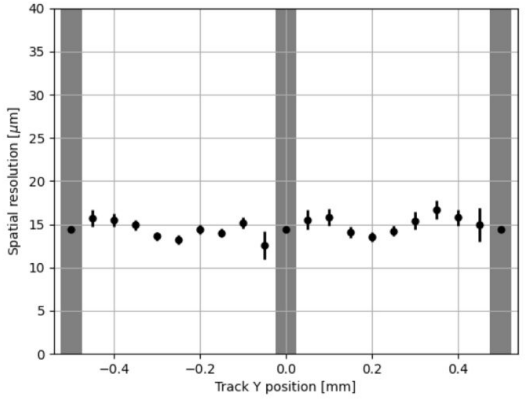


- Components that go into overall timing:
  - $\sigma_T^2 = \sigma_{LGAD}^2 + \sigma_{preamp/disc}^2 + \sigma_{Internal\ Clock}^2 + \sigma_{System\ Clock}^2 + \sigma_{TDC}^2$

Component	Spec
LGAD+ preamp/discriminator	~40 ps
Internal clock distribution	< 10 ps
System clock distribution	< 10 ps
TDC binning	< 10 ps
Total	~ 45 ps

- Results published in NIM A 1089 (**2026**) 171599





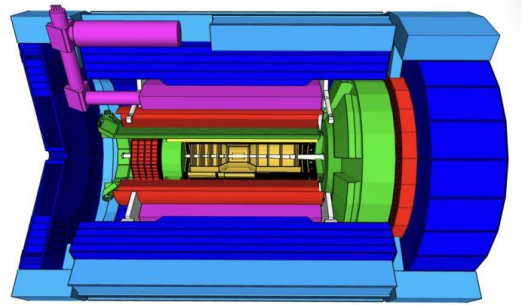
Parameters to optimize
- active thickness 20 or 30 um?
- electrode 100 vs 150 um?

Can we successfully bump-bond pixel sensor to pixel ASIC?
- % of failed bonds??

Total jitter with ASIC needs careful evaluation

AC-LGAD-based Detectors in EPIC

- Barrel TOF (BTOF) as the strip sensor detector
- Forward TOF (FTOF) and ancillary detectors which share its pixel sensor approach and are located further away along the beam
  - Roman Pots (RP), Off-momentum Detector (OMD), B0 Tracker, Luminosity Pair Spectrometer



red: BTOF & FTOF

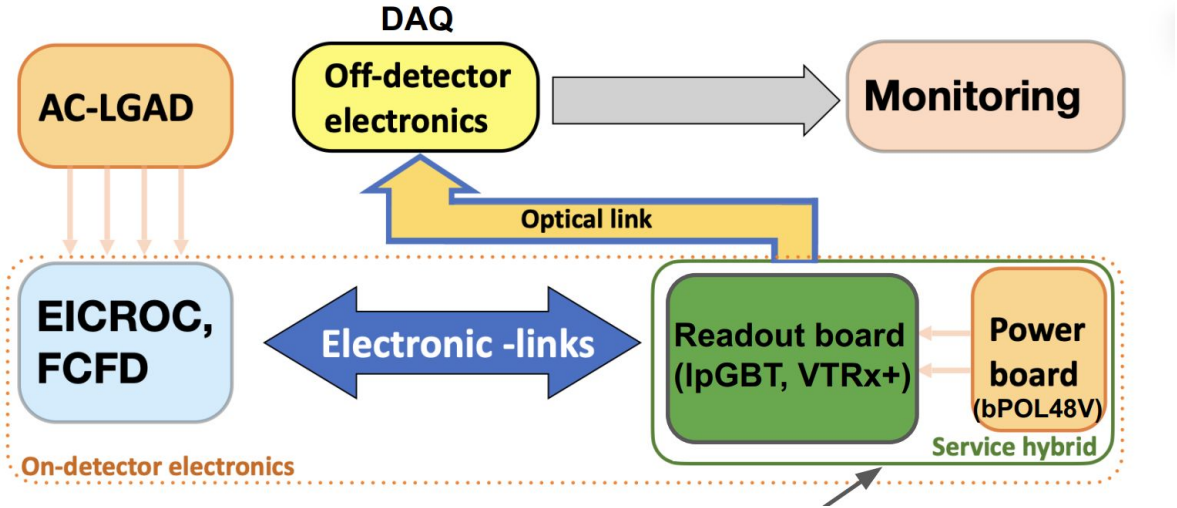
Subsystem	Area (m^2)	pad-size (mm^2)	channel count	timing σ_t (ps)	spatial σ_x (μm)	material budget (X/X_0)
BTOF	12	0.5*10	2.4M	35	30 ($r \cdot \phi$)	3%
FTOF	1.1	0.5*0.5	3.2M	25	30 (x, y)	5%

Required timing resolutions: 25-35 ps
Required spatial resolutions: 20-140 um

Subsystem	Area (m^2)	Pad-size (mm^2)	Channel Count	Timing σ_t (ps)	Spatial $\sigma_{x,y}$ (μm)	Material budget (X/X_0)
Roman pots	0.135	0.5*0.5	541k	35	< 140	5%
Off-momentum det.	0.08	0.5*0.5	295k	35	< 140	5%
B0 tracker	0.12	0.5*0.5	516k	35	< 20	5%
Lumionsity Pair spectrometer	0.1296	0.5*0.5	520k	< 9 ns	< 70	5%

Common Readout Scheme

- [on detector] Sensor ⇒ Readout ASIC ⇒ Service Hybrid (Readout & Power Board) ⇒ {fiber}
- [off detector] Data Aggregation Module (DAM) ⇒ DAQ PC ⇒ Event Builders ⇒ “Tape”



Readout ASICs: EICROC

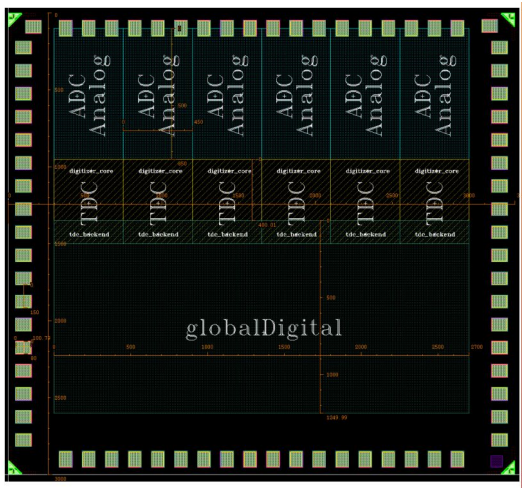
⇒ see detailed morning's presentation Christophe et al

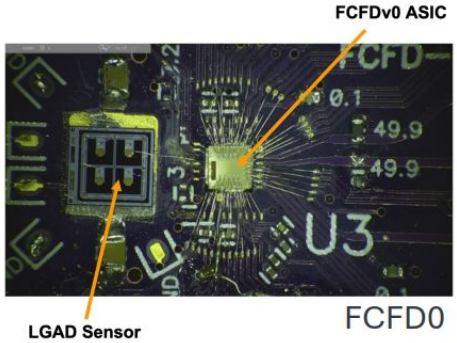
Quick recap:

- designed for 500 um X 500 um AC-LGAD pixels
- 1024 channels (32x32)

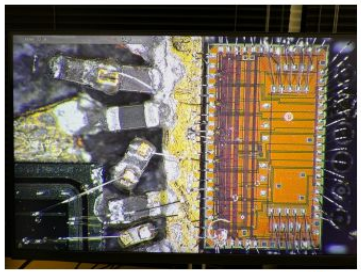
Readout ASIC for strips: FCFD

- Designed at Fermilab for strip AC-LGADs
- Constant Fraction Discriminator based ⇒ avoids the need for offline timewalk calibration
- Various prototypes: v0, v1, v1.1
- Current version FCFDv1.2
  - submitted in Apr 2026: full digital backend readout, streaming mode
  - only 6 channels
  - 3300 um X 3000 um
  - Testboard being designed…
- FCFD2: full functionality, full 32 channels (end of 2027)
- FCDF3: final version (end of 2028)





FCFD0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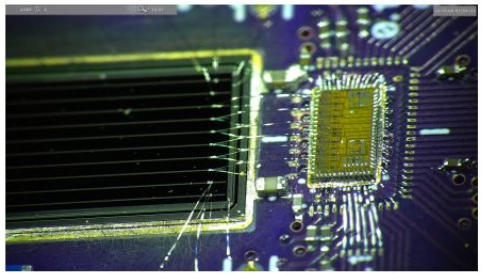
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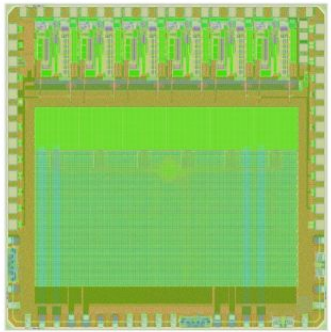

FCFD1.2

Readout (RB) & Power Boards (PB) [Service Hybrids (SH)]

- Readout Board
  - provides electrical interfaces between multiple ASICs for data, timing and control
    - we use CERN-developed lpGBT ASICs
    - as well as the MUX64 ASIC for monitoring
  - provides electrical to optical interface to the off-detector electronics and processing
    - we use CERN-developed VTRX+ as the electro-optical transceivers
      - up to 4 10 Gbs upstream links to offline processors
      - 2.5 Gbs downlink for timing and control protocols
- Power Board
  - provides a bias voltage (BV) path/conduit from the external BV supplies to the sensors
  - provides required low-voltage (LV) power to the readout ASICs
    - typically 1.2 and 2.5V
    - Note: our ASICs use from 2-4 mW per channel – significant
  - provides LV power to the Readout Board components (1.2V and 2.5V)
  - our main component is CERN-developed bPOL48 DC/DC converter
    - reached 70% efficiency

Side Note: radiation tolerance requirements are **modest ≈1 krad** (orders of magnitude below LHC)

	Both EICROC2 (FTOF) and FCFD (BTOF)
Clock	320 MHz (40 MHz internal)
Fast Command	8 bits @ 320 Mbs
Data Lane #	1
Data Rate	320 Mbs
Zero-suppressed data	Yes
Streaming	Yes
Control Iface	I2C @ 1 Mbs

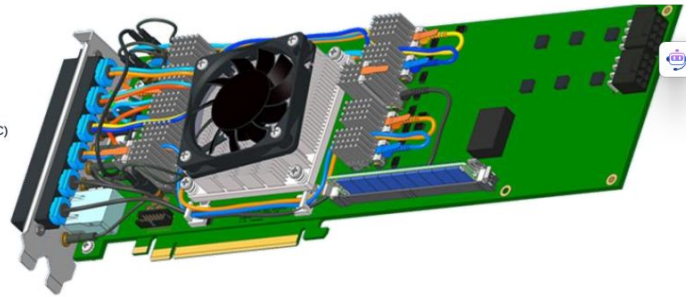
custom boards, more later…

Detector Aggregation Module (Receiver Board)

- The optical “Receiver Board” where the data from multiple Readout Board fibers are aggregated
- EPIC plans to use the “FELIX” board developed by ATLAS@CERN
  - 48 fiber pairs on input
  - PCIe based readout into a “DAQ PC”
  - fiber connection to the Global Clock and Timing unit
  - Powerful FPGA can be used for significant amount on online (real-time) processing, potential AI algorithms under consideration
- At this stage, for convenience, we use a much simpler, smaller, cheaper commercial AXAU15 PCIe FPGA board with only 4 fiber capability ⇒

FLX-155

AMD Versal Premium VP1552
PCIe Gen 5 x 16 (480Gb/s)
48 Bidirectional optical links (25Gb/s)
1 Firefly for Timing Trigger & Control (TTC)
1 Firefly for 100Gb Ethernet



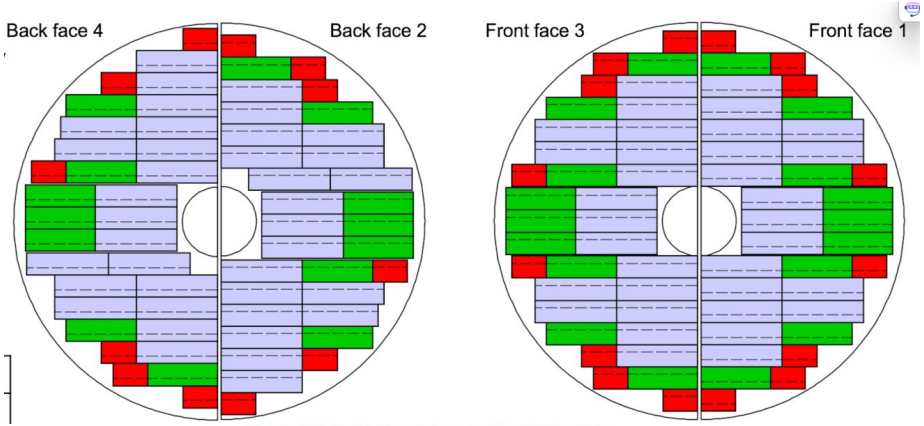
Streaming Readout

- EPIC will use the Streaming Data Readout concept
  - non-triggered mode ⇒ all detector data for all detectors is constantly digitized and sent to the upstream pre-processing
- data is synchronized among different components by using a common EIC clock and a common deterministic SYNC command sent to all RBs at the same instant
  - RB's internal EIC clock counters are reset to 0 upon receipt of the SYNC
    - each future datum is tagged with the smaller (~16bit) internal counter counting at the EIC clock
  - SYNC command is expected every ~1ms or so
    - command payload is a 64 bit EIC clock counter
    - data packets (timeslices) contain the corresponding SYNC counter in their header
- data processing on the DAM board, DAQ PC and later in the Event Builders will stitch the data from different parts of different detectors into 1 full timeslice
    - preliminary online analysis, software triggers and scalers, calibration use, etc
- No trigger window → all the noise is also readout
  - EIC is a low occupancy detector → raw data is mostly noise
  - need robust algorithms to reduce the noise
  - AC-LGAD detectors are particularly good at this
    - actual signal needs to be in a narrow timing window
    - actual signal needs to form a cluster in x-y, needs more than 1 adjacent hit (morphological cut)

Backend Processors (“DAQ PCs”)

- The DAM boards reside in PCIe buses of reasonably powerful DAQ PCs
  - expectation is 1 DAM board per PC; Linux; dense & cheap processing power in racks ⇒
- The PCs are powerful enough for further processing e.g.
  - noise suppression
  - cluster finding ⇐ interesting for AC-LGAD detectors
  - additional data compression
  - online Q&A
  - pre-calibration
- The PCs are additionally expected to have enough buffer space to assemble timeslices from different fibers into 1 larger super-timeslice and send it over 10 Gbs Ethernet to EPIC Event Builders following a designed protocol

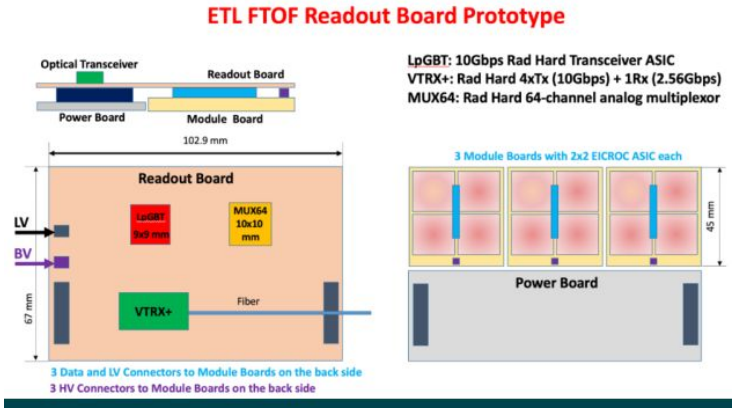
On Detector Electronics for FTOF

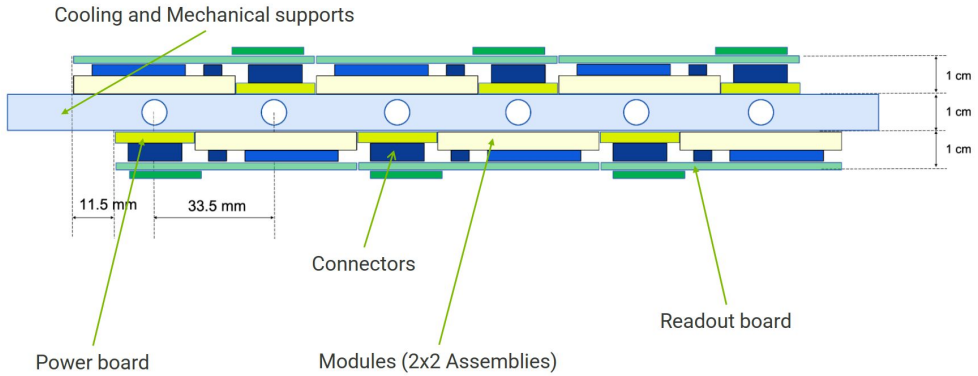


different tiles are Service Hybrids of different length and number of ASICs: 12,24,28

Data rates are modest:
87 Mbs for the largest RB

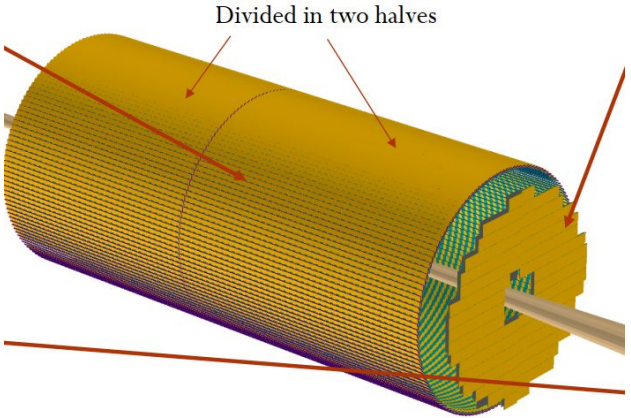
R=60cm

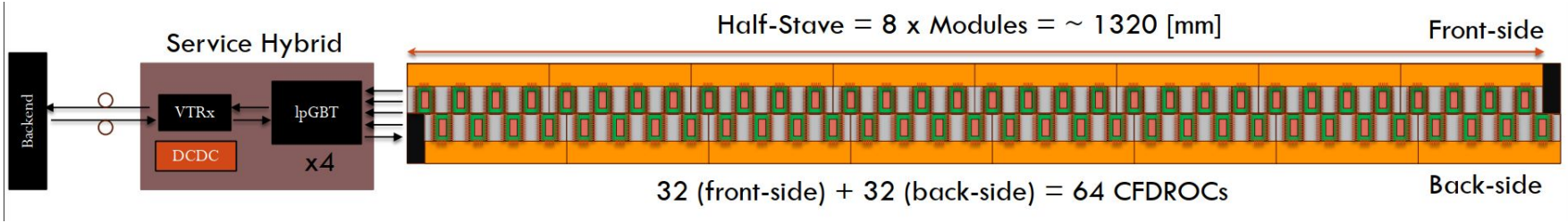




On Detector Electronics: BTOF

Barrel is divided into 2x144 half-staves ⇒



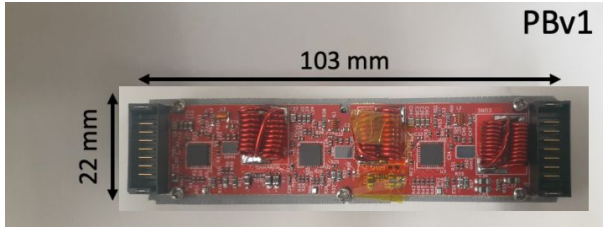


Each stave is double sided and each side has 4x32 Readout ASICs connected to the Service Hybrid at the end of the stave.

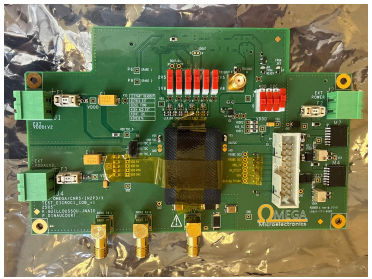
Readout Boards contain 2x lpGBT modules in a master/slave configuration.

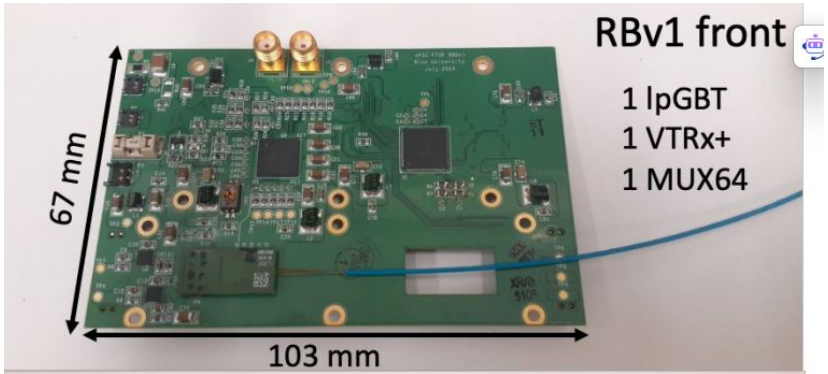
Prototypes Available

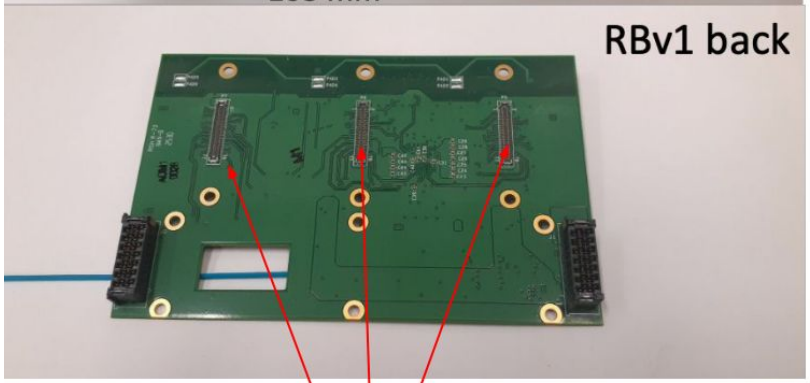
- FTOF Readout Board RBv1 [Rice]
- FTOF Power Board PBv1 [BNL]
- commercial PCIe FPGA Board AXAU15
  - test setups in Rice and BNL
- EICROC1 Testboard [OMEGA,IN3P3]
  - with ZCU106 FPGA for early testing and debugging [BNL]
  - and adapter for RBv1 [Rice]
- FCFD Testboard (in progress now) [Fermilab]
  - and adapter for RBv1 [Rice]



EICROC1 Testboard

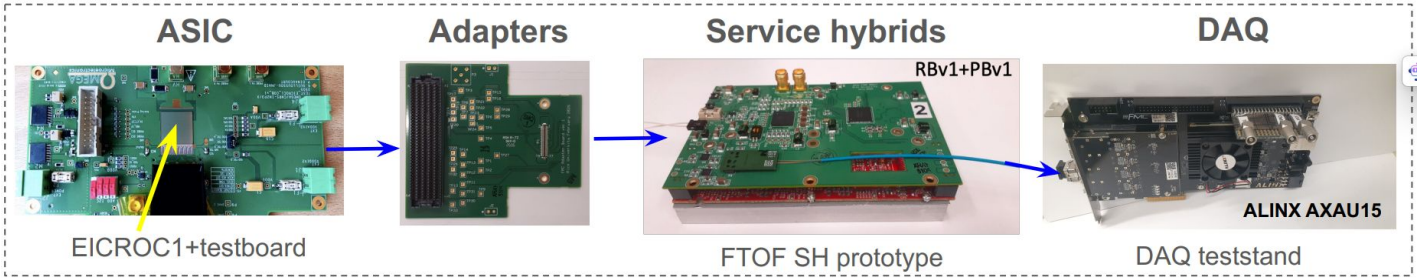






Module connector:
78-pin Kyocera

Readout Chains



1 full chain currently at BNL

another full chain expected at Rice

Current effort: basic sanity tests using FPGA development kits for convenience

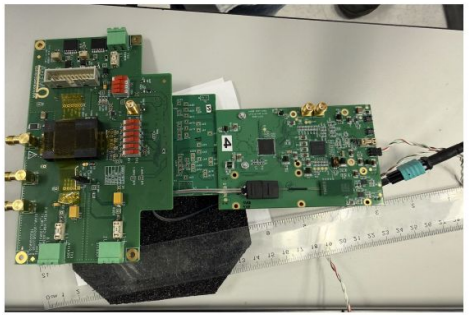
Within weeks: commissioning full lpGBT readout of the EICROC1 ASIC (as shown above)

Near Future

1. Verification of the lpGBT-based RBv1 using the AXAU15 PCIe optical receiver
   a. Done. 2 setups exist: at Rice, at BNL
2. Verification of the bPOL48 based power board
   a. Done. We still need to verify the ASIC powering.
3. Full verification of EICROC1 ASIC with FPGA dev kit using the appropriate lpGBT-compatible ASIC signals
   a. FPGA is convenient because we need to fully understand the control signals, I2C register setups, data format
4. Full verification of the EICROC1 ASIC with lpGBT-based RBv1 readout ⇒
   a. also using the PBv1 Power Board
5. Start developing automated calibration & QA procedures using the Readout chains
   a. for further large-sensor commissioning and lab testing
   b. plans for beam tests
   c. plans for various commissioning and QA steps of detector sub-components
      i. e.g. stavelets, staves, etc.
   d. this commissioning will be ongoing for a long while…
6. Develop Streaming DAQ primitives within the DAM Receiver and DAQ PC
7. Replicate 2..5 for the FCFD ASIC once it and its Testboard become available
   a. Fall 2026

Further down the line

- Design, produce and test a BTOF-specific Service Hybrid
- Use the FELIX DAM for data aggregation
- Work with multiple RBv1's in streaming mode



Conclusion

- We are moving forward with AC-LGAD sensors, corresponding ASICs and their readout schemes
- Currently developing readout chains with 2nd versions of prototype ASICs
  - EICROC1 readout chain expected in ~1 month
  - FCFD1.2 readout chain in testboard development, expected in ~1-3 months
  - **Note:** the currently designed readout chains will also be used in beam tests as well as QA of the subdetector modules during detector installation and commissioning

2026 will be a busy year for Electronics and Readout