

EICROC : AC-LGAD readout chip for EIC

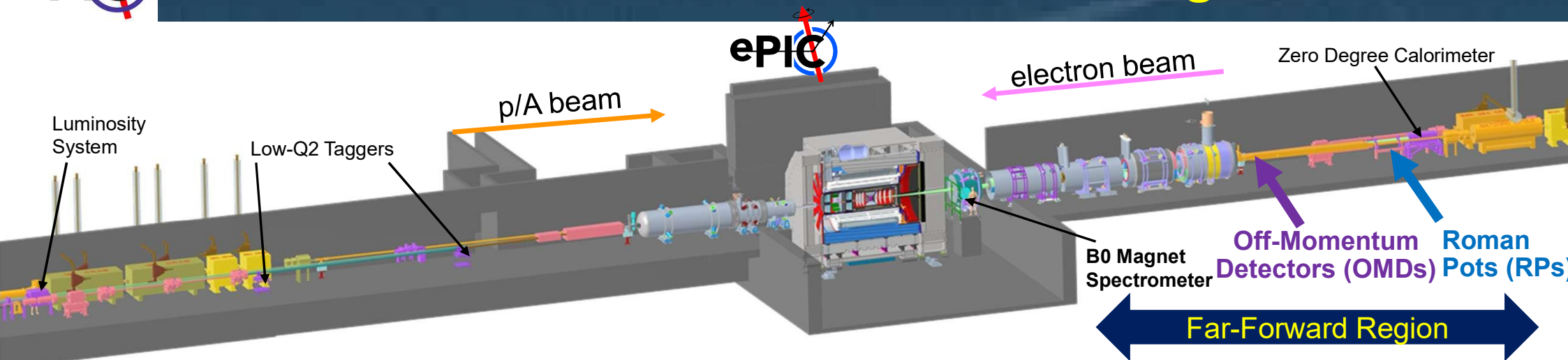
5th IWEQCD CAS 2 july 2026

F. Bouyjou, H. Chanal, F. Dulucq, M. El Berni, S. Extier, M. Firlej, T. Fiutowski, K. Guillosoy, F. Guilloux, M. Idzik, N. Kachkachi, B.-Y. Ki, C. de La Taille, J. Moron, D. Marchand, L. Royer, N. Seguin-Moreau, L. Serin, A. Shama, A. Soulier, K. Swientek, D. Thienpont, A. Verplancke

Organization for Micro-Electronics design and Applications



ePIC Detectors & Far-Forward Region



Far-Forward detectors are **essential** to measure **exclusive processes**, as Deep Virtual Compton Scattering (DVCS) → Generalized Parton Distributions (GPDs)

❖ Roman pots (RP)

- Detect particles scattered at very small angle (< 5 mrad)
- Required to measure exclusive processes on proton targets
 - DVCS, DVMP...
 - All the channels relevant to GPDs of quarks and gluons

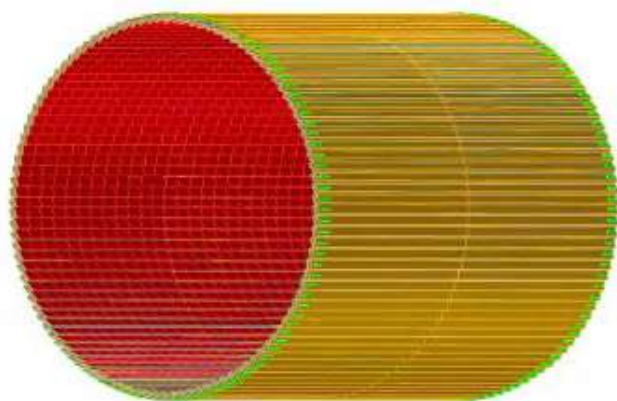
❖ Off-Momentum Detectors (OMD)

- Detect small angle particles with a different rigidity than the beam
 - Access angles down to 0 for rigidity < 0.65
- Necessary for all tagged measurements
 - Study of nuclear effects
 - Effective neutron target

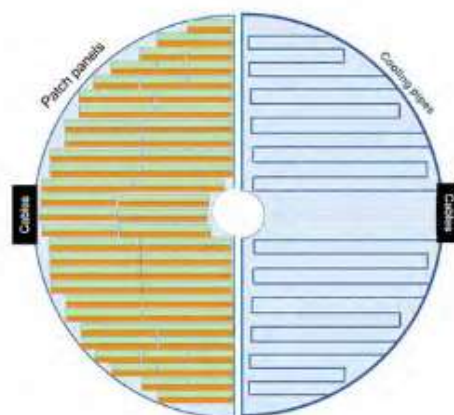
ePIC AC-LGAD detectors

Specifications of ePIC AC-LGAD detectors:

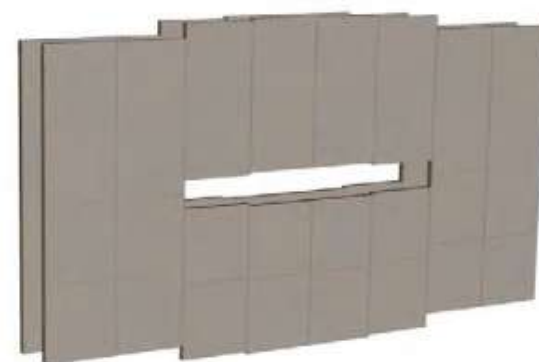
BToF



FToF



Roman Pots



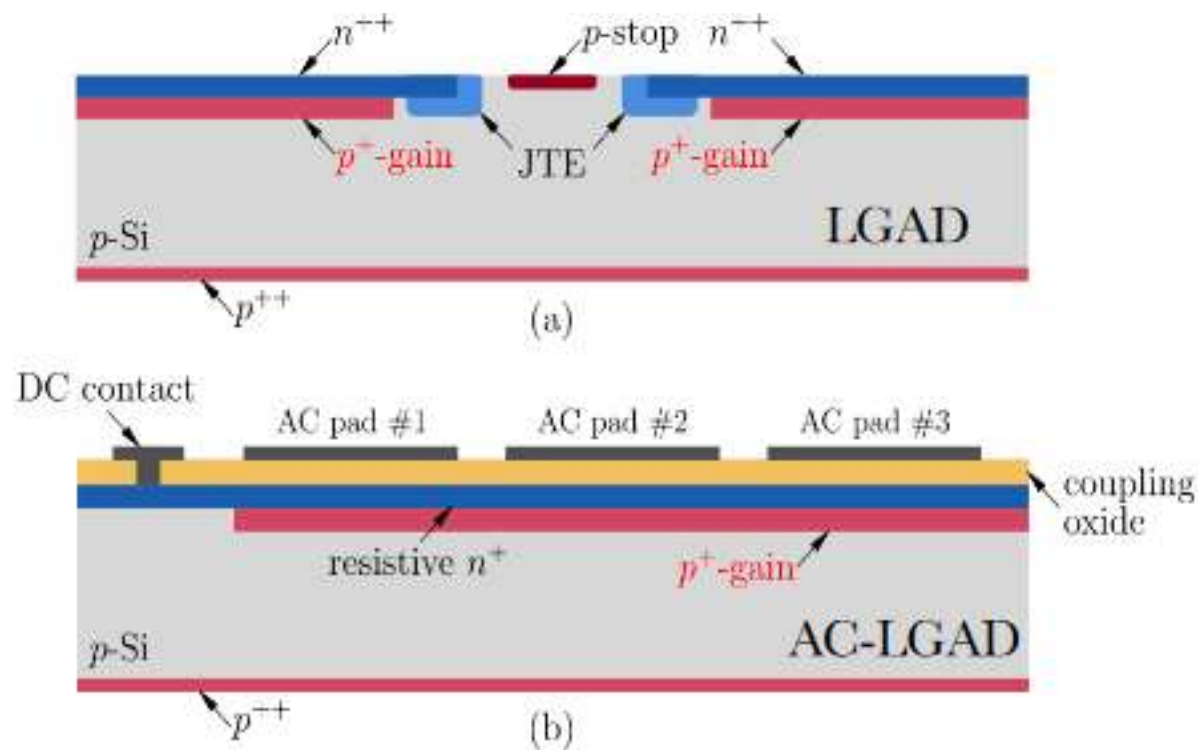
4D Trackers

	Area (m ²)	Channel size (mm ²)	# of Channels	Timing Resolution	Spatial resolution	Material budget
Barrel TOF	10.9	0.5*10 (strips)	2.4M	30 ps	30 μm in φ	0.01 X0
Forward TOF	2.22	0.5*0.5 (pixels)	8.8M	25 ps	30 μm in x and y	0.08 X0
B0 tracker	0.07	0.5*0.5 (pixels)	0.28M	30 ps	20 μm in x and y	0.05 X0
RPs/OMD	0.14/0.08	0.5*0.5 (pixels)	0.56M/0.32M	30 ps	140 μm in x and y	no strict req.

DC LGAD and AC LGAD

From S. Nanda : <https://indico.cern.ch/event/1232761/contributions/5321425/>

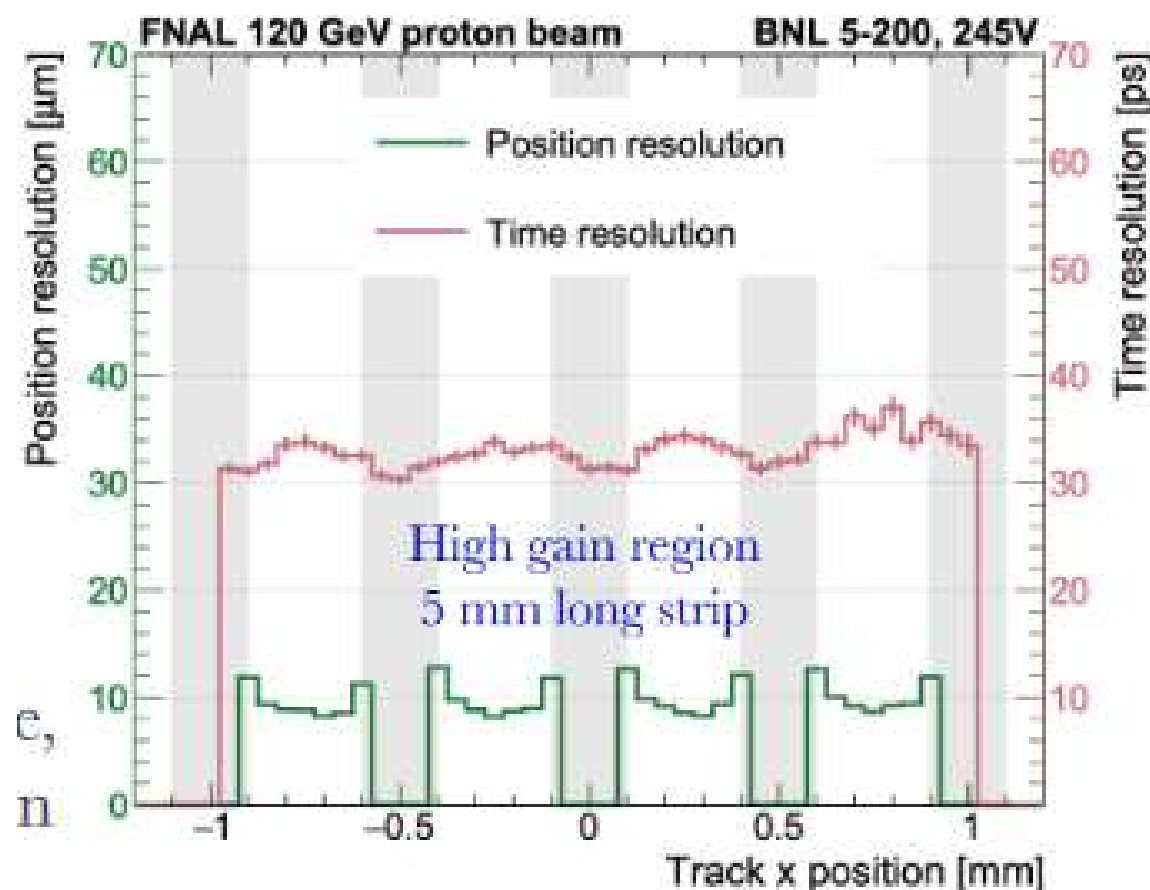
- MIP timing detectors (HGTD, ETL) use DC LGAD sensors
 - ~ 10 fC/MIP
 - Area : $(1.3 \text{ mm})^2$
 - Good timing resolution : 30-50 ps
 - Poor position resolution : $\sim 400 \mu\text{m}$
 - « dead zone » between pixels
- AC LGADs for EIC
 - Resistive layer to get signal sharing
 - Area $(500 \mu\text{m})^2$
 - Good position resolution : $< 50 \mu\text{m}$
 - No dead area
 - Good timing resolution (as DC LGAD)



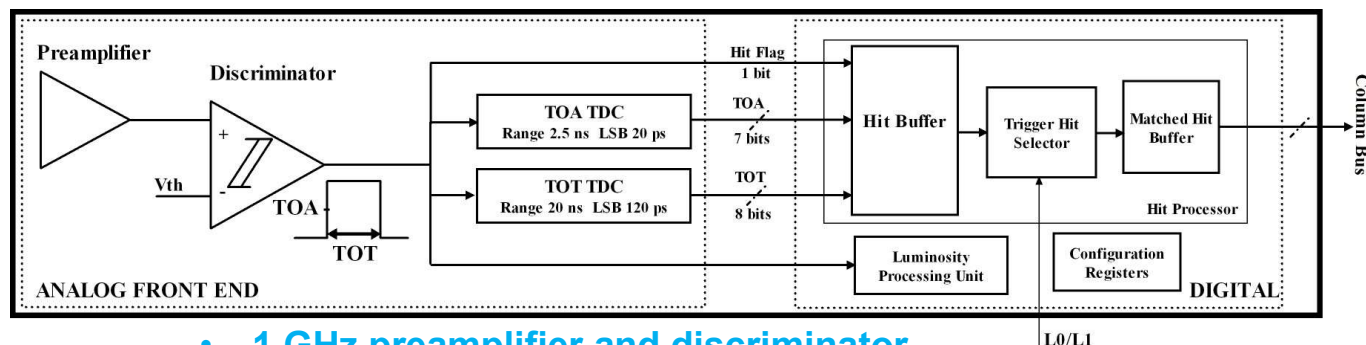
AC LGAD performance [FNAL]

From S. Nanda : <https://indico.cern.ch/event/1232761/contributions/5321425/>

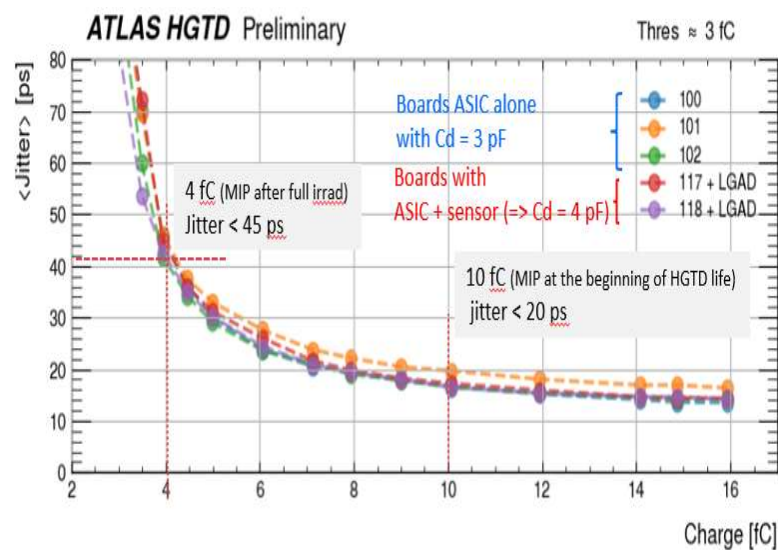
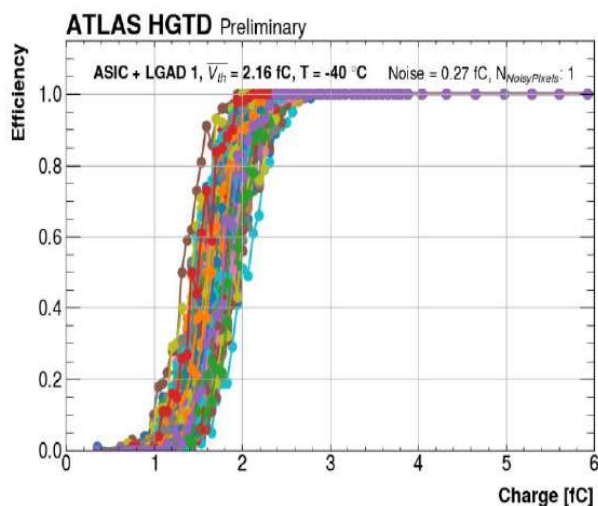
- Here for strips : 500 μm x 5 mm
 - ~30-35 ps timing resolution
 - ~10 μm position resolution
 - Oscilloscope readout
 - Still preliminary results and improvements underway on gain uniformity
 - Chosen as baseline for several EIC detectors
- New and promising detector
 - Need readout chip
 - Strips (see next talk by A. Apresyan)
 - Pixels 500 μm x 500 μm : EICROC



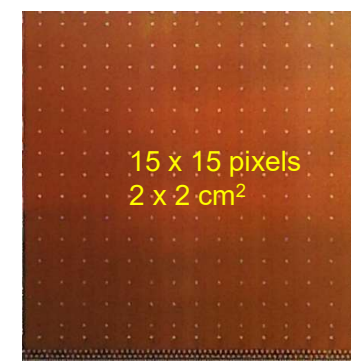
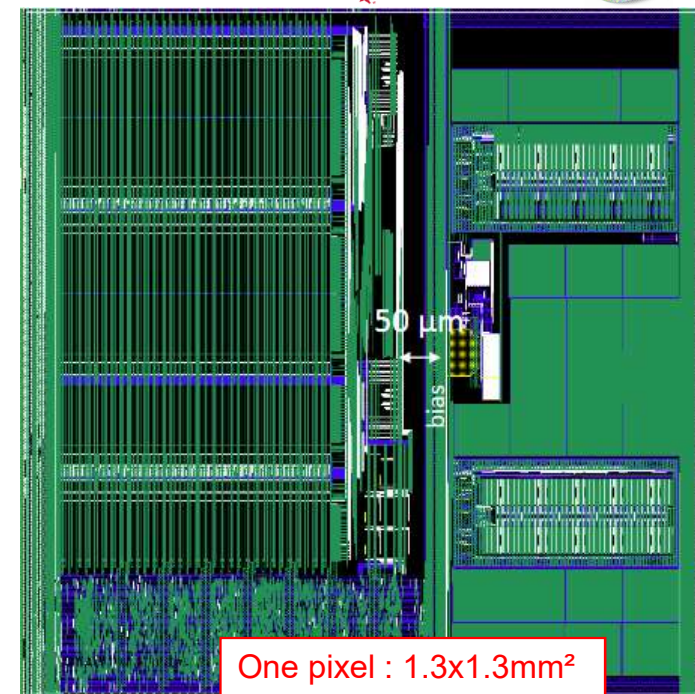
ALTIROC : DC-LGAD readout chip



- 1 GHz preamplifier and discriminator
- 2 vernier TDCs for ToA and ToT
- Hit buffer: SRAM 1536 x 19 bit (38 μ s latency)

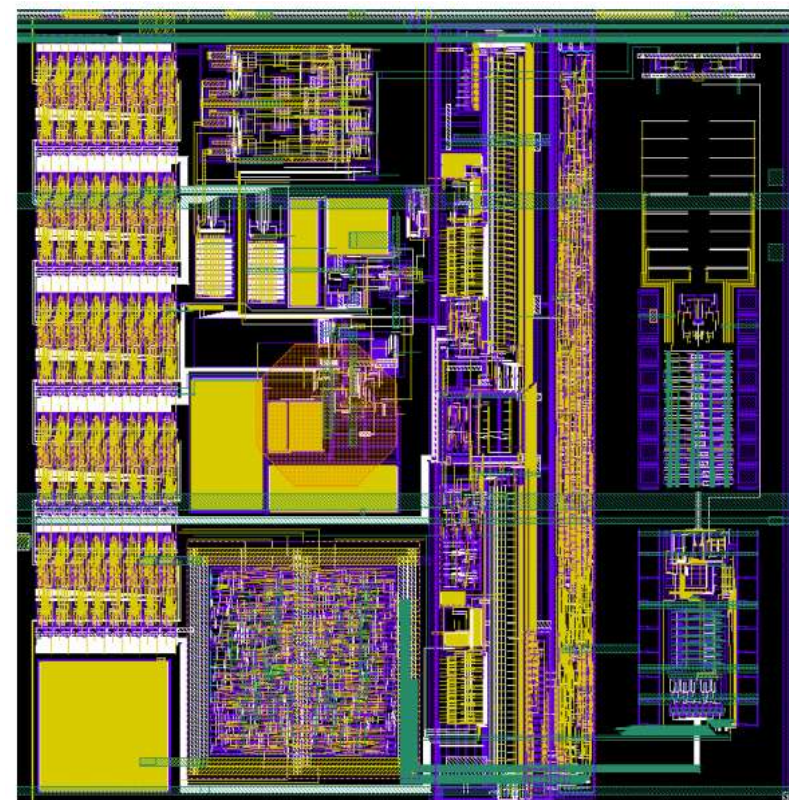


CdLT EICROC2 july 2026



EICROC0

- Analog frontend similar to ATLAS ALTIROC
 - $C_d = 1$ pF (max 3 pF)
- **Need ADC instead of ToT** for charge measurement : 8bit 40 MHz from AGH Krakow
- TDC taken from HGCROC by CEA Saclay
- Simple digital readout but SEE-proof I²C slow control
- ~2 mW/pixel
- Fabricated in spring 2022 in TSMC 130nm



 **OMEGA**
Microelectronics

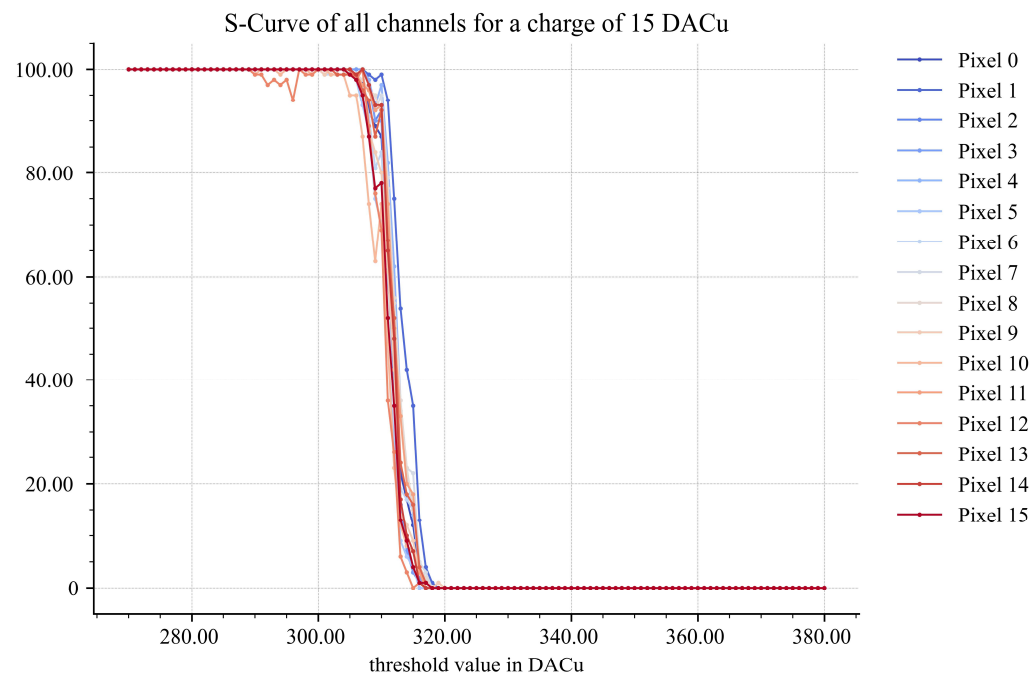
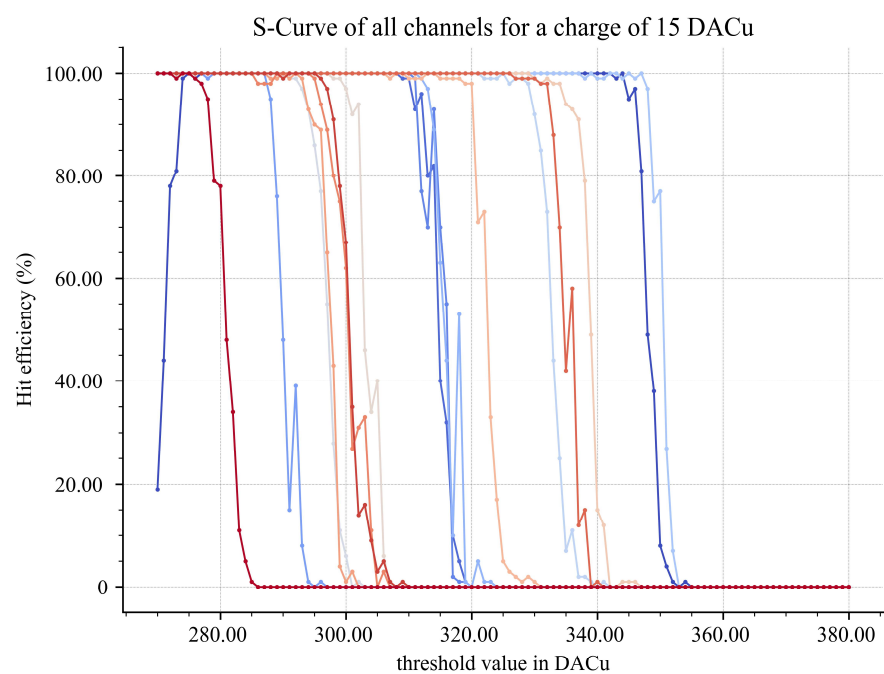
 **Lrfu**

 **AGH**

CdLT EICROC2 july 2026

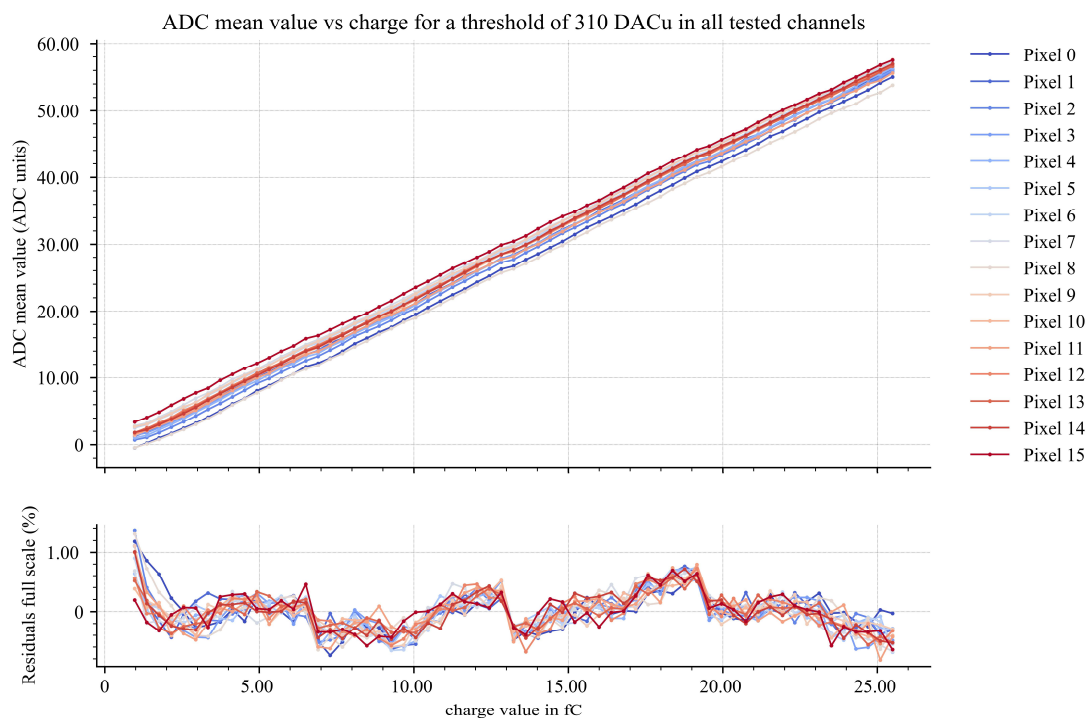
- 6-bit DAC for channel-wise threshold alignment

Correction of channels for a charge of 5 fC (ASIC alone)

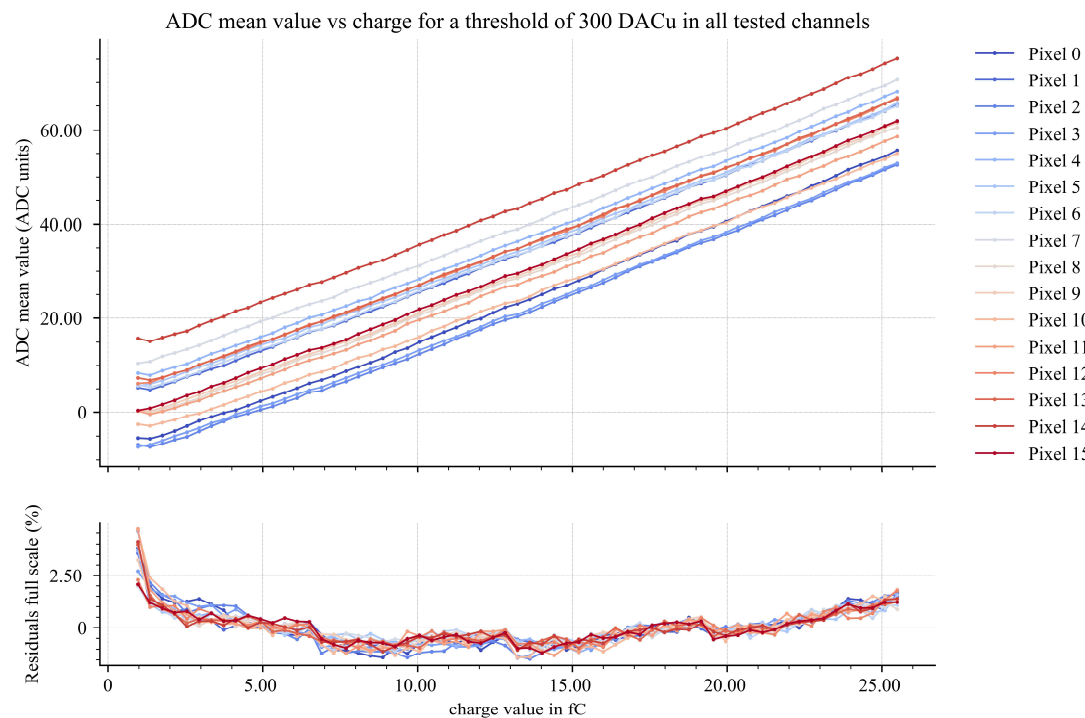


- 8 bit 40 MHz SAR ADC [Krakow]
 - Noise ~1 UADC but large common mode noise (here subtracted)
 - Signal 50 UADC ~500 μm $\Rightarrow$ 1 UADC ~10 μm

ADC mean & residuals – no sensor

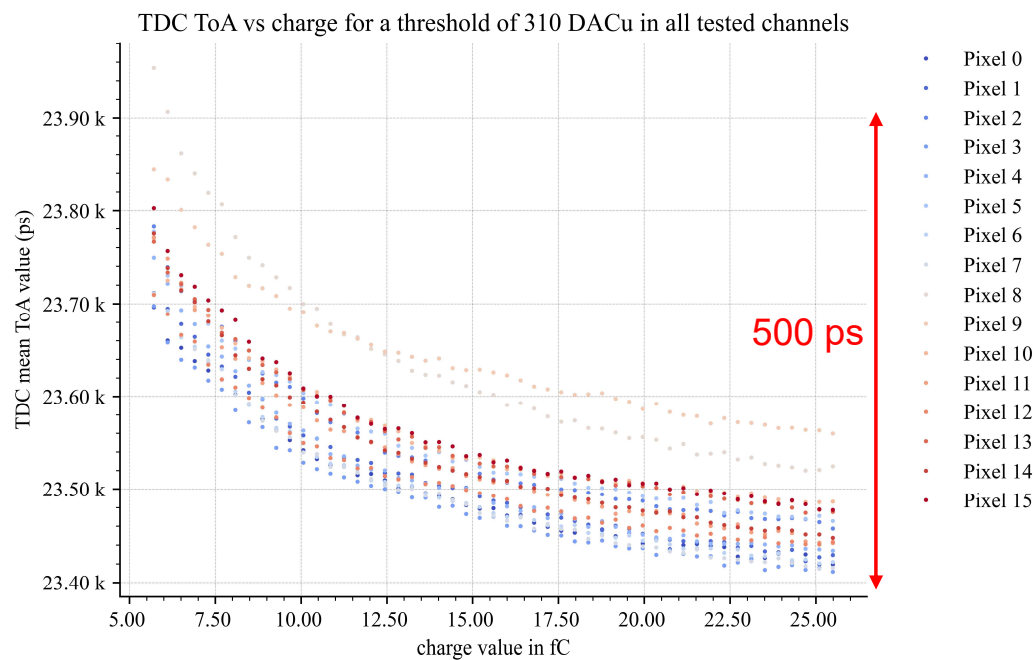


ADC mean & residuals – BNL Flipchip sensor

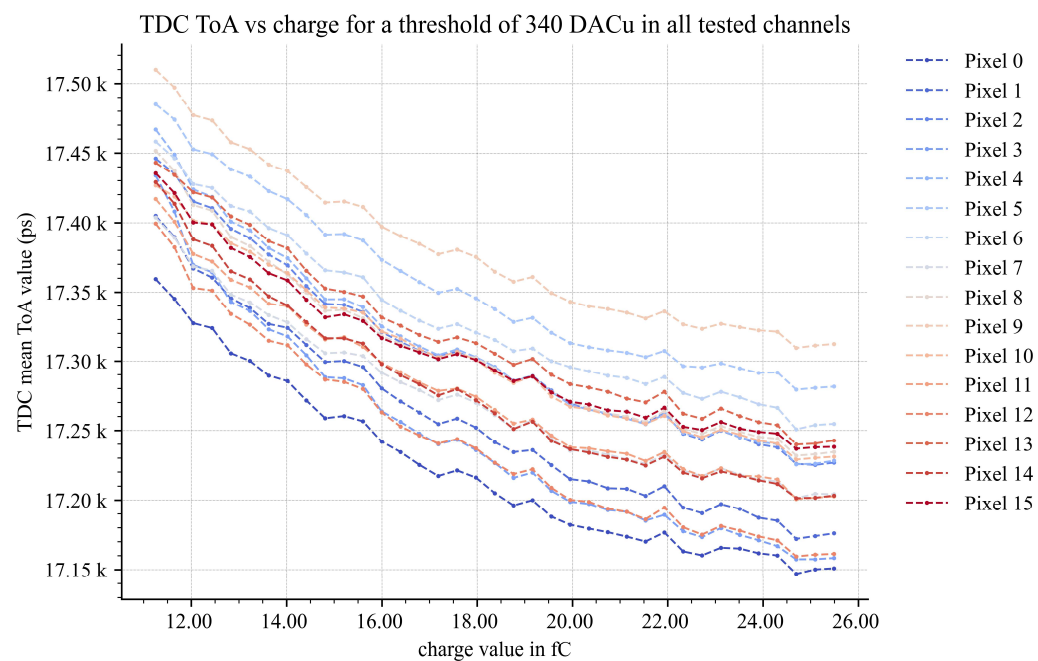


- Time walk measurement : ~400 ps

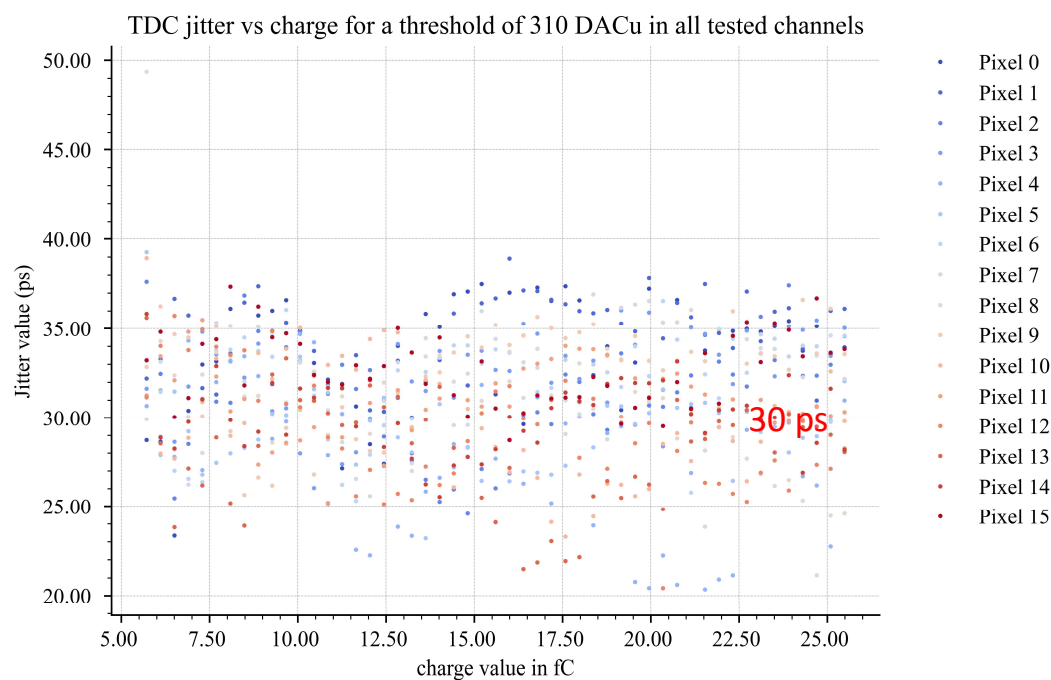
TDC ToA – no sensor



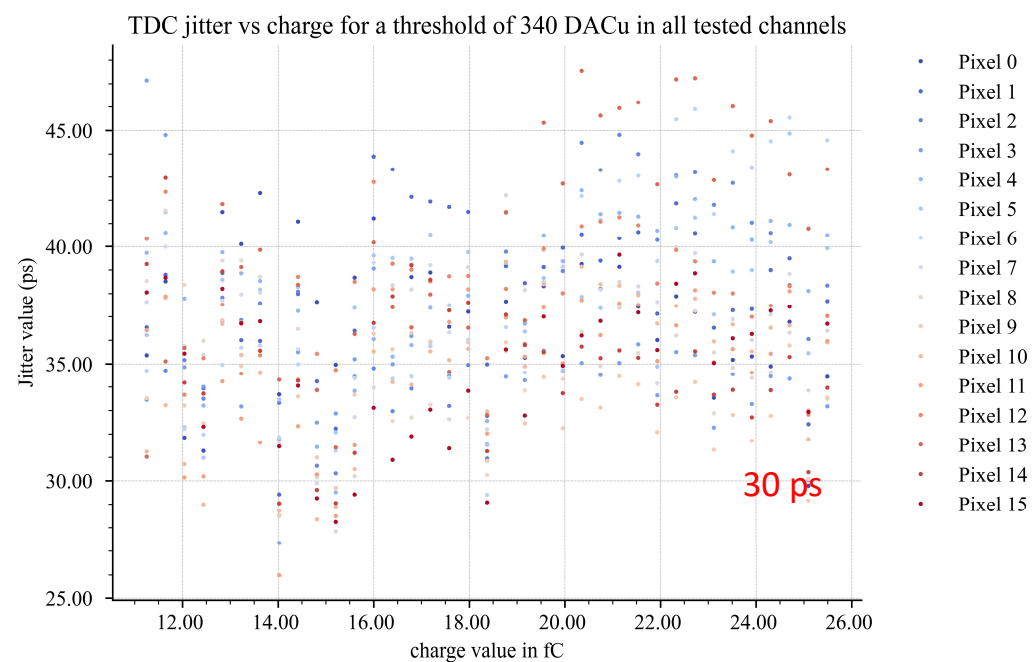
TDC ToA – BNL Flipchip sensor



TDC jitter – no sensor



TDC jitter – BNL Flipchip sensor

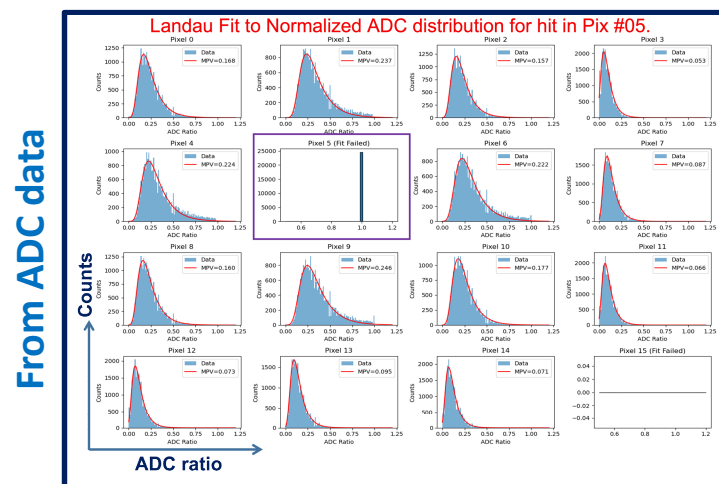
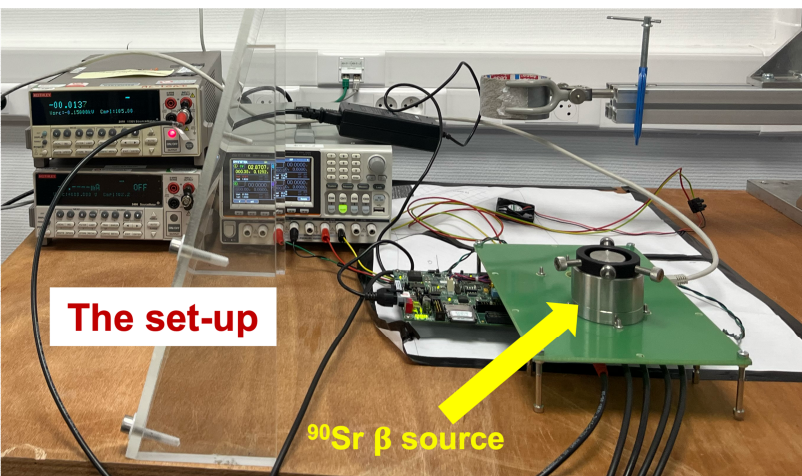


Charge range degraded with sensor, still need to properly calibrate the TDC for each channel and remove correlated noise

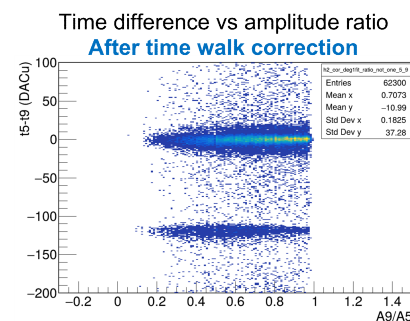
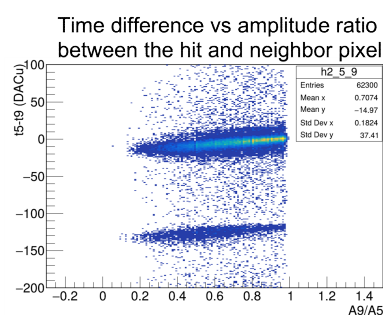
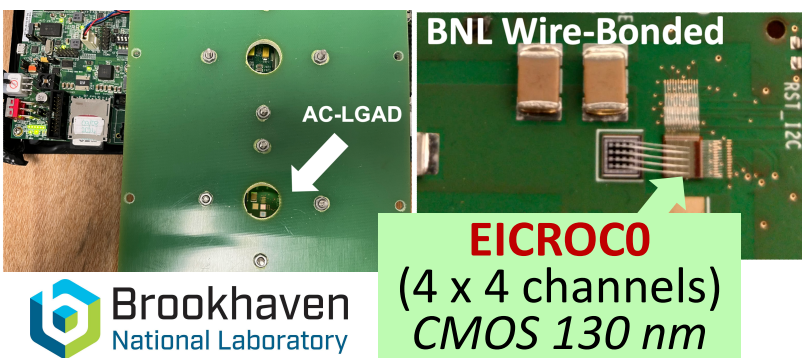
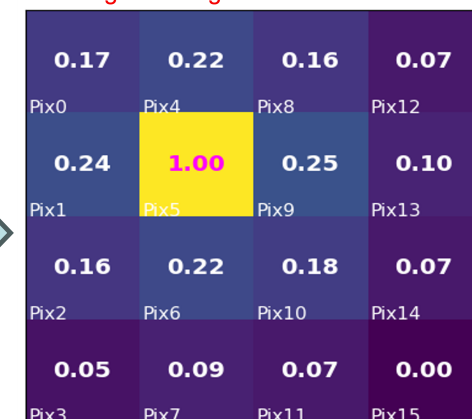
Pixelated AC-LGAD read-out characterization

Measurements with ^{90}Sr β source at IJCLab PSI platform (July '25)

1) digital data stored when the PreAmp signal amplitude of at least 1 channel among the 16 is passing the discriminator threshold



Charge Sharing ratio for hit in Pix #05



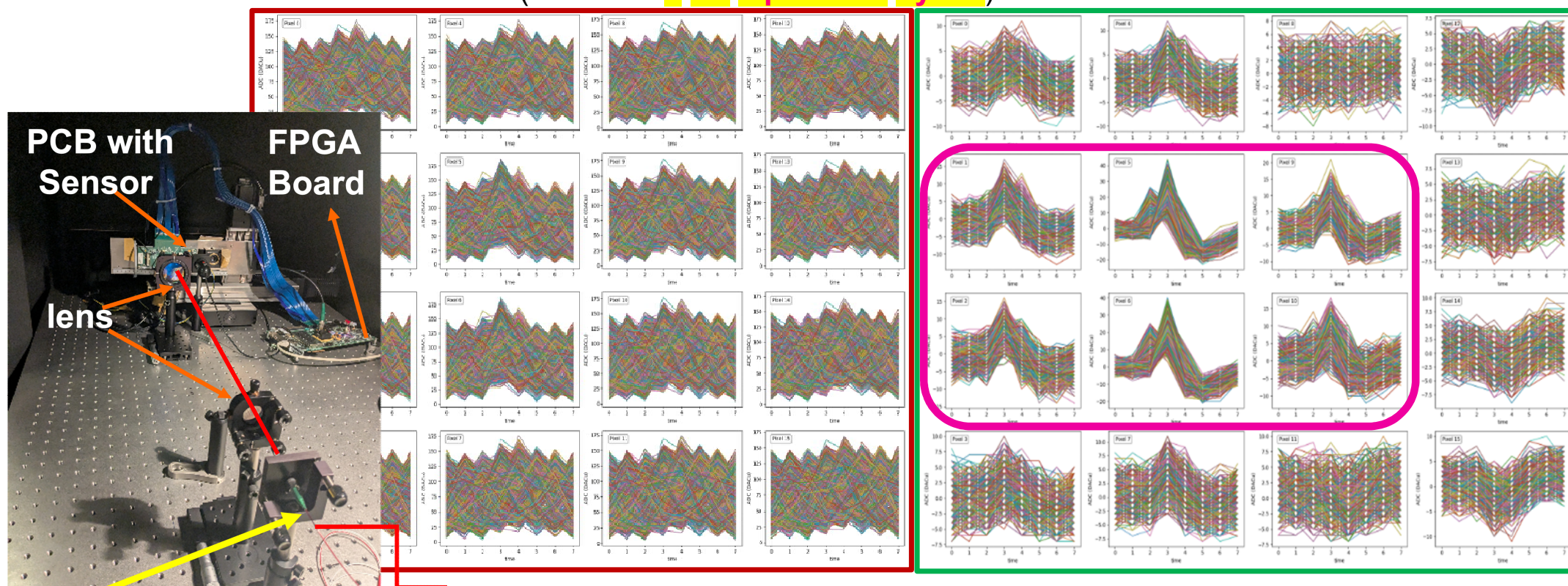
- ADC pedestal subtraction computed from "far" pixel
- More charge sharing (~23%) for adjacent neighbors
- Time walk correction applied successfully to TDC data

A. Sharma, B.-Y. Ky, D. Marchand, L. Serin

Pixelated AC-LGAD read-out characterization

Preliminary results with Infrared Laser (1/2)

ADC waveforms (8 time samples = 8 points/event): **BEFORE** & **AFTER** pedestal subtraction
(based on « far » pixel evt by evt)



Pulsed Infrared laser λ 1056 nm

A. Sharma & D. Marchand

CDLT EICROC2 July 2026

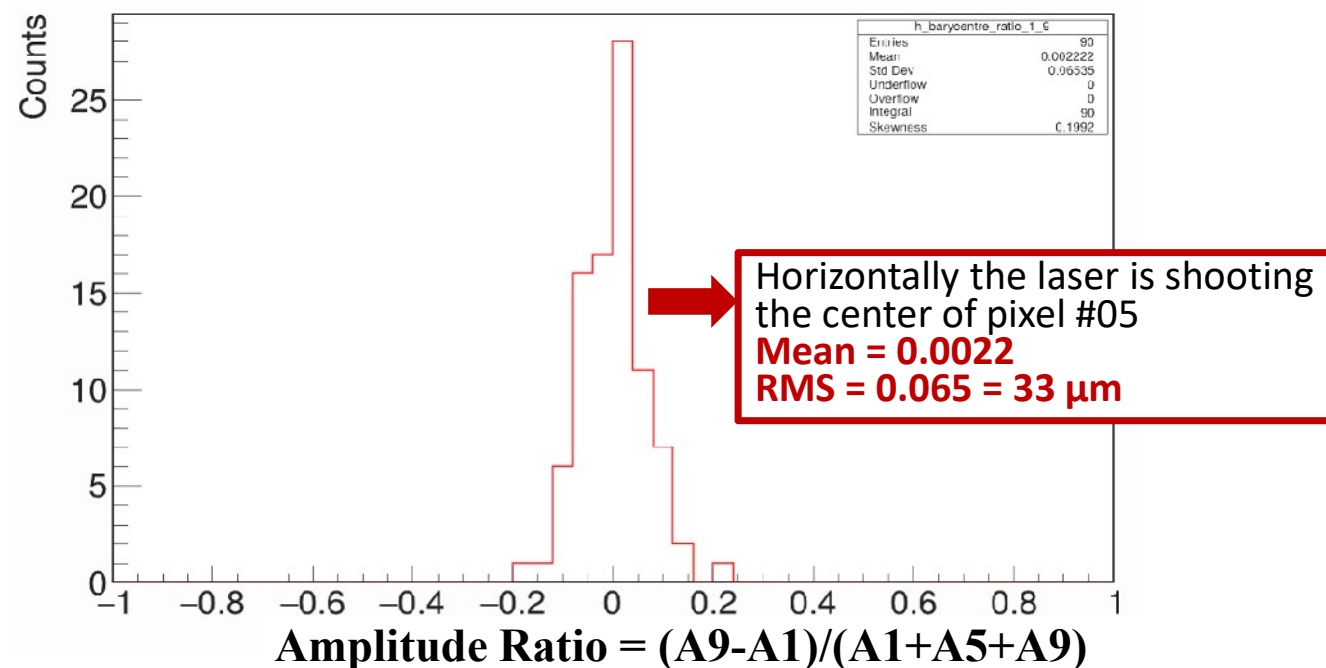
Pixelated AC-LGAD read-out characterization

Preliminary results with Infrared Laser

Barycenter calculation from ADC data

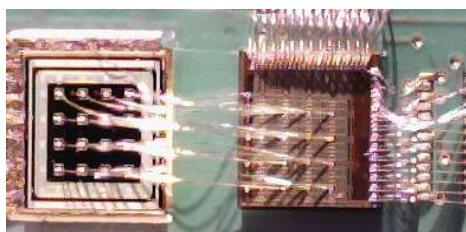
Considering pixels #01, #05 & #09

Pixel / Channel Mapping	Column 0	Column 1	Column 2	Column 3
Line 0	Pixel (0,0) #00	Pixel (1,0) #04	Pixel (2,0) #08	Pixel (3,0) #12
Line 1	Pixel (0,1) #01	Pixel (1,1) #05	Pixel (2,1) #09	Pixel (3,1) #13
Line 2	Pixel (0,2) #02	Pixel (1,2) #06	Pixel (2,2) #10	Pixel (3,2) #14
Line 3	Pixel (0,3) #03	Pixel (1,3) #07	Pixel (2,3) #11	Pixel (3,3) #15



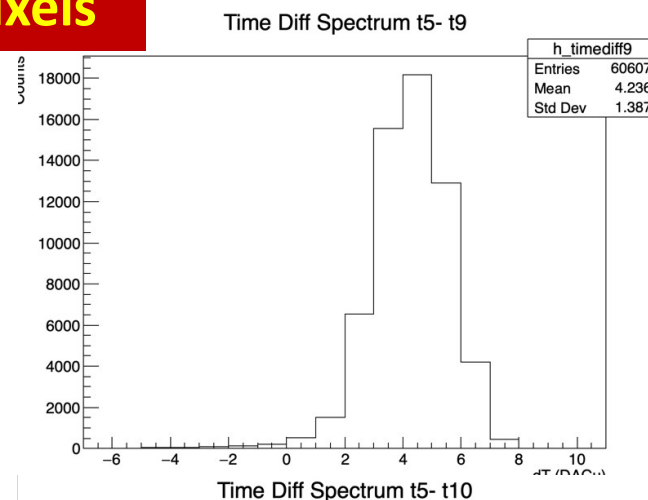
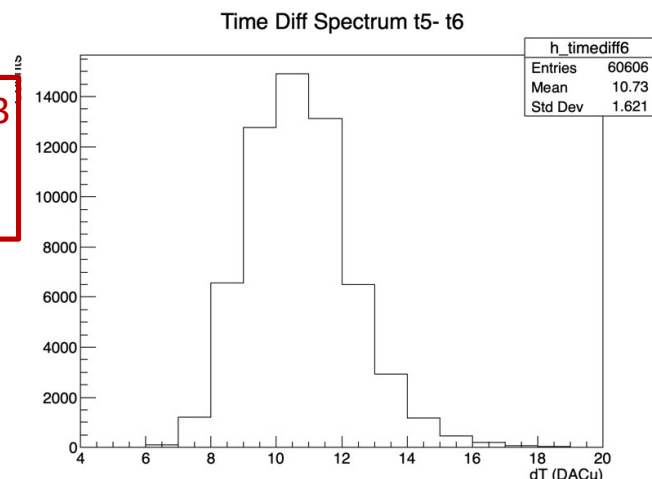
Pixelated AC-LGAD read-out characterization With Infrared Laser

TDC differences between 2 hit neighboring pixels

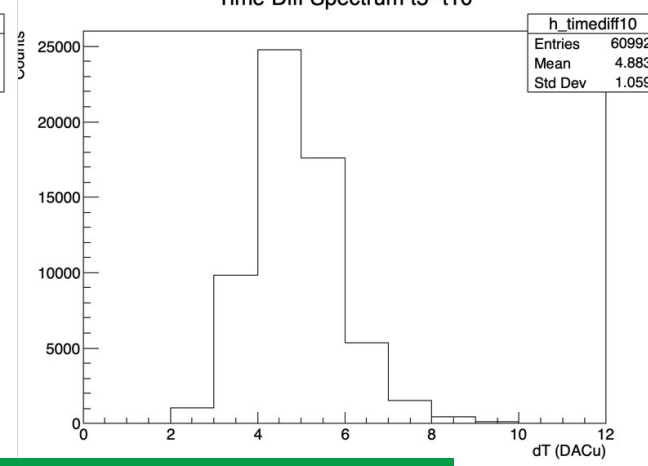


BNL sensor biased at HV = -190V

$\sigma [\text{pix05} - \text{pix06}]_{\text{DACu}} = 1.623$
→ TDC jitter for individual pixel [= $\sigma / \sqrt{2}$]: **28.7 ps**



$\sigma [\text{pix05} - \text{pix09}]_{\text{DACu}} = 1.387$
→ TDC jitter for individual pixel [= $\sigma / \sqrt{2}$]: **24.5 ps**



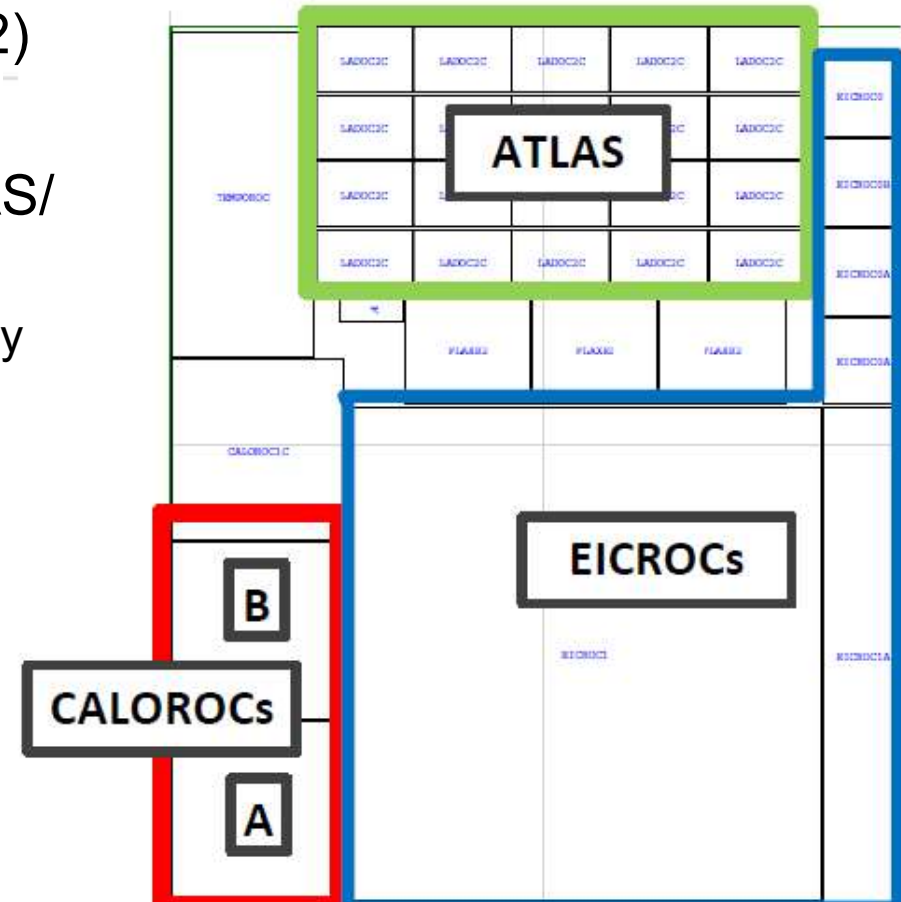
$\sigma [\text{pix05} - \text{pix10}]_{\text{DACu}} = 1.059$
→ TDC jitter for individual pixel [= $\sigma / \sqrt{2}$]: **18.7 ps**

Individual Pixel jitter from 19 ps up to 29 ps

Call EICROC2 July 2026

EICROC prototypes

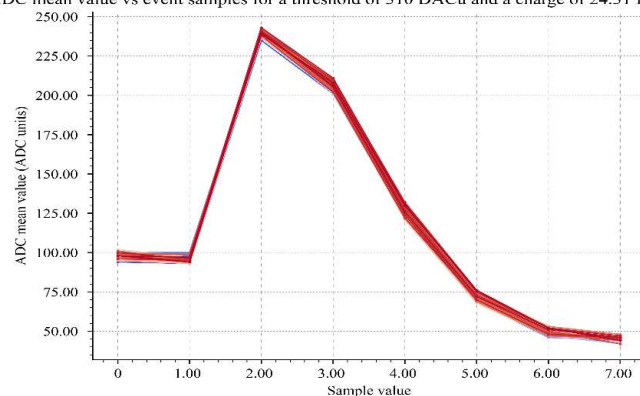
- EICROC0 : 4x4 pixels with simple readout (2022)
- EICROC OA/0B 1/1B fabricated in 2025 « ATLAS/EIC » engineering run TSMC 130n
 - EICROC0A/B : 4x4 with improved blocks and testability
 - EICROC1/1A : 32x32 and 4x32
- EICROC2 will be fabricated Q1 2027
 - Should be the final chip...



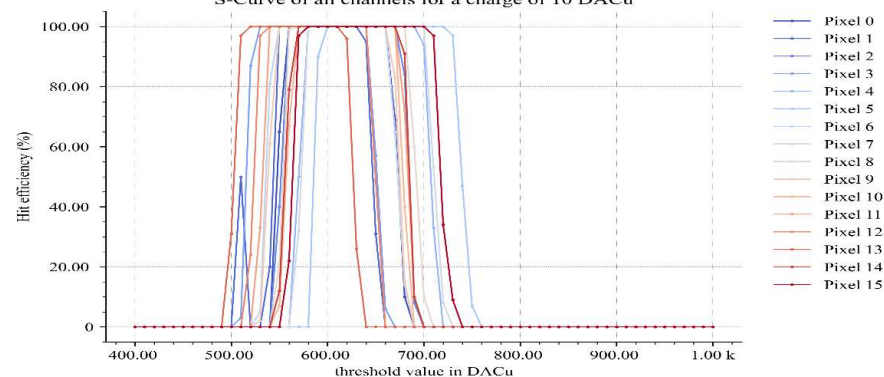
First measurements of EICROC0A

- Only partial configuration is possible : look at ADC data and s-curves
 - Improved ADC baseline, similar minimum threshold (3 fC)

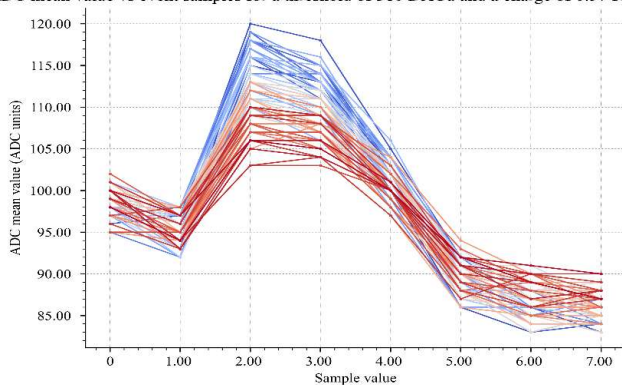
ADC mean value vs event samples for a threshold of 310 DACu and a charge of 24.31 fC in channel 1



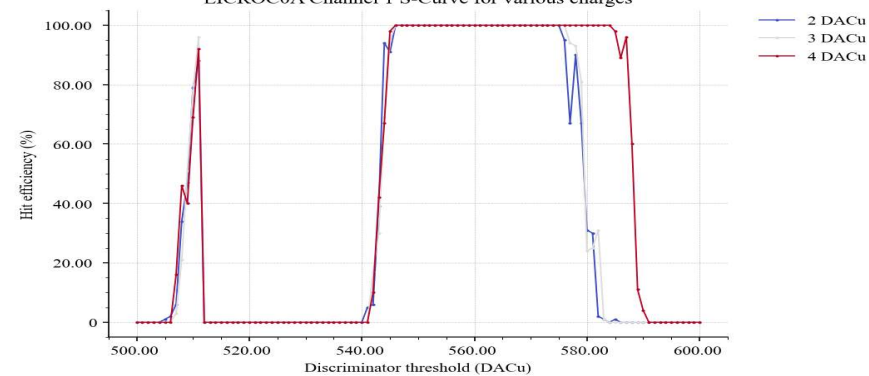
S-Curve of all channels for a charge of 10 DACu



ADC mean value vs event samples for a threshold of 310 DACu and a charge of 0.57 fC in channel 1

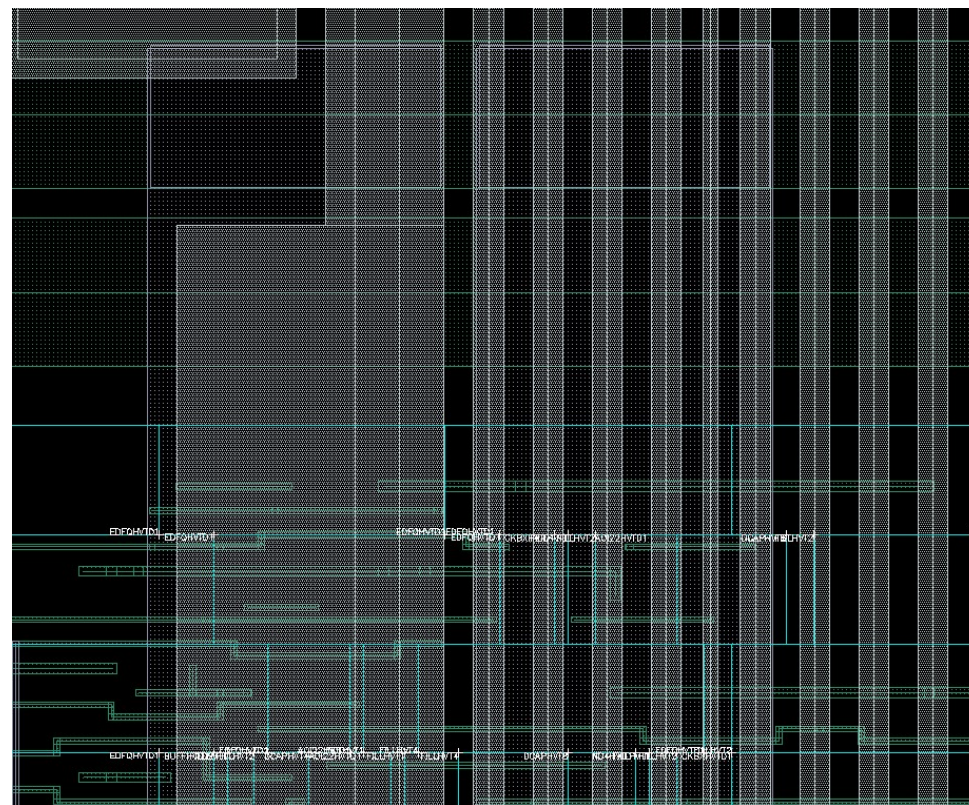


EICROC0A Channel 1 S-Curve for various charges



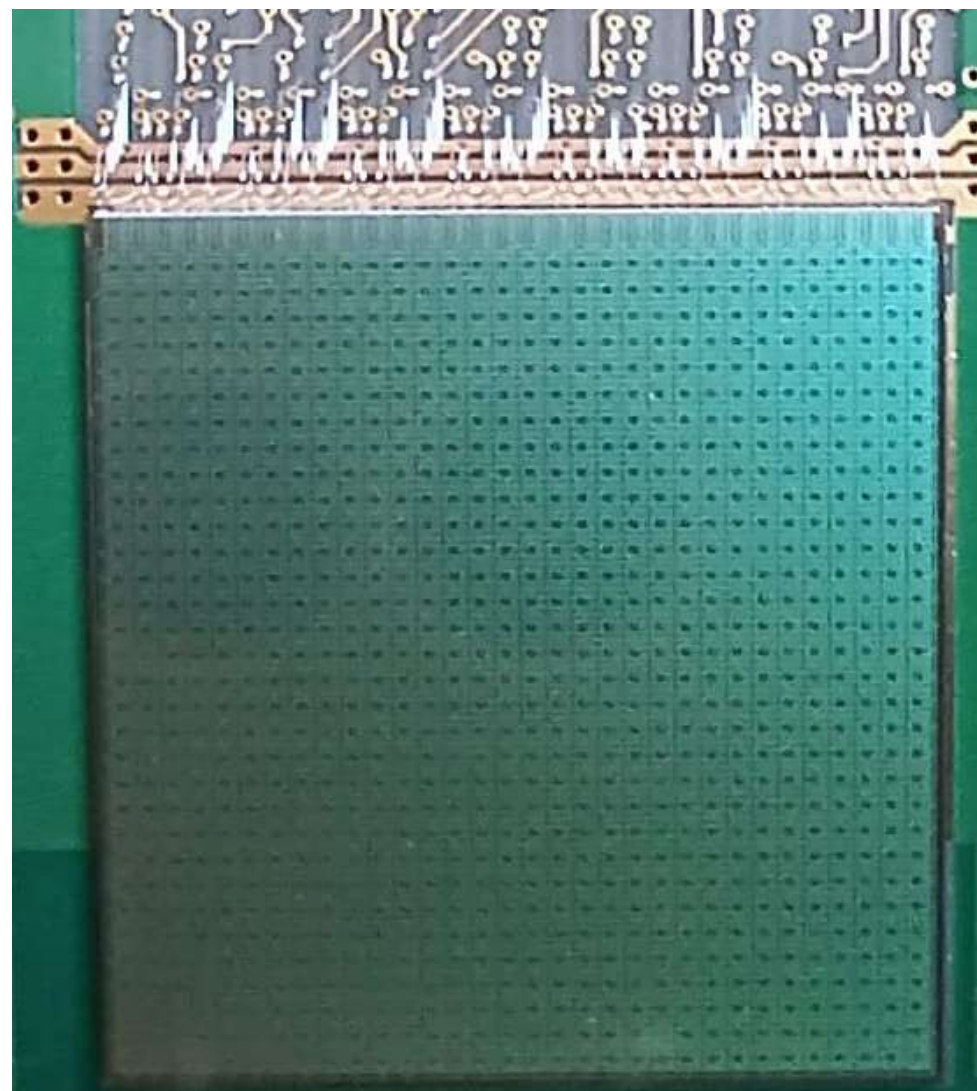
EICROC0 Coupling investigation

- Large coupling seen on the ADC data which was completely hiding the signal up to 20 fC
- Large coupling capacitance between local (pixel) digital block and preamp / shaper bias lines
- Layout improved by adding exclusion zones and a shield between bias lines and digital



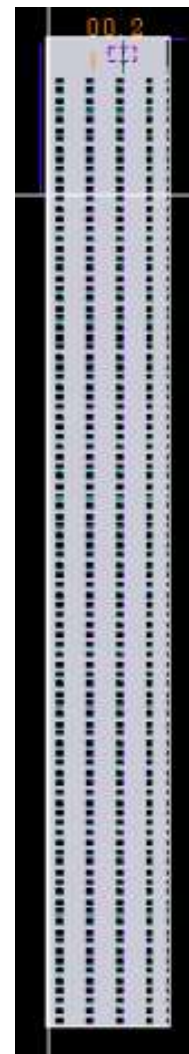
Bias / digital block layout in new EICROC ASICs

- 32x32 chip : final dimensions
- Goal :
 - test full-scale chip analog performance (IR drops)
 - Allow final sensor characterization
 - Test interface with DAQ : fast commands and 320 Mb/s data output
 - Progress on module/front-end boards
- Caveats :
 - Not (yet) zero-suppressed data
 - Still 2mW/ch
 - Still analog-on-top

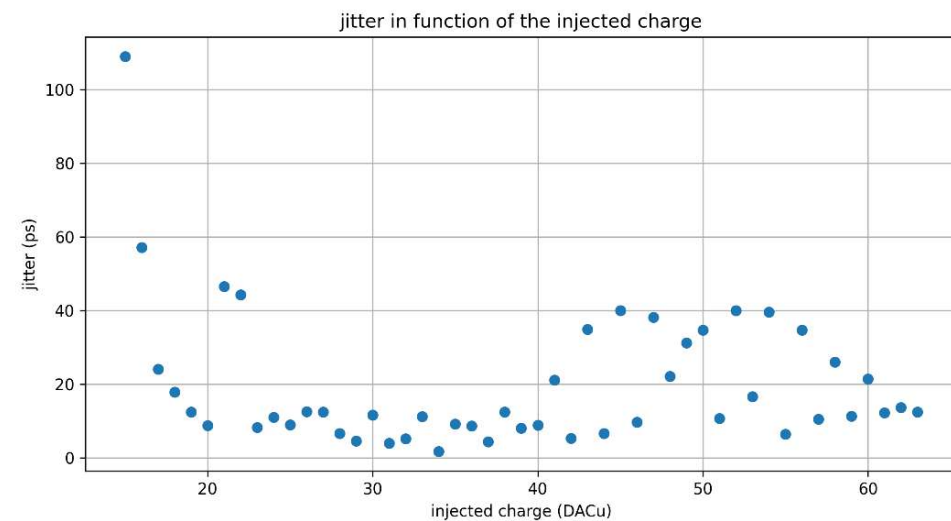
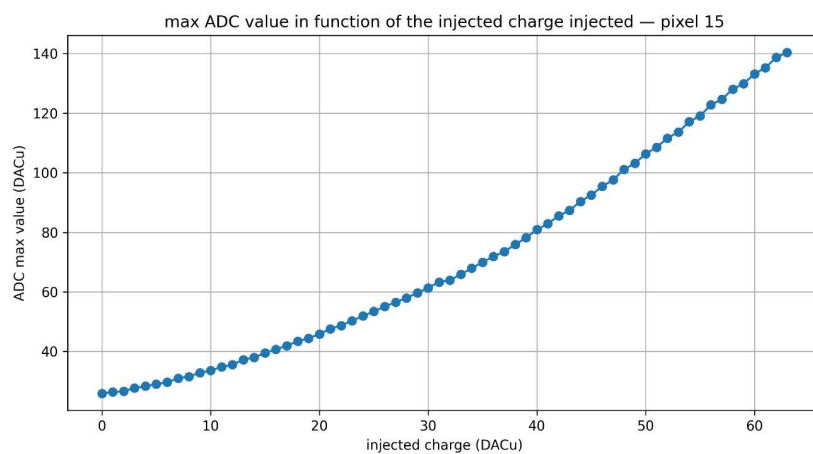
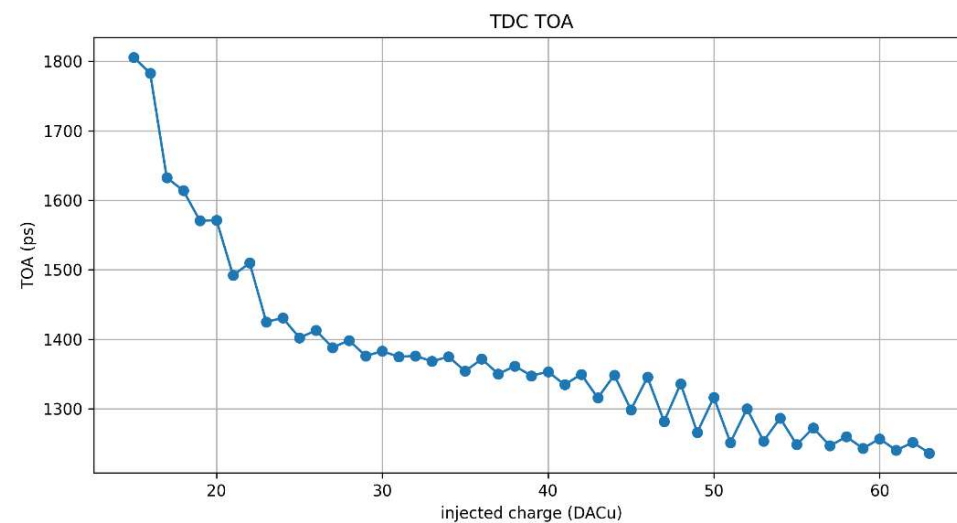
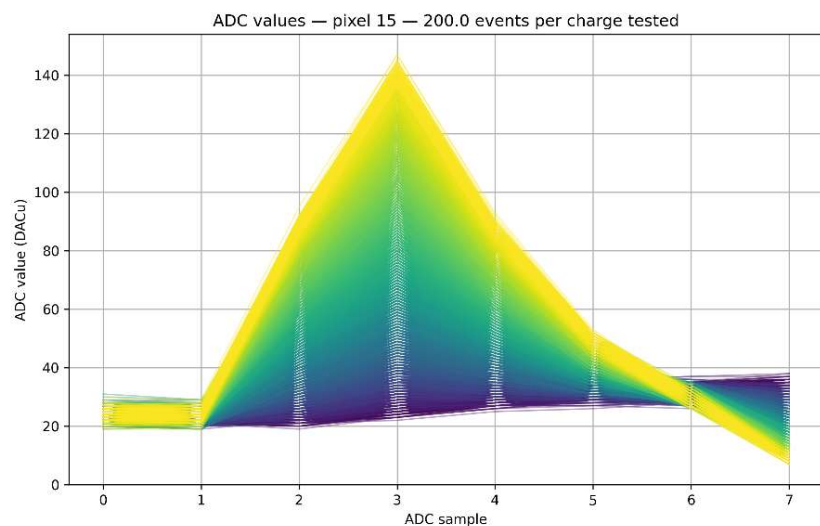


EICROC1 description

- Designed as 8 blocks of 4x32
 - Read out sequentially, like EICROC0
 - Pixel similar to EICROC0A
 - 8 CLPS outputs at 40 MHz
 - Clock tree for isochronous calib_pulse distribution
- Common balcony (End of column)
 - Biases and slow control
 - **New : fast command** decoder (clock, calib_pulse, enable_acquisition, start_readout)
 - Backup clock and cmd_pulse inputs available
 - 320 MHz serializer for 1 CLPS output : to be used for system tests



First measurements of EICROC1 ADC&TDC



next EICROC2 (2027)

- What is missing in EICROC1 ?
 - Larger rate compatibility ?
 - Derandomizer for successive events (how many ?)
 - Digital on Top (DoT) design for digital power reduction and timing verification on large area : more powerful tools available (UVM)
 - Auto-trigger and zero_suppressed data
 - Power reduction if possible below 2 mW/ch
- Clermont Ferrand lab has joined to take responsibility for the DoT
 - Already participated in ATLAS ALTIROC
 - The design and verification should take ~9 months from now
- Technology choice
 - Seems to converge to 130nm provided rate remains low enough

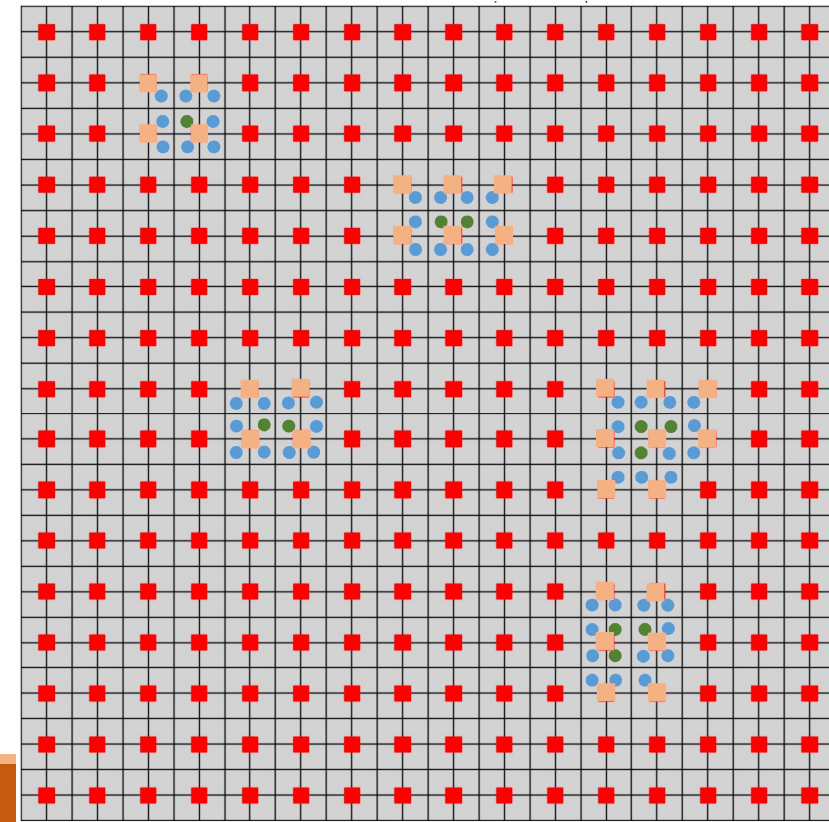


- Goals
 - Less digital logic possible inside pixel/matrix
 - Less signals possible between matrix and periphery
 - Triplication of sensitive circuits (configuration registers for example)
 - No triplication on data path
 - Complexity on periphery side, simple logic inside pixel
- Proposal : **Based on clusters of 4 pixels, controlled by the periphery**
 - Some logic shared at cluster level
 - Shared data bus between 2 columns

First iteration of this architecture is ready at RTL level, some debug in progress

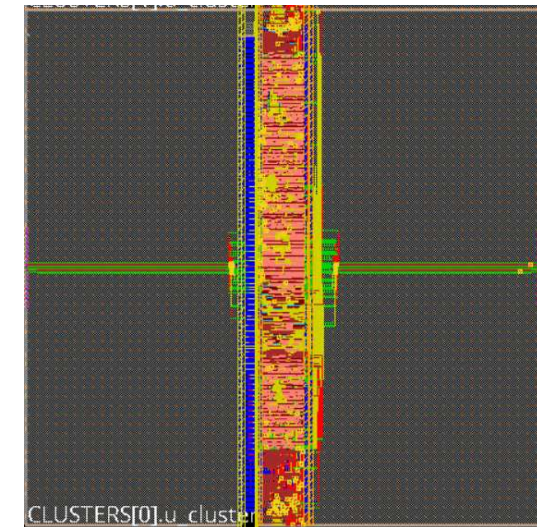
➔ Physical implementation can reveal new constraints, architecture may change

- Triggered Pixel (TP)
- Neighbor pixel (TL1)
- Busy cluster
- Cluster waiting for hit

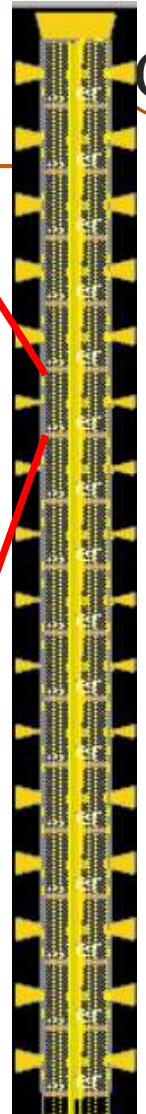


Physical implementation

- First physical implementation done in **130nm**
 - Check if we manage to fit digital readout inside pixel
- Preliminary layout of the cluster of 4 pixels and the column
- Triplication of cluster (probably need some refinement)
- Using a pixel_analog_dummy macro, not the real analog front-end
- **Need more time to validate that this architecture can fit using 130nm technology**



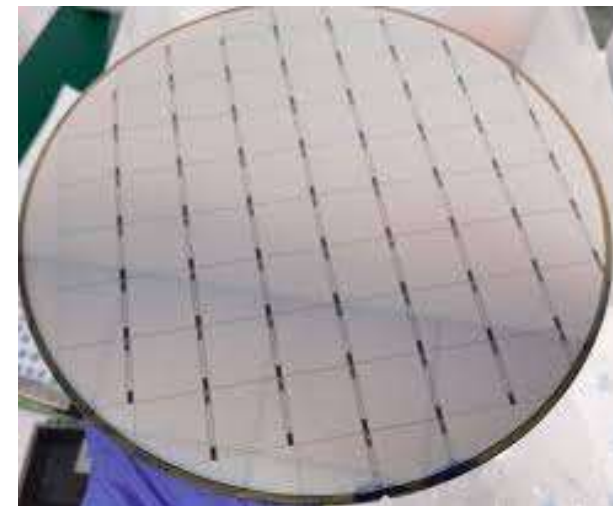
Cluster of 4 pixels



Double column

Path towards production and QC

- For roman pots ~500 chips would be needed (500 k ch) = 6 wafers
- For FToF 10k chips ~100 wafers
- EICROC2 should be a final version (all features implemented)
 - Schedule accomodates a possible EICROC3 to fix bugs in EICROC2
 - ~1 year after EICROC2 tests and system tests complete
- Wafer probing station and test setup will be needed
 - Can be inspired from ALTIROC setup

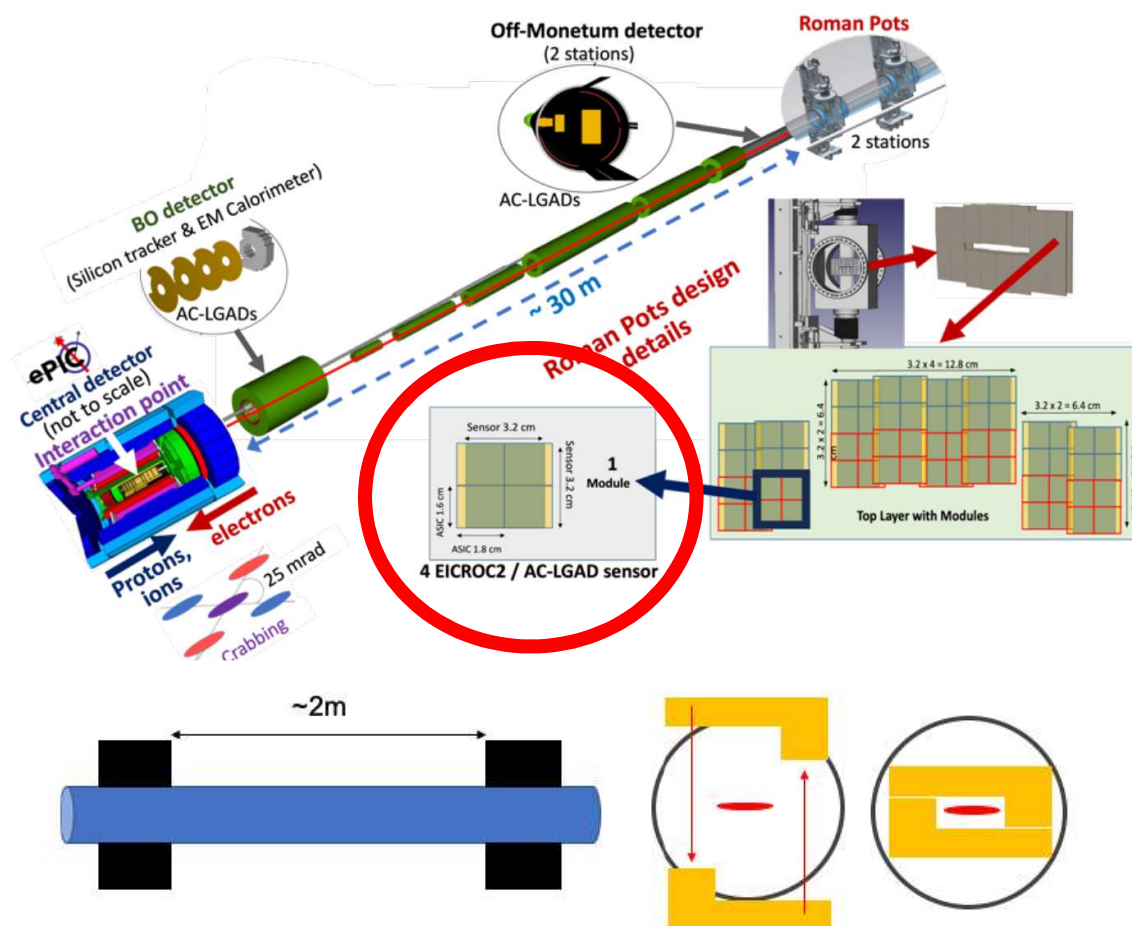


summary

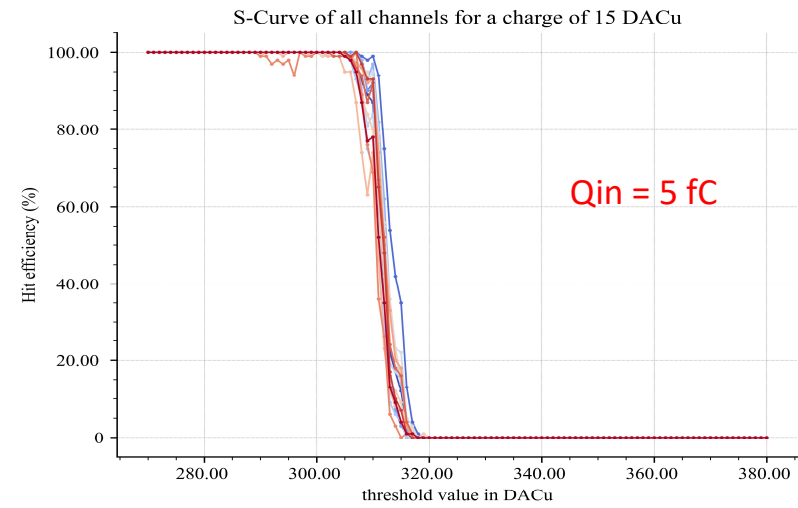
- EICROC now reached full scale 32x32 with EICROC1
 - Important for analog performance and sensor test
 - Also allows to progress on system design
- Small scale EICROC0s 4x4 still under test to improve performance and reduce power
 - Tests to start soon with sensors
- EICROC2 now needs its digital design DoT : ~6 months design time from now
 - Responsibility of Clermont Ferrand lab
 - Main driving specification is power minimization and low hit rate (< 100 Hz/pixel)
 - Submission in Engineering run in TSMC130n Q1 2027
- System tests will be (as always) an important input for chip(s) finalization

ePIC experiment far-forward region

- Roman Pots for ePIC experiment
 - Used in the far forward tracking of particle collisions, mandatory for exclusive reactions
- 2 stations ~2m apart
 - 2-3 layers of sensors per station
 - Square pixels of $(500\mu\text{m})^2$
- Stringent requirements
 - AC-LGAD sensors will be used because of their capability to provide excellent resolution in timing and spatial resolution.

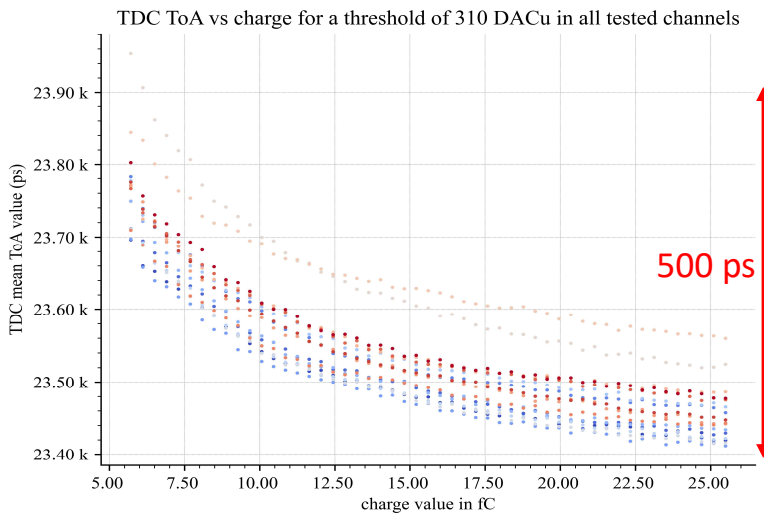


EIC Conceptual Design Report, 2021

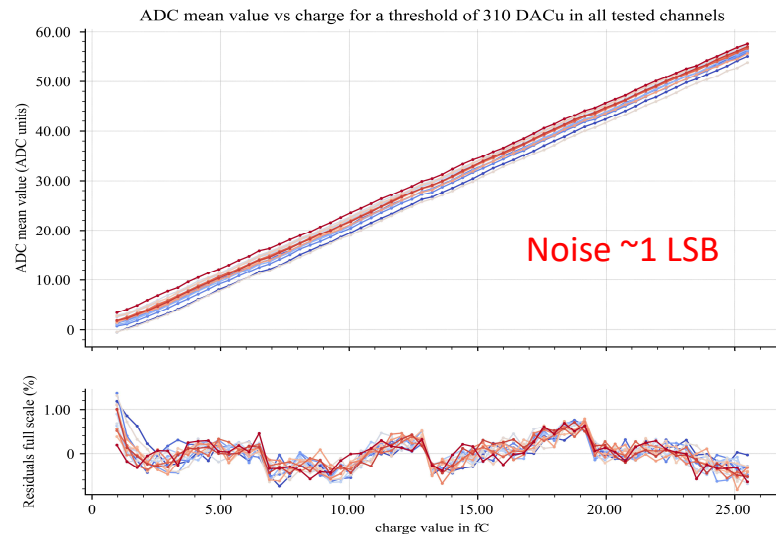


- Pixel 0
- Pixel 1
- Pixel 2
- Pixel 3
- Pixel 4
- Pixel 5
- Pixel 6
- Pixel 7
- Pixel 8
- Pixel 9
- Pixel 10
- Pixel 11
- Pixel 12
- Pixel 13
- Pixel 14
- Pixel 15

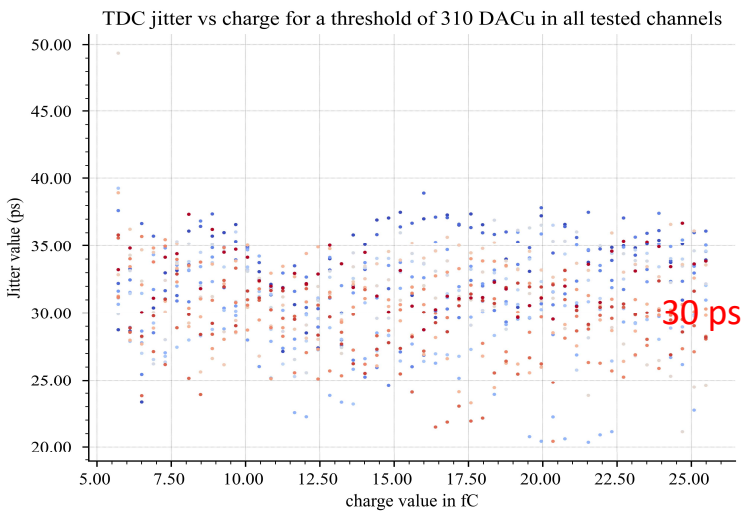
More in backup



- Pixel 0
- Pixel 1
- Pixel 2
- Pixel 3
- Pixel 4
- Pixel 5
- Pixel 6
- Pixel 7
- Pixel 8
- Pixel 9
- Pixel 10
- Pixel 11
- Pixel 12
- Pixel 13
- Pixel 14
- Pixel 15



- Pixel 0
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- Pixel 14
- Pixel 15



- Pixel 0
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- Pixel 4
- Pixel 5
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