

# Robotic Testing System Automation for DUNE Cold Electronics ASIC Quality Control

Natalie Tianai Ma<sup>1</sup>, Alejandro Yankelevich<sup>1</sup>, Larry Zhao<sup>1</sup> for the DUNE Collaboration  
<sup>1</sup> Department of Physics and Astronomy, University of California, Irvine

## Motivation

1. DUNE far detector uses liquid argon time projection chambers (LArTPCs) to study neutrino oscillation spectra
2. The two 17 kt Phase-I modules require custom cold electronics ASICs that operate reliably in liquid argon. FD-VD requires approximately **35,000** ASICs, while FD-HD requires approximately **54,000** ASICs
3. Each ASIC must pass pre-installation quality control (QC)
4. The Robotic Testing System (RTS) automates chip handling, testing, and result tracking at scale

## Automation

A Python-based finite state machine controls the RTS during long QC runs. It tracks the current operating state, supports safe pause and resume, and helps localize failures.

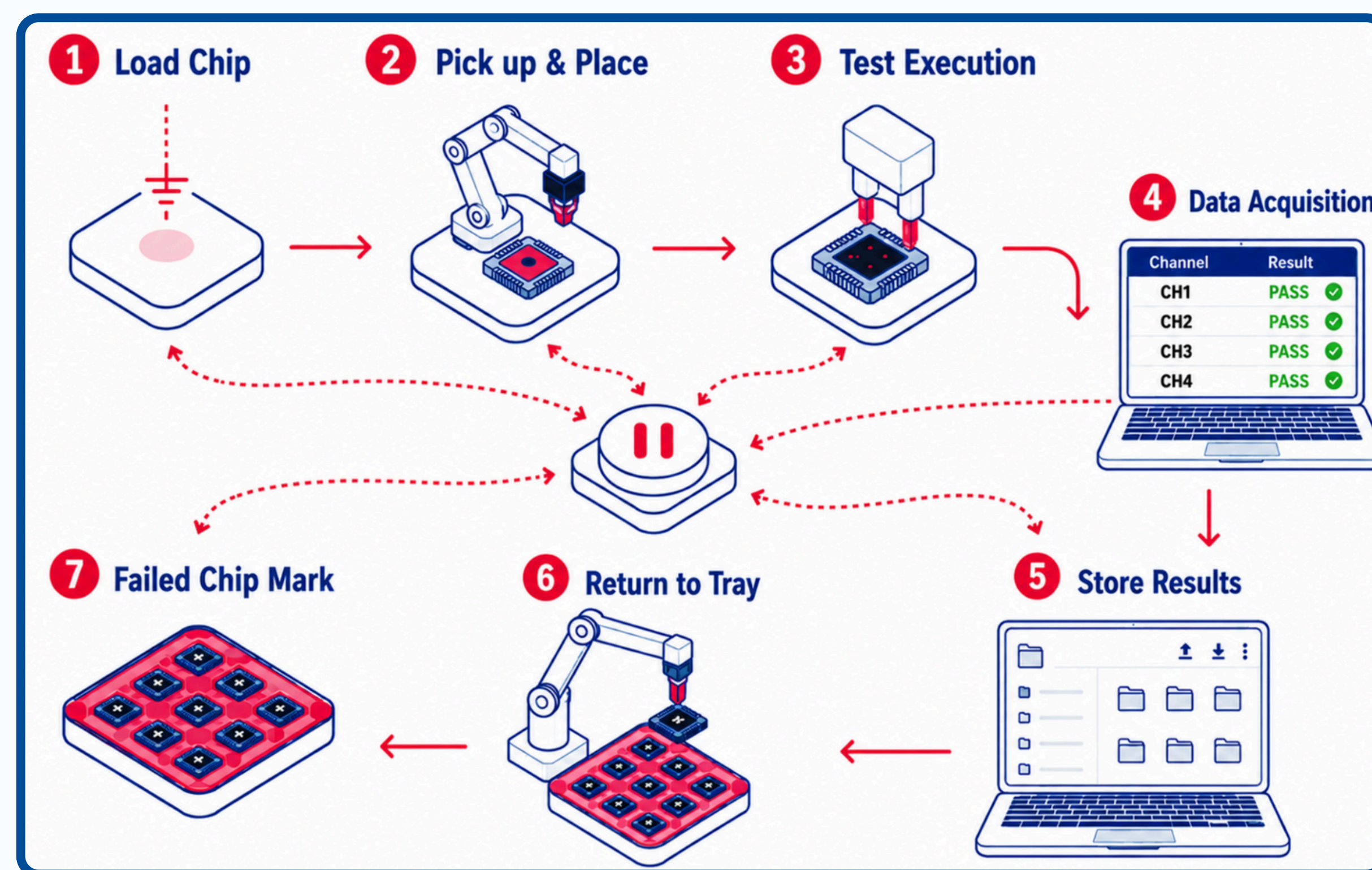
Each tray holds 40 COLDATA controller/transmitter chips, with two chips tested at a time. This control logic improves testing throughput by reducing routine operator input during each run. One tray requires about 20 test cycles and can be completed in roughly **4 hours**.



The RTS at UC Irvine, May 2026

We specifically acknowledge the Michigan State University and Brookhaven National Laboratory groups for designing and producing the RTS hardware.

## RTS Workflow



RTS Workflow Diagram

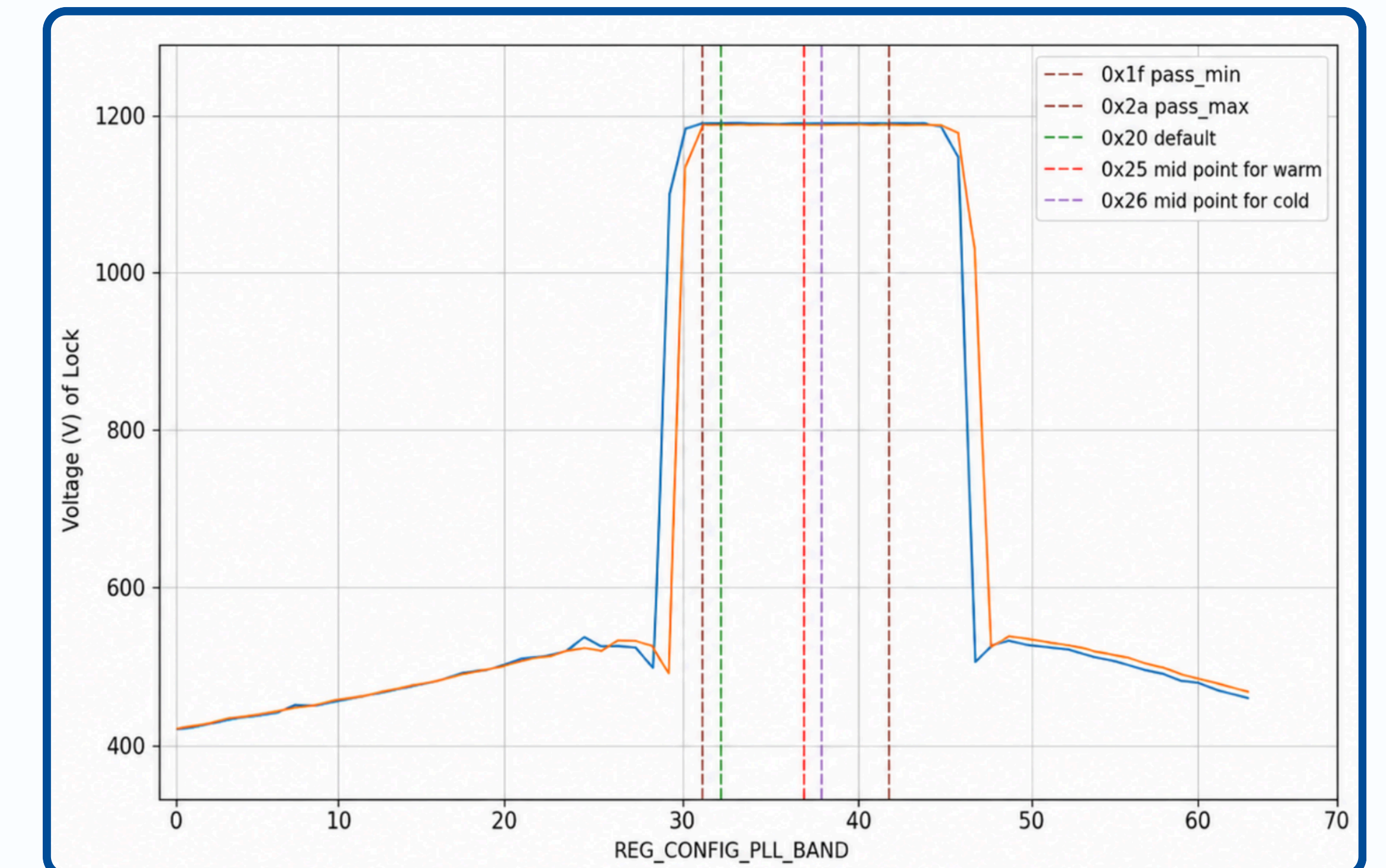
The RTS workflow tracks each chip from indexed tray loading to paired-socket COLDATA QC testing. Good chips are returned to their original tray positions, while failed chips are marked and placed in a designated failure tray location.

Chip position, socket assignment, and test output are preserved for later review.

## Results and Validation

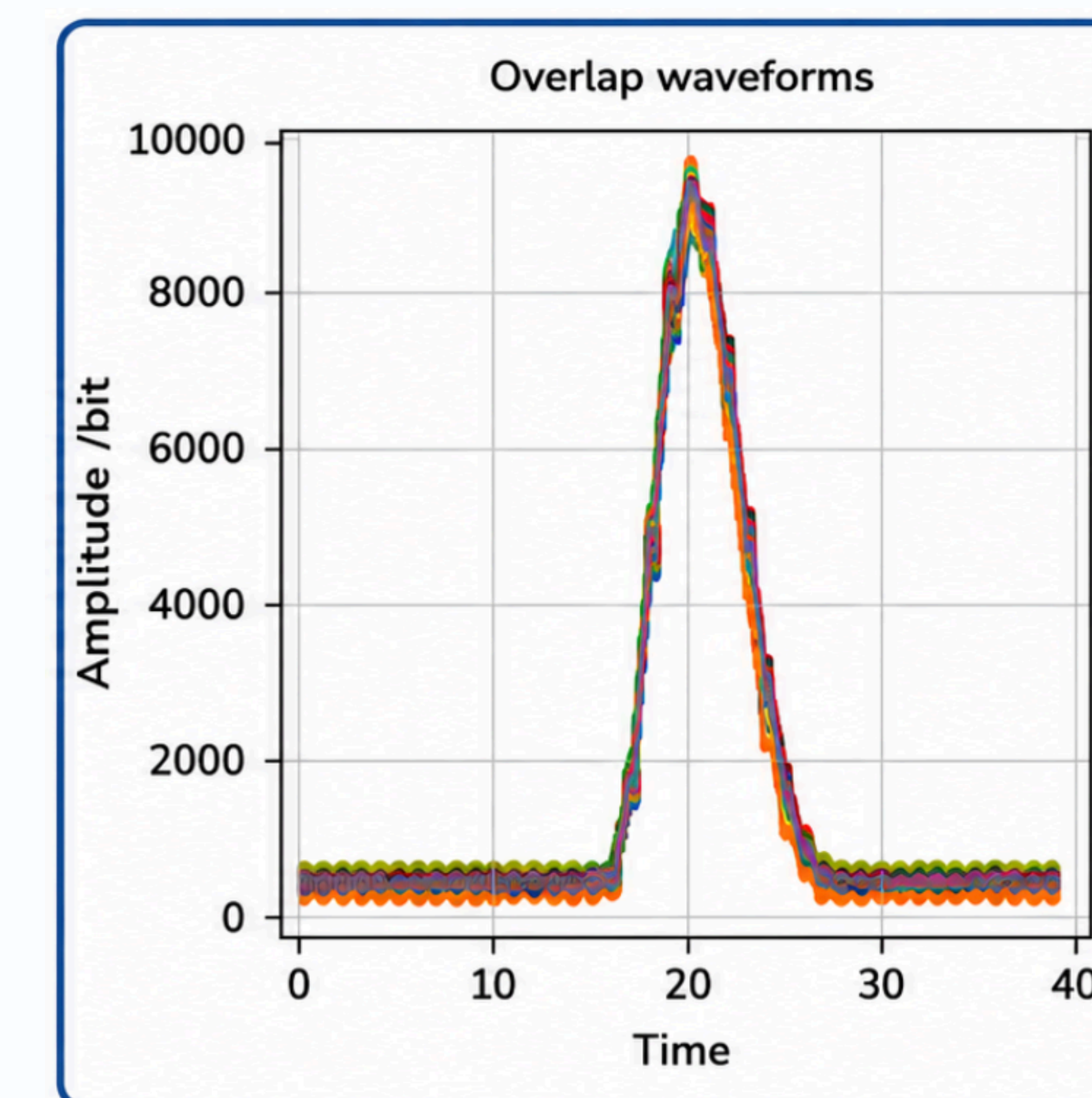
RTS runs are validated using standard COLDATA QC outputs, including calibration checks, PLL lock scans, ADC pattern tests, pulse response distributions, and noise measurements.

These plots confirm stable power, PLL lock, expected ADC response, and low noise, showing that the automated workflow executes the required test sequence and produces **diagnostic results** for each chip pair.

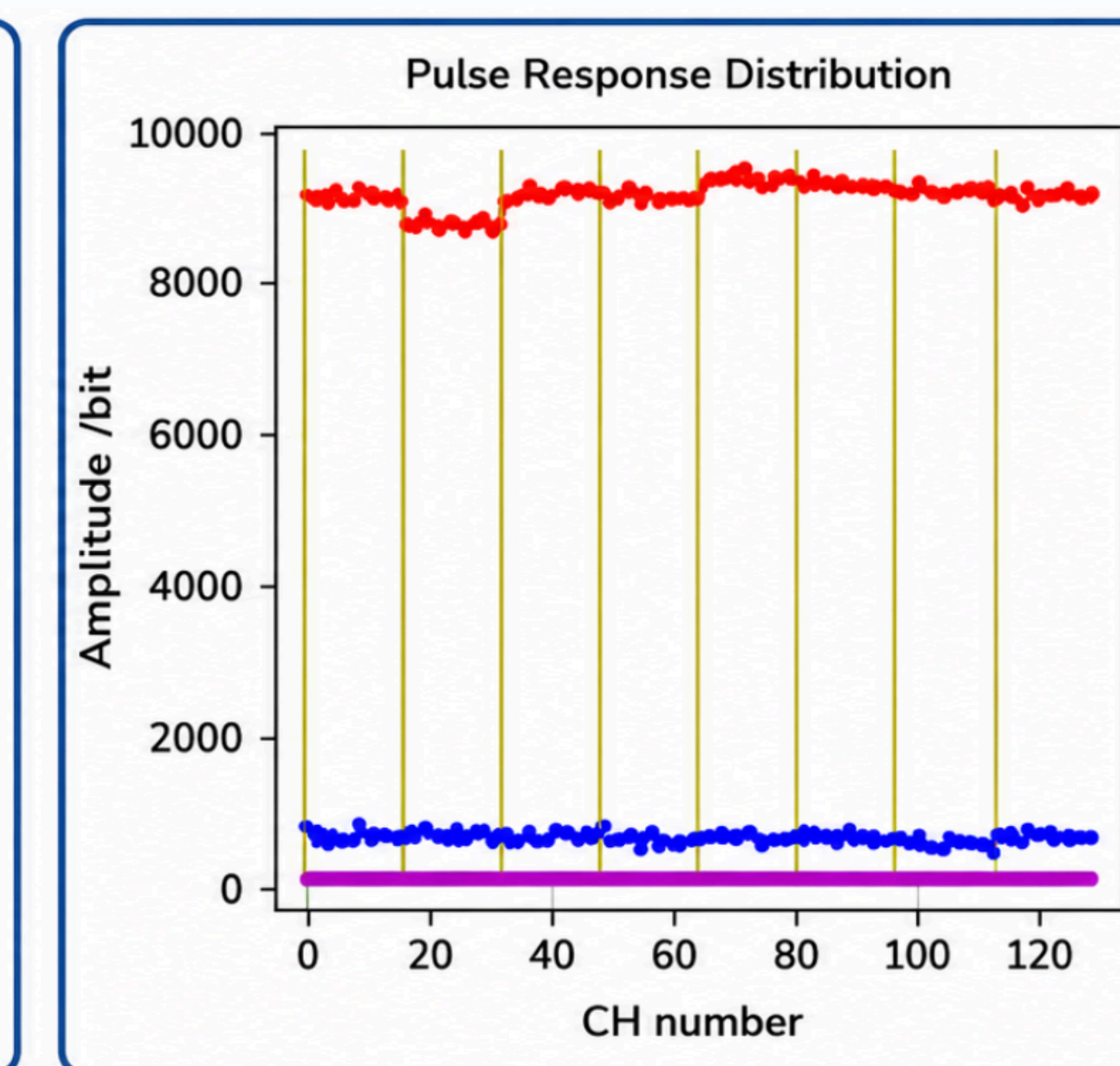


Phase-Locked Loop (PLL) scan confirms stable lock across the accepted register range

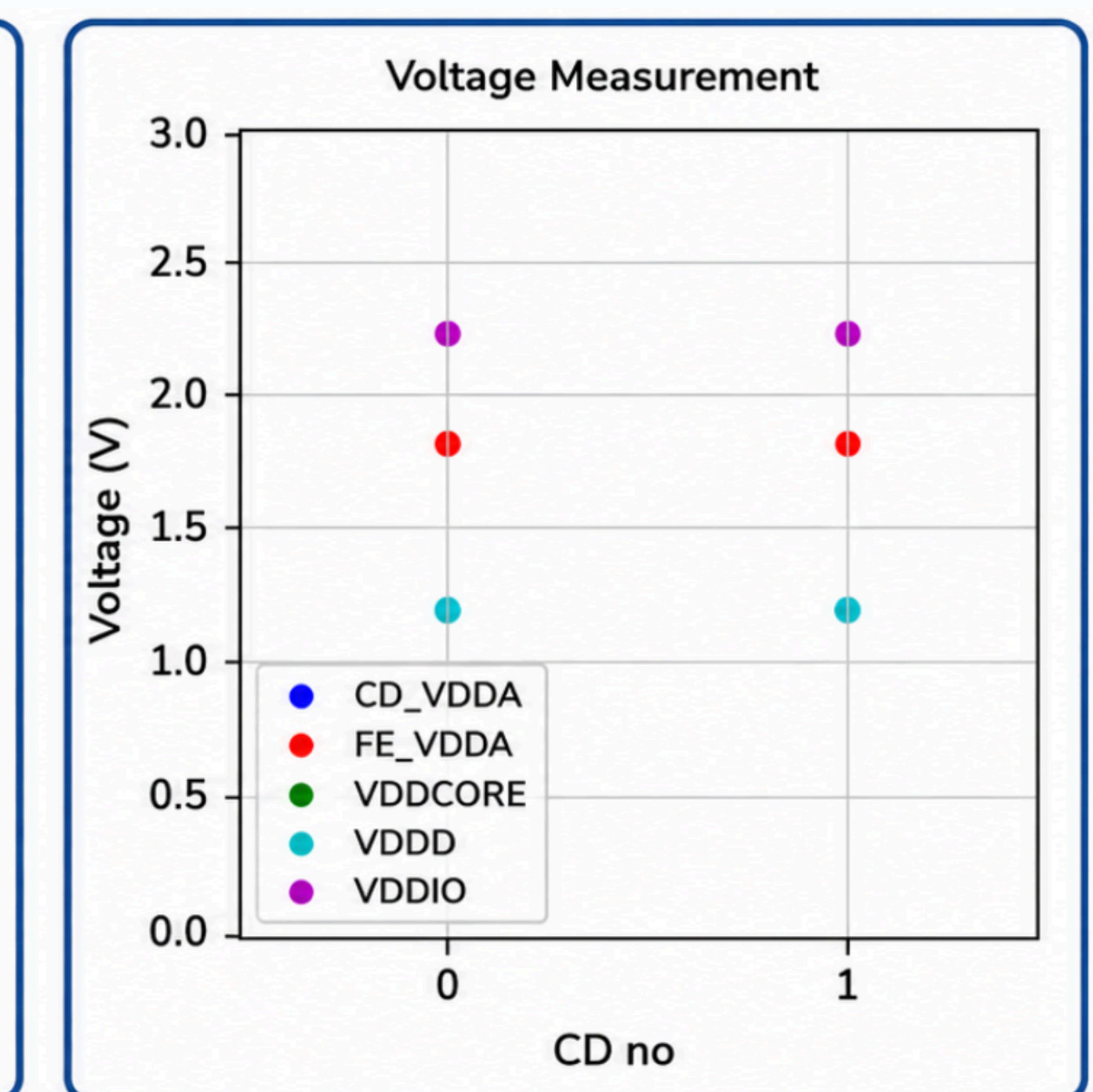
\*Plots here are **selected** QC outputs. Each RTS run produces additional diagnostic graphs for review.



Pulse Shape Consistency



Channel Pulse Response



Voltage Rail Monitoring

From July 2025 to May 2026, the UCI RTS site completed testing of **2,000** COLDATA chips. **COLDATA yield: 98.24%**, with 1,952 passed out of 1,987 electrically tested chips and 35 failed QC tests, excluding bent chips.

Future RTS upgrades will support liquid-nitrogen cryogenic ASIC testing, as already demonstrated by the cryo-capable RTS at Brookhaven National Lab. RTSs are also operated at **Fermilab**, **Michigan State University**, **Louisiana State University**, **Brookhaven National Laboratory**, and **Lawrence Berkeley National Laboratory**. We acknowledge their contribution in DUNE ASIC QC testing.