Detector development for the Future Circular Collider in the DRD3 Collaboration

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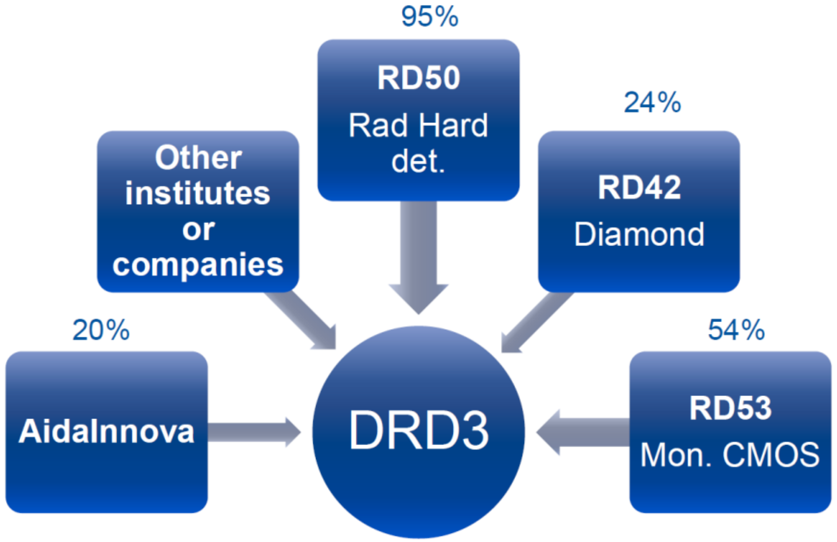
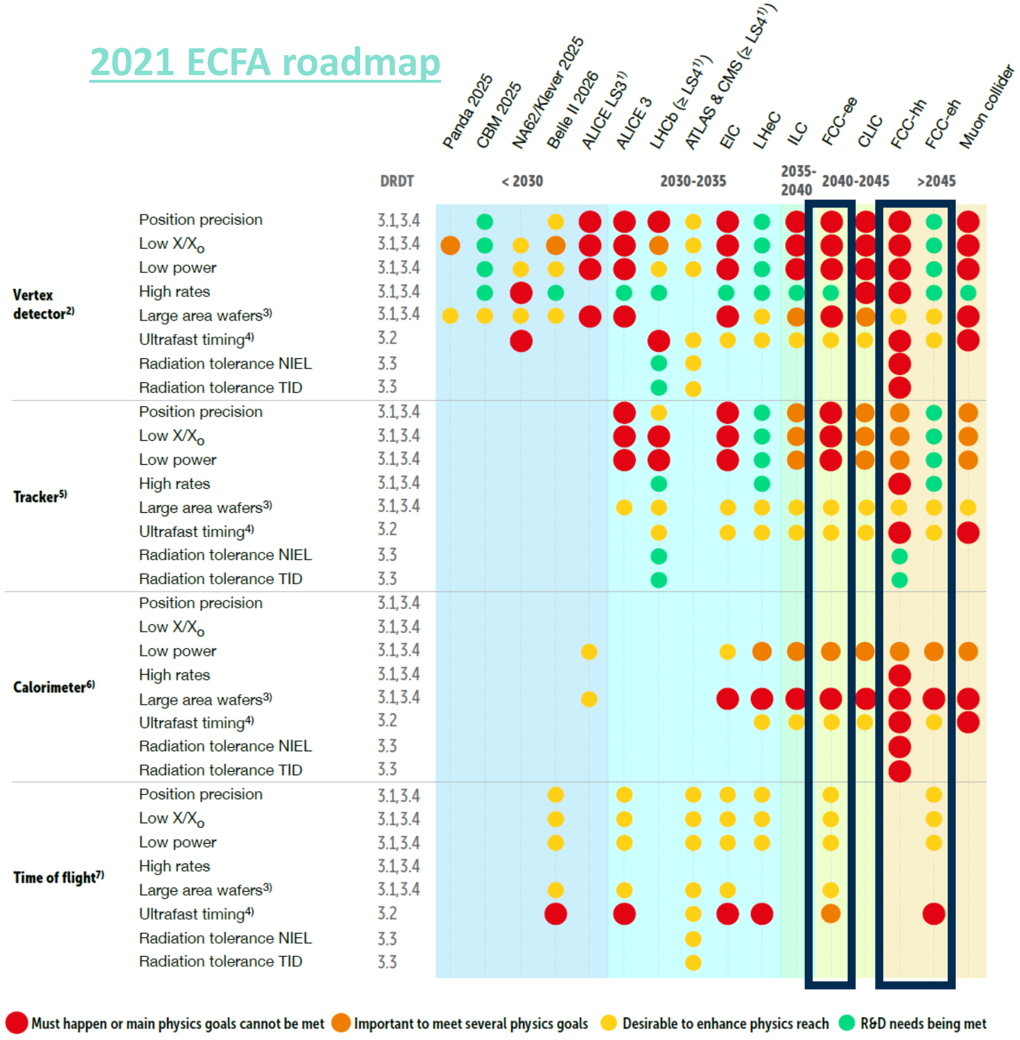
CAP Congress 2026

Introduction

- solid state detectors based on semiconductors are used in almost all particle physics experiments
  - revolutionary performance improvements are needed for future experiments
- DRD3 as successor to RD50 Collaboration, extended by diamonds (RD42) and 3D integration



[2021 ECFA roadmap](#)

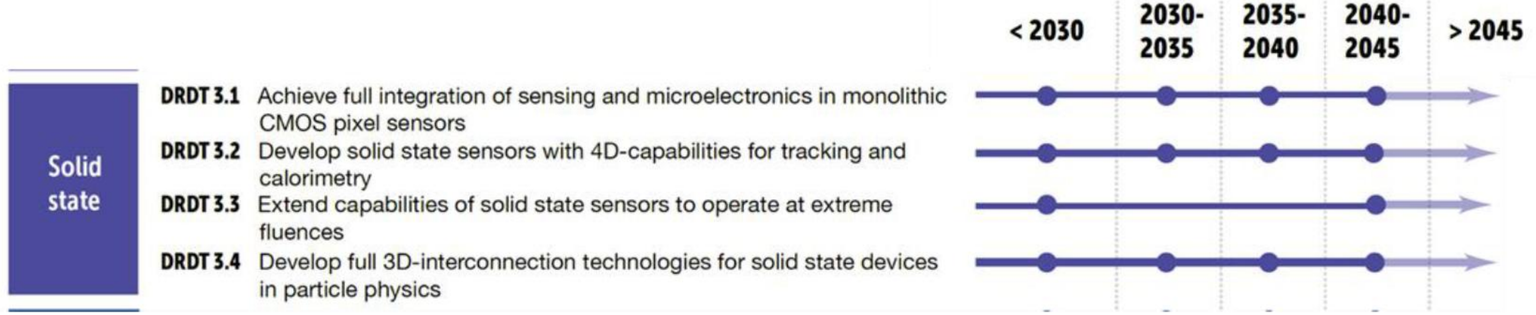


		DRDT	Panda 2025	CBM 2025	NA62/Klever 2025	Belle II 2026	ALICE LS3$^{1)}$	ALICE 3	LHCb (≥ LS4$^{1)}$)	ATLAS & CMS (≥ LS4$^{1)}$)	EIC	LHeC	ILC	FCC-ee	CLIC	FCC-hh	FCC-eh	Muon collider
			< 2030					2030-2035					2035-2040	2040-2045		>2045		
Vertex detector$^{2)}$	Position precision	3.1,3.4		🟢		🟡	🔴	🔴	🔴	🟡	🔴	🟢	🔴	🔴	🔴	🔴	🟢	🔴
	Low X/X$_0$	3.1,3.4	🟠	🟢	🟡	🟠	🔴	🔴	🟠	🟡	🔴	🟢	🔴	🔴	🔴	🔴	🟢	🔴
	Low power	3.1,3.4		🟢	🟡	🟡	🔴	🔴	🟡	🟡	🔴	🟢	🔴	🔴	🔴	🔴	🟢	🔴
	High rates	3.1,3.4		🟢	🔴	🟢		🟢	🟢		🟢	🟢	🟢	🟢	🔴	🔴	🟢	🟢
	Large area wafers$^{3)}$	3.1,3.4	🟡	🟡	🟡	🟡	🔴	🔴			🔴	🟡	🟠	🔴	🟠	🟡	🟡	🔴
	Ultrafast timing$^{4)}$	3.2			🔴				🔴	🟡	🟡	🟡	🟡	🟡	🟡	🔴	🟡	🔴
	Radiation tolerance NIEL	3.3							🟢	🟡						🔴		
	Radiation tolerance TID	3.3							🟢	🟡						🔴		
Tracker$^{5)}$	Position precision	3.1,3.4						🔴	🟡		🔴	🟢	🟠	🔴	🟠	🟠	🟢	🟠
	Low X/X$_0$	3.1,3.4						🔴	🔴		🔴	🟢	🟠	🔴	🟠	🟠	🟢	🟠
	Low power	3.1,3.4						🔴	🔴		🔴	🟢	🟠	🔴	🟠	🟠	🟢	🟠
	High rates	3.1,3.4							🟢			🟢				🔴	🟢	
	Large area wafers$^{3)}$	3.1,3.4						🟡	🟡		🟡	🟡	🟡	🟡	🟡	🟡	🟡	🟡
	Ultrafast timing$^{4)}$	3.2							🟡		🟡	🟡	🟡	🟡	🟡	🔴	🟡	🔴
	Radiation tolerance NIEL	3.3							🟢							🟢		
	Radiation tolerance TID	3.3							🟢							🟢		
Calorimeter$^{6)}$	Position precision	3.1,3.4																
	Low X/X$_0$	3.1,3.4																
	Low power	3.1,3.4					🟡				🟡	🟠	🟠	🟠	🟠	🟠	🟠	🟠
	High rates	3.1,3.4														🔴		
	Large area wafers$^{3)}$	3.1,3.4					🟡				🔴	🔴	🔴	🔴	🔴	🔴	🔴	🔴
	Ultrafast timing$^{4)}$	3.2										🟡	🟡	🟡	🟡	🔴	🟡	🔴
	Radiation tolerance NIEL	3.3														🔴		
	Radiation tolerance TID	3.3														🔴		
Time of flight$^{7)}$	Position precision	3.1,3.4				🟡		🟡		🟡	🟡	🟡		🟡			🟡	
	Low X/X$_0$	3.1,3.4				🟡		🟡		🟡	🟡	🟡		🟡			🟡	
	Low power	3.1,3.4				🟡		🟡		🟡	🟡	🟡		🟡			🟡	
	High rates	3.1,3.4																
	Large area wafers$^{3)}$	3.1,3.4				🟡		🟡		🟡	🟡			🟡				
	Ultrafast timing$^{4)}$	3.2				🔴		🔴		🟡	🔴	🔴		🟠			🔴	
	Radiation tolerance NIEL	3.3								🟡								
	Radiation tolerance TID	3.3								🟡								

🔴 Must happen or main physics goals cannot be met 🟠 Important to meet several physics goals 🟡 Desirable to enhance physics reach 🟢 R&D needs being met

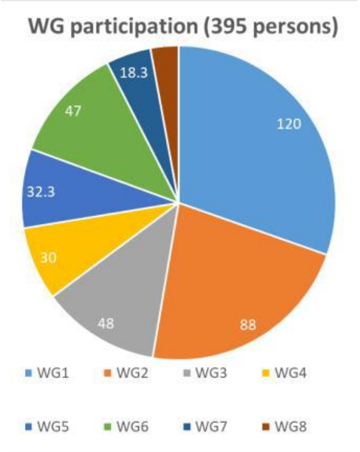
Organisation of the DRD3 collaboration

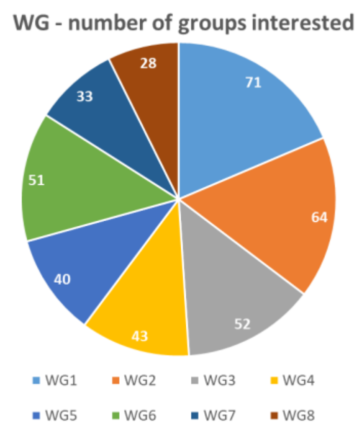
- **Working group (WG)** – long term **collaborative** R&D activity linked to certain technology / purpose / application / method aiming to fulfil the research goals; linked to semiconduction detectors, e.g.:
  - R&D outside particle physics application with benefits for HEP
  - novel semiconductor material characterization ideas
- **Working package (WP)** – short / midterm strategic R&D activity reflected in the ECFA detector roadmap document – DRD Themes; **will be supported by dedicated funding lines**



		< 2030	2030-2035	2035-2040	2040-2045	> 2045
Solid state	**DRDT 3.1** Achieve full integration of sensing and microelectronics in monolithic CMOS pixel sensors	●	●	●	●	
	DRDT 3.2 Develop solid state sensors with 4D-capabilities for tracking and calorimetry	●	●	●	●	
	DRDT 3.3 Extend capabilities of solid state sensors to operate at extreme fluences	●			●	
	DRDT 3.4 Develop full 3D-interconnection technologies for solid state devices in particle physics	●	●	●	●	

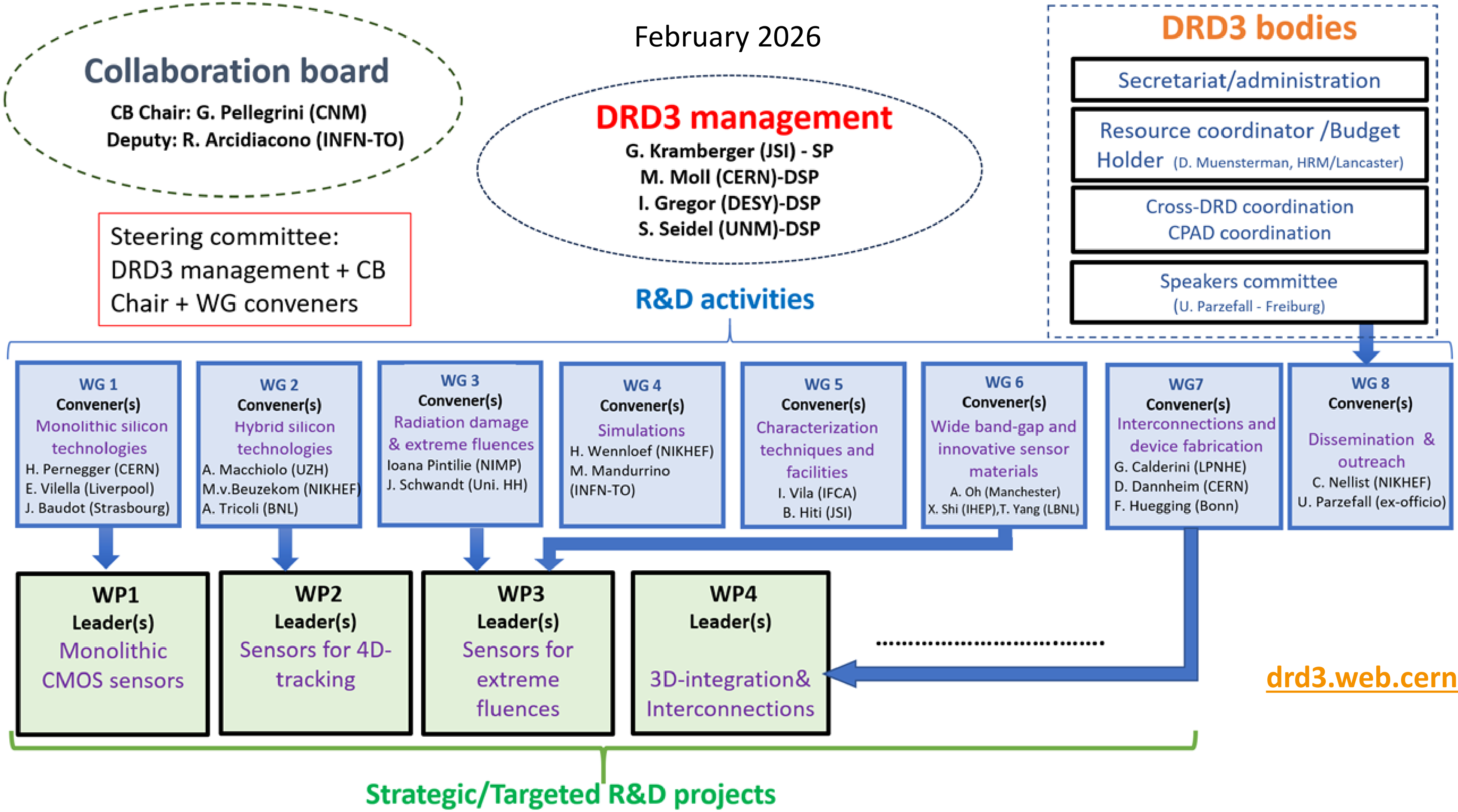
- **Common Collaboration Fund** – finance Blue-sky R&D small projects, common hardware, common activities (e.g. organization of the schools, thesis awards, test-beam / laser-test / irradiation campaigns)





in Canada:
Carleton + NRC,
SFU/TRIUMF

Organisation of the DRD3 collaboration



February 2026

Collaboration board
CB Chair: G. Pellegrini (CNM)
Deputy: R. Arcidiacono (INFN-TO)

Steering committee:
DRD3 management + CB Chair + WG conveners

DRD3 management
G. Kramberger (JSI) - SP
M. Moll (CERN)-DSP
I. Gregor (DESY)-DSP
S. Seidel (UNM)-DSP

DRD3 bodies

Secretariat/administration

Resource coordinator /Budget Holder (D. Muensterman, HRM/Lancaster)

Cross-DRD coordination
CPAD coordination

Speakers committee
(U. Parzefall - Freiburg)

R&D activities

WG 1
Convener(s)
Monolithic silicon technologies
H. Pernegger (CERN)
E. Vilella (Liverpool)
J. Baudot (Strasbourg)

WG 2
Convener(s)
Hybrid silicon technologies
A. Macchiolo (UZH)
M.v.Beuzekom (NIKHEF)
A. Tricoli (BNL)

WG 3
Convener(s)
Radiation damage & extreme fluences
Ioana Pintilie (NIMP)
J. Schwandt (Uni. HH)

WG 4
Convener(s)
Simulations
H. Wennloef (NIKHEF)
M. Mandurrino (INFN-TO)

WG 5
Convener(s)
Characterization techniques and facilities
I. Vila (IFCA)
B. Hiti (JSI)

WG 6
Convener(s)
Wide band-gap and innovative sensor materials
A. Oh (Manchester)
X. Shi (IHEP),T. Yang (LBNL)

WG7
Convener(s)
Interconnections and device fabrication
G. Calderini (LPNHE)
D. Dannheim (CERN)
F. Huegging (Bonn)

WG 8
Convener(s)
Dissemination & outreach
C. Nellist (NIKHEF)
U. Parzefall (ex-officio)

WP1
Leader(s)
Monolithic CMOS sensors

WP2
Leader(s)
Sensors for 4D-tracking

WP3
Leader(s)
Sensors for extreme fluences

WP4
Leader(s)
3D-integration& Interconnections

……………………………………

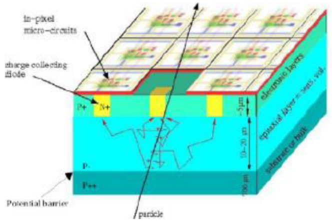
Strategic/Targeted R&D projects

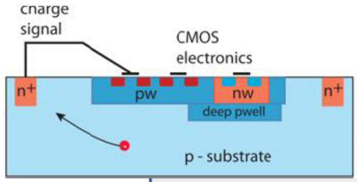
drd3.web.cern.ch

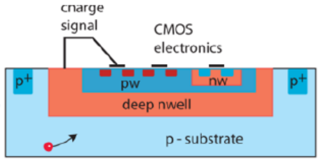
Present silicon sensor R&D

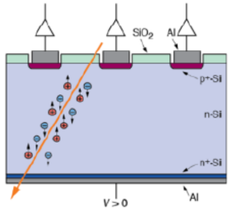
G. Kramberger
March 2026 DRDC review

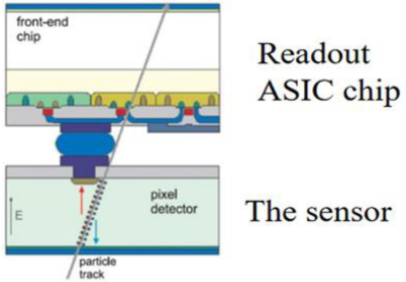
- Monolithic devices
  (**WG1/WP1-CMOS**)
  55-180 nm processes
  - **Small electrode device**
    - MAPS
      monolithic active pixel sensors
    - with gain
    - Depleted MAPS wo Gain
      - Optimized for rates/power/position resolution
  - **Large electrode device**
    - Depleted MAPS wo Gain
      - Optimized for radiation hardness /timing
    - with gain
    - Large area passive devices (strips)
- Hybrid devices
  (WG2/WP2-4D tracking)
  - Planar
    - Large area passive devices (strips)
    - With Gain (LGADs)
  - 3D devices
    - Trench 3D
    - Column 3D
      - With Gain

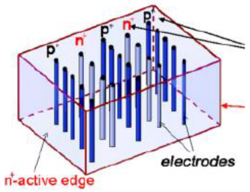








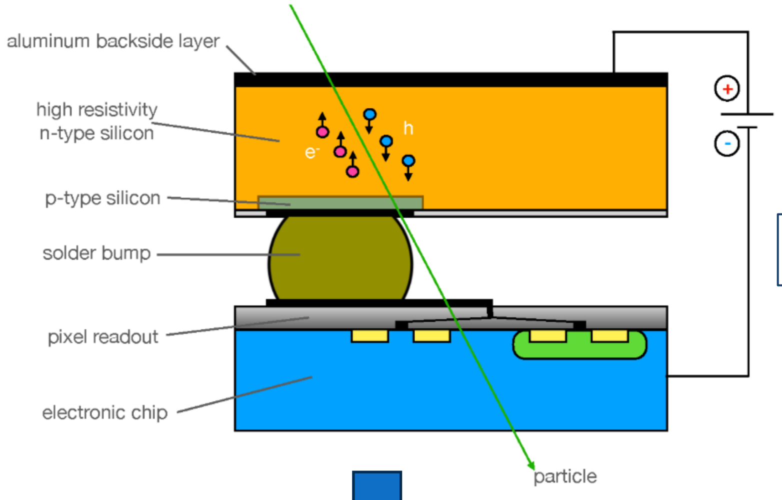




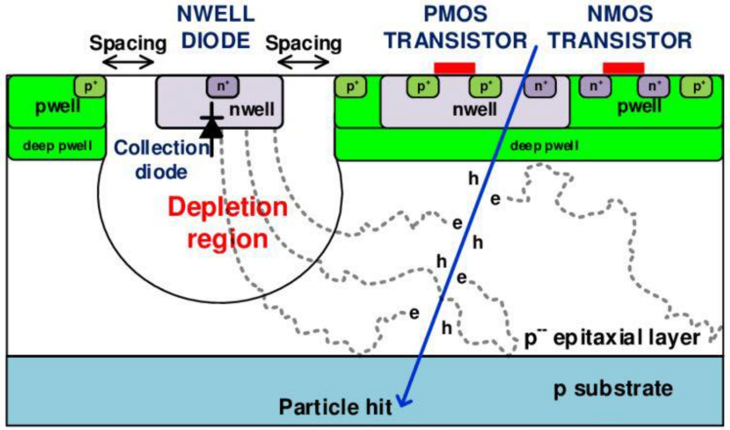
🟥 proof of concept ongoing
🟨 recent research (working prototype)
🟩 proven/demonstrated

Monolithic silicon sensors (WG1)

- combine sensing and readout elements on a single silicon wafer
  - integration of front-end electronics (amplifier, shaper, ADC, comparator, etc.)
  - potential to use commercial CMOS processes: fast, large-scale, low-cost production
- monolithic sensors are thinner, lighter, cheaper than hybrid devices
- tackle challenges of future colliders:
  - fast charge collection
  - high signal-to-noise ratio
  - low power consumption
  - high spatial and timing resolution



hybrid pixel



monolithic pixel sensor

The MALTA depleted monolithic active pixel sensor (WG1)

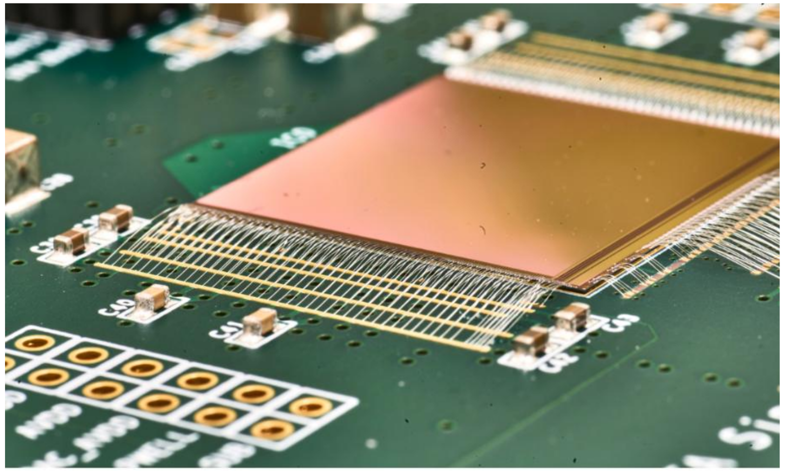
MALTA: Monolithic ALice To Atlas

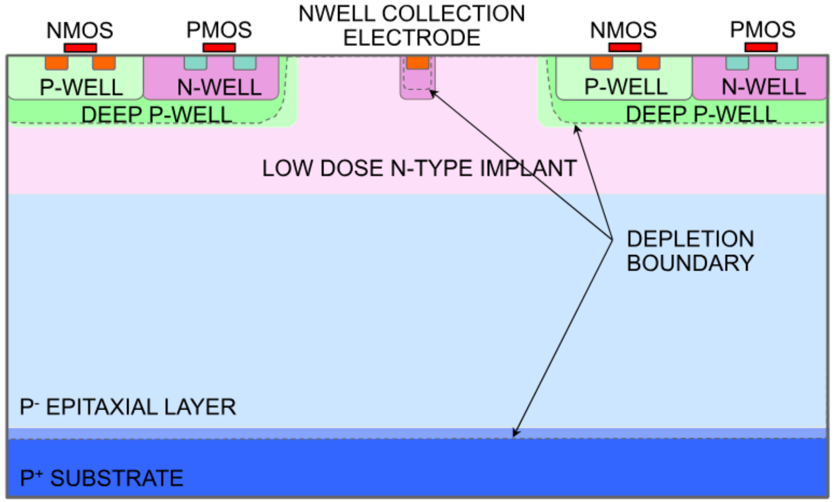
- developed in 180nm TowerJazz CMOS imaging technology
- 2 x 2 cm^2 sensor with 512 x 512 pixel matrix
- thickness: 50 to 300µm

- performance:
  - radiation hardness: up to 3 x 10^{15} n_{eq}/cm^2 (NIEL), >100 Mrad (TID)
  - time response <2ns

- process features:
  - modified process with low dose n-type implant for uniform depletion
  - further modifications (n-layer gap & extra deep well) to improve charge collection at pixel edges
  - high resistivity substrates for improved radiation tolerance

- outlook:
  - new mini-MALTA3 demonstrator chips are being produced (ETA: July/August)
  - migration to 65nm CMOS technology
    - simulation efforts ongoing to verify performance (Carleton 🍁)





Caribou DAQ system

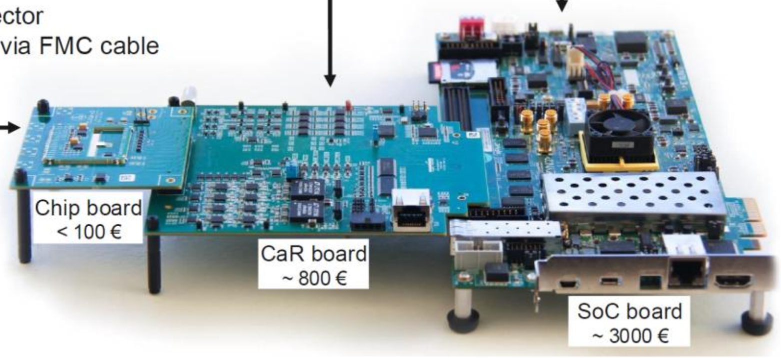
- open source, flexible, modular data acquisition (DAQ) platform for silicon pixel detectors
  - laboratory studies and beam tests
  - many DRD3 (RD50) pixel detector projects integrated,
  - ready-to-use, adjustable, and efficient prototyping platform for detector development

- currently working on final board design for Caribou v2.0 (among others at Carleton)
- based on commercial System-on-Module (SoM)
  - integrated on CaR board

System-on-Chip (SoC) board
- ie: Xilinx ZC706 evaluation board
- Embedded CPU runs DAQ and control software
- FPGA runs custom firmware for detector control and readout

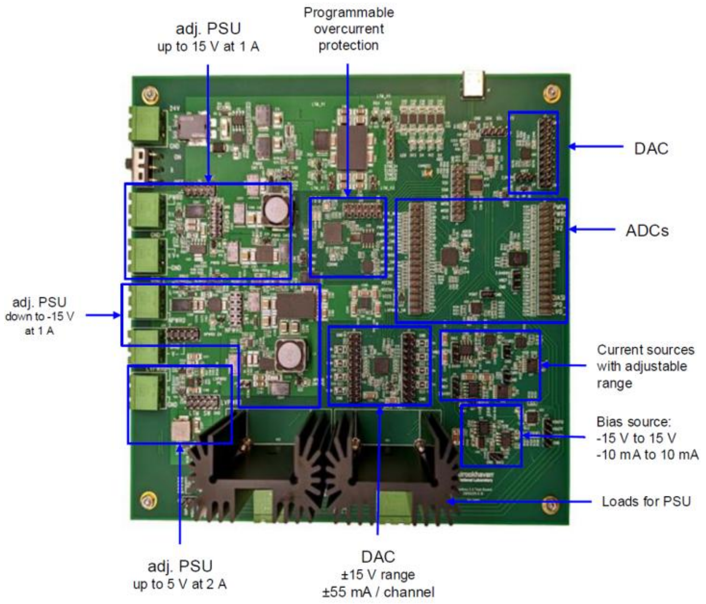
Control and Readout (CaR) interface board
- Physical interface from SoC to detector
- CaR – SoC connection extendable via FMC cable

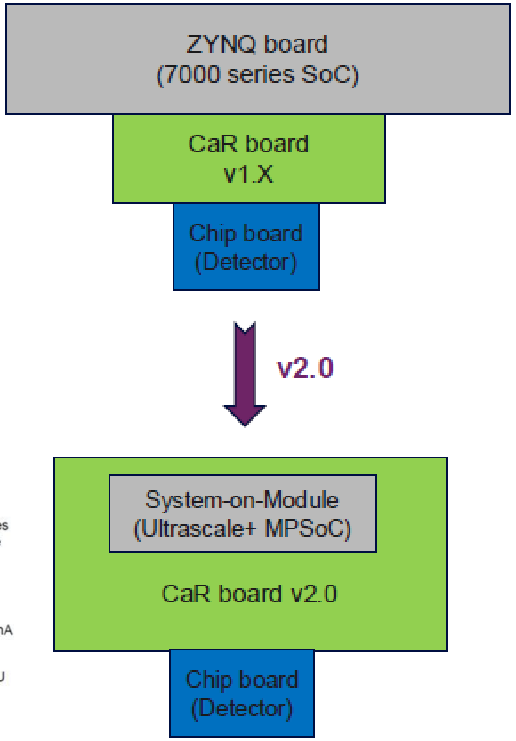
Detector (chip) carrier board
- Custom low-cost PCB
- Designed by users



[Caribou website](#)

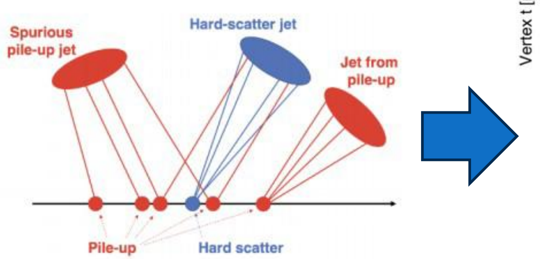
CaR board v2.0 test board (no SoM)

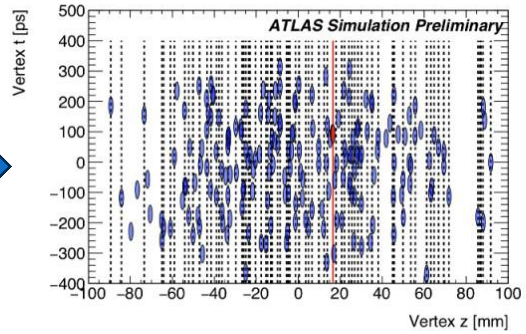




Low-Gain Avalanche Diodes (LGAD)

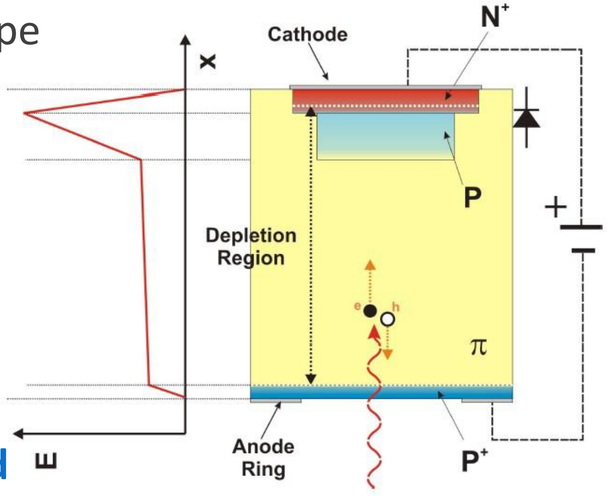
- segmented semiconductor diodes have achieved excellent spatial resolution for particle tracking
  - signal proportional to sensor active thickness
  - time resolution limited by signal rise time and S/N
  - not a problem if hit multiplicity low enough





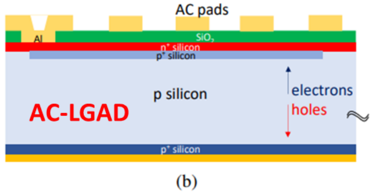
- **but**:
  - already in HL-LHC conditions, event pile-up can degrade physics performance → even worse in FCC
  - timing information can be used to mitigate pile-up
  - difficult to improve time resolution without compromising S/N in standard sensor design

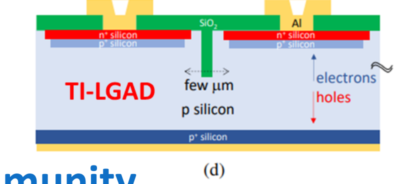
- silicon detectors with deep p-type gain implant below cathode
  - high electric field leads to charge multiplication (similar to avalanche diodes)
  - low gain of 10-50
  - LGADs can not only off-set lower signal, but also be used for **simultaneous position and timing measurement (~30ps)**
  - fine segmentation and fill factor become challenging



- fill factor and radiation hardness part of **several WP2 projects**
- fabricate LGADs in wide bandgap materials e.g. SiC, GaN

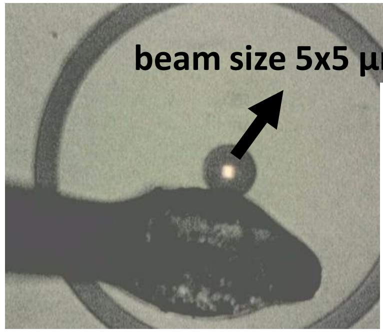
➢ **achieving sufficient radiation hardness for future colliders is a major effort in the community**

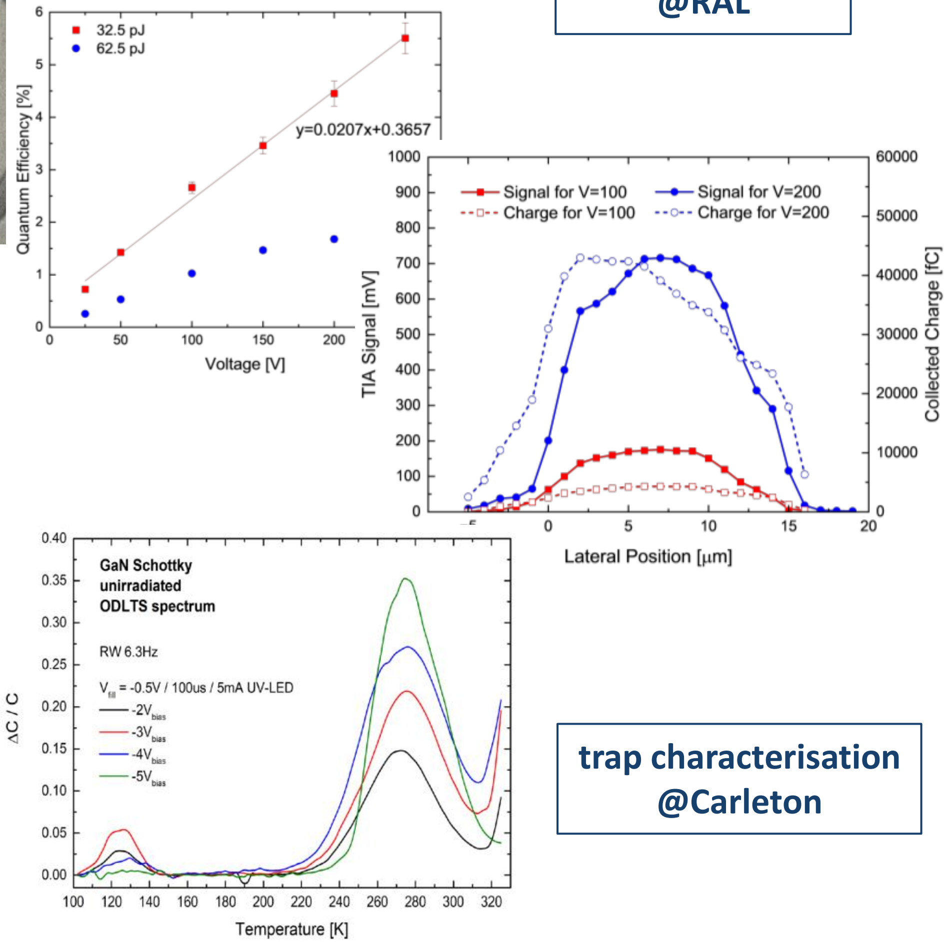




Gallium Nitride (GaN) devices for sensing applications (WG6)

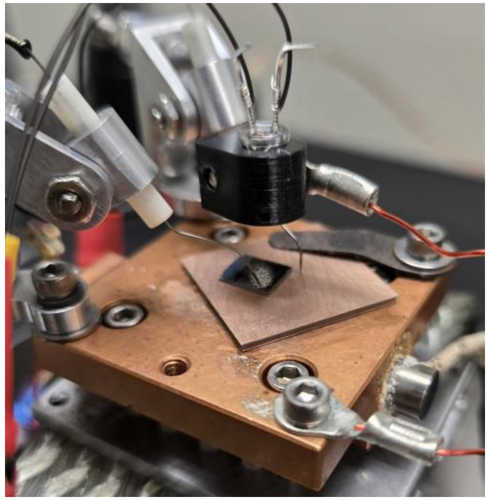
- GaN ubiquitous in high-power electronics, commonly used in UV photodetection, and under investigation for ionizing radiation detection
  - wide bandgap material attractive for application in extreme conditions (high temperature / radiation)
  - fast response due to high electron mobility
- increase material quality and reduce dislocation density by using **native GaN substrate** with thin epitaxial GaN layer
- previous Schottky fabrication runs at NRC Advanced Technology Facility
  - electrical tests at RAL and Carleton
- new fabrication runs already planned with different flavours of GaN devices: Schottky, p-i-n diode, Low-Gain Avalanche Diodes (LGADs)


beam size 5x5 µm²



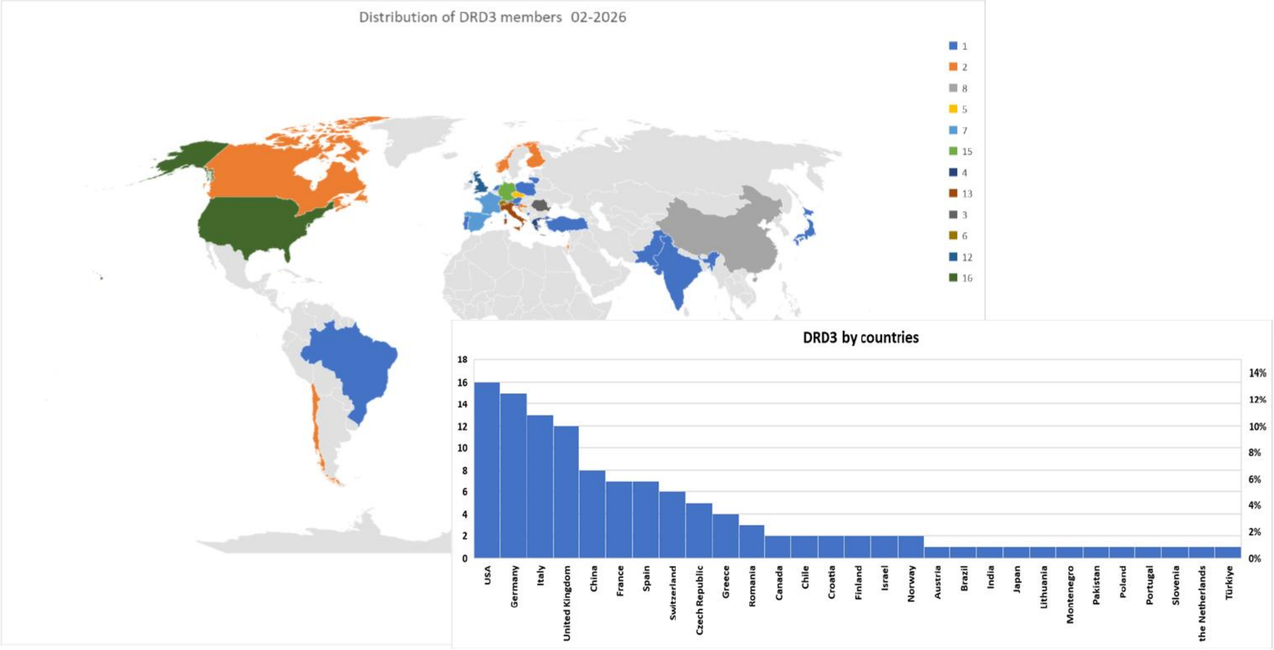
optical response @RAL

trap characterisation @Carleton



Summary

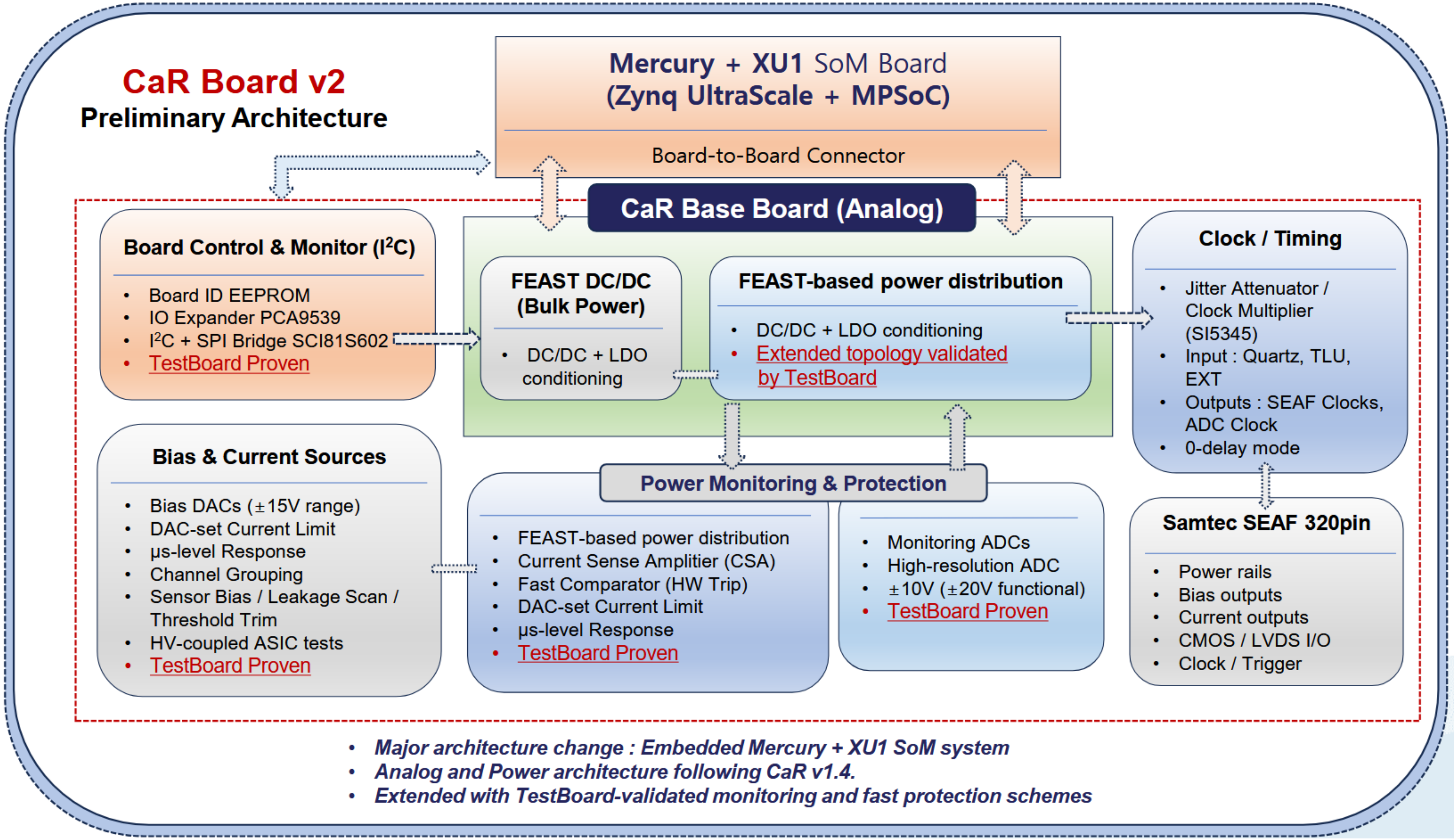
- DRD3 is a large international collaboration committed to semiconductor detector R&D
- many projects are working on detector solutions for future colliders like FCC-ee/hh
  - interlink with other CERN DRDs
- synergies with other field (e.g. medical imaging, space, nuclear physics)
- R&D efforts of many groups expected to ramp up in coming years, once HL-LHC upgrades are finished



drd3.web.cern.ch

Backup

Caribou v2 CaR (Control and Readout) Preliminary Architecture



CaR Board v2
Preliminary Architecture

Mercury + XU1 SoM Board
(Zynq UltraScale + MPSoC)

Board-to-Board Connector

CaR Base Board (Analog)

Board Control & Monitor (I^2C)

- Board ID EEPROM
- IO Expander PCA9539
- I^2C + SPI Bridge SCI81S602
- TestBoard Proven

FEAST DC/DC (Bulk Power)

- DC/DC + LDO conditioning

FEAST-based power distribution

- DC/DC + LDO conditioning
- Extended topology validated by TestBoard

Clock / Timing

- Jitter Attenuator / Clock Multiplier (SI5345)
- Input : Quartz, TLU, EXT
- Outputs : SEAF Clocks, ADC Clock
- 0-delay mode

Bias & Current Sources

- Bias DACs (±15V range)
- DAC-set Current Limit
- μs-level Response
- Channel Grouping
- Sensor Bias / Leakage Scan / Threshold Trim
- HV-coupled ASIC tests
- TestBoard Proven

Power Monitoring & Protection

- FEAST-based power distribution
- Current Sense Amplifier (CSA)
- Fast Comparator (HW Trip)
- DAC-set Current Limit
- μs-level Response
- TestBoard Proven

- Monitoring ADCs
- High-resolution ADC
- ±10V (±20V functional)
- TestBoard Proven

Samtec SEAF 320pin

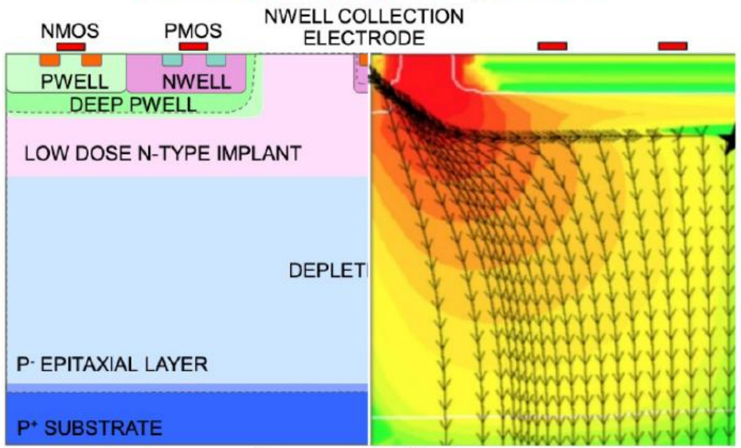
- Power rails
- Bias outputs
- Current outputs
- CMOS / LVDS I/O
- Clock / Trigger

- ***Major architecture change : Embedded Mercury + XU1 SoM system***
- ***Analog and Power architecture following CaR v1.4.***
- ***Extended with TestBoard-validated monitoring and fast protection schemes***

MALTA process modification

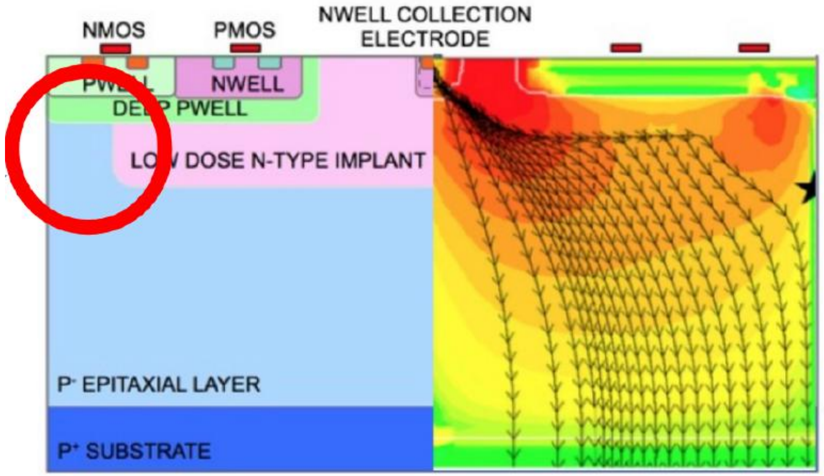
[A. Vijay
HSTD14 slides]

Standard modified process



- Lateral electric field not sufficient to push the deposited charge towards the small central electrode.
  - Efficiency decreases in pixel corners
  - Effect amplified by radiation damage

Gap in n- layer (NGAP)



Process modifications to improve charge collection in the pixel edges.

Extra deep well (XDPW)