CEPC Outer Tracker Recent Progress in Key Detector Technologies
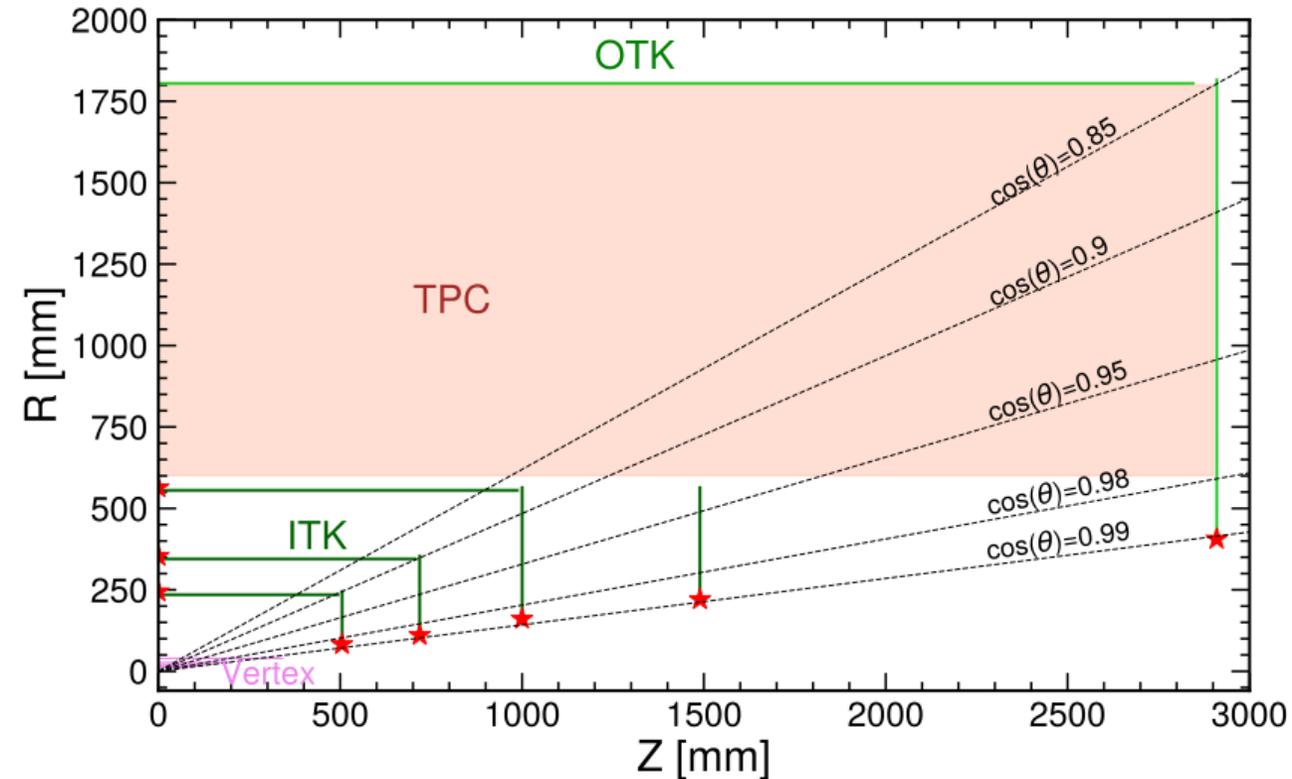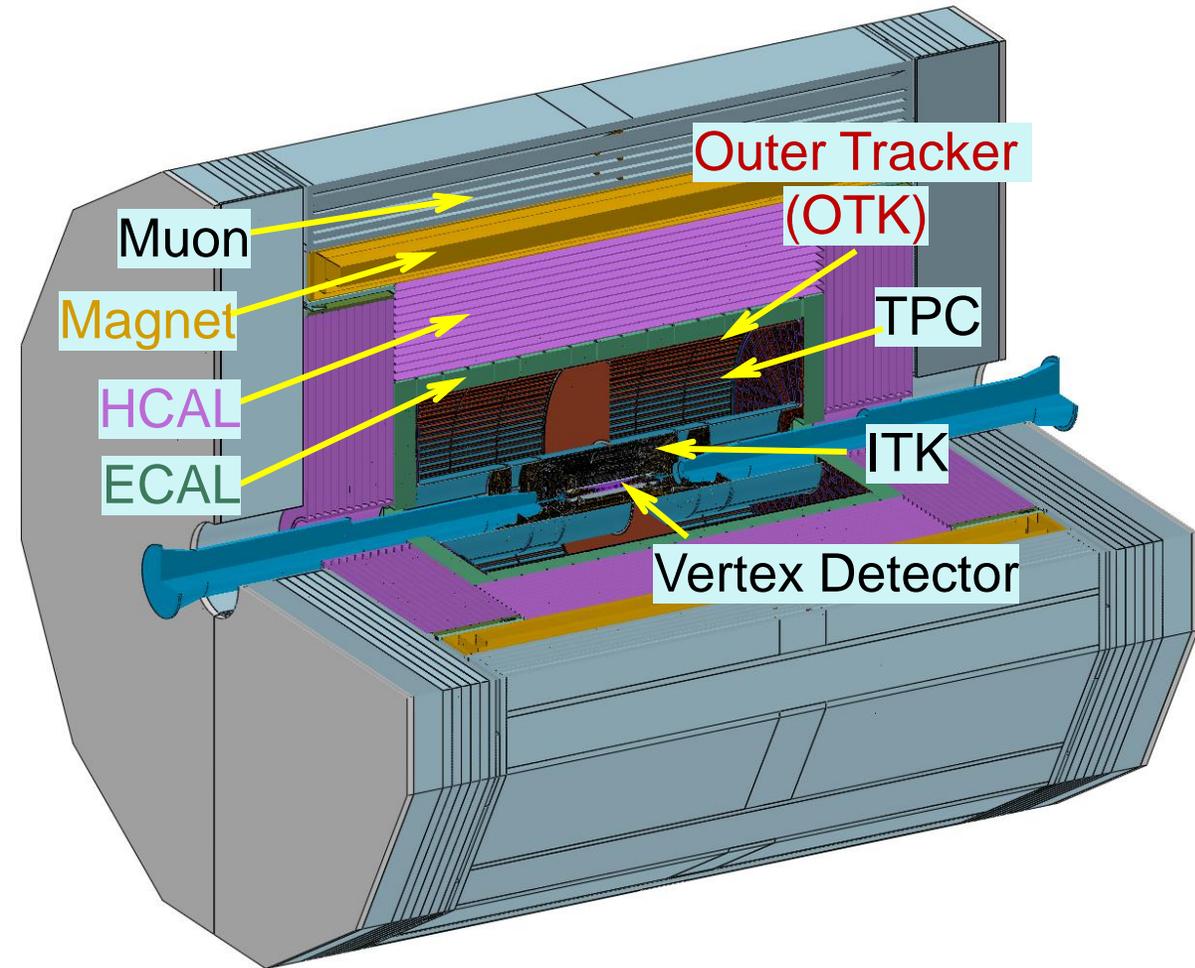
JiaJian TEOH（张嘉健）

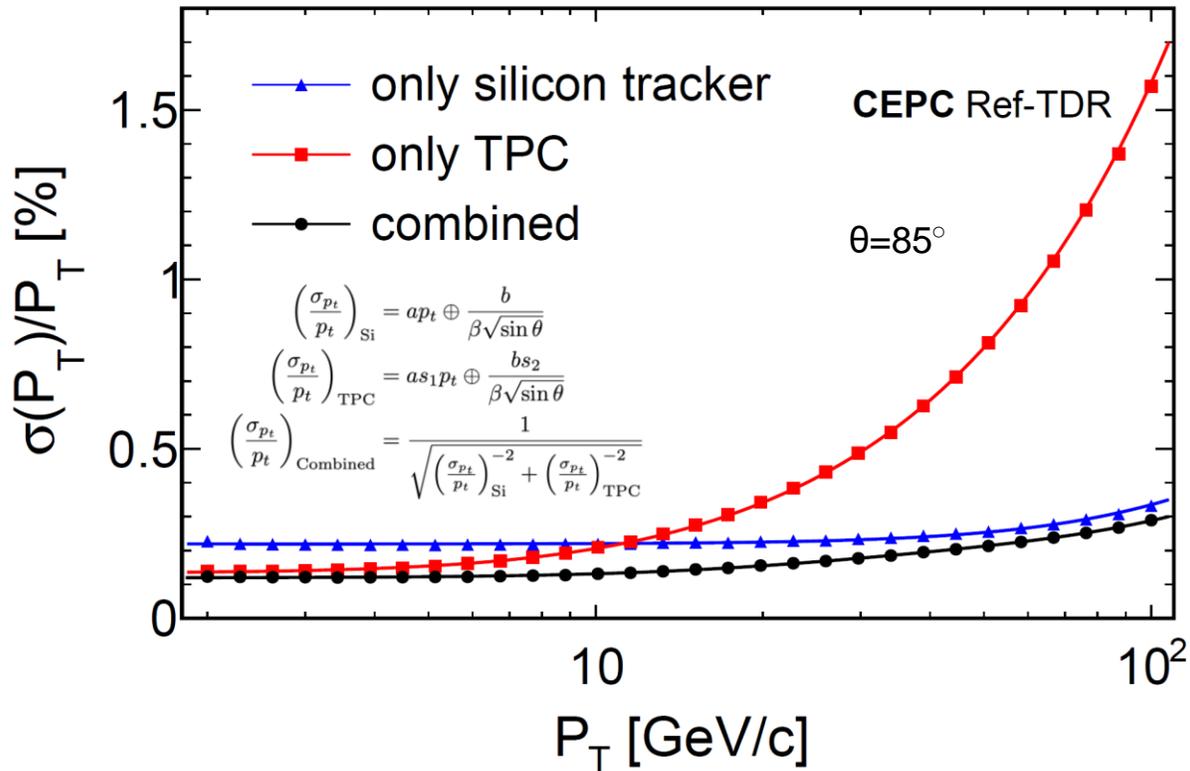*On behalf of the CEPC Silicon Tracker Group*

中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences
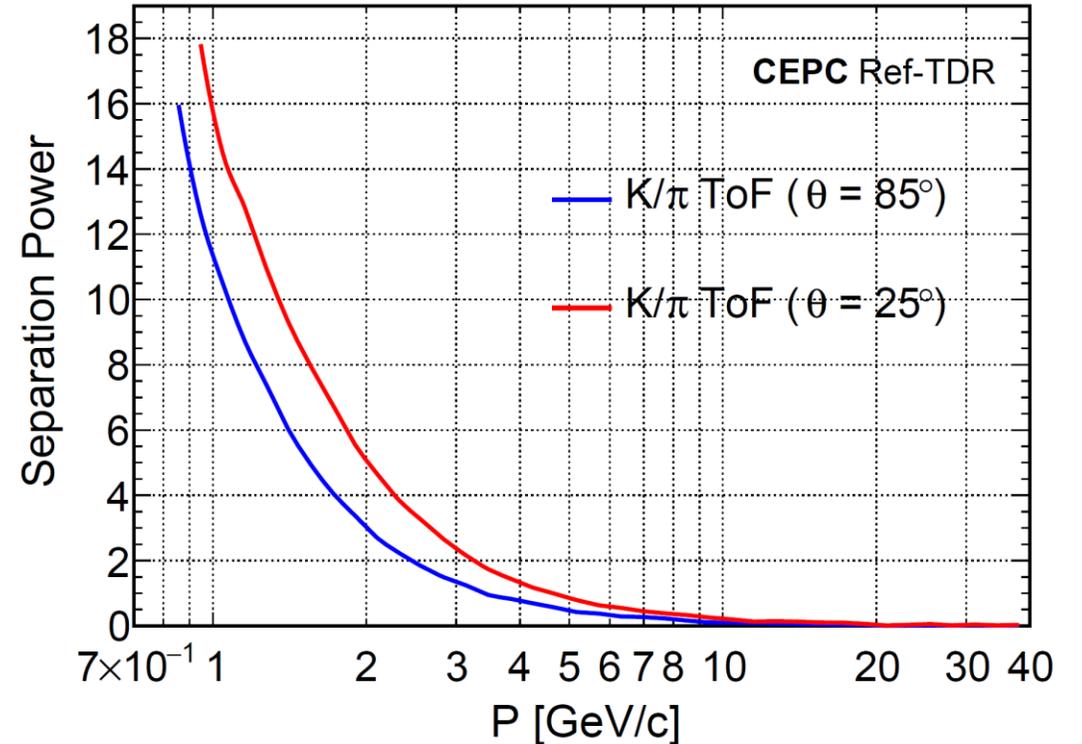
Introduction: CEPC Detector

- The outer tracker has single barrel layer and two endcap disks, with a total active area of 85 m².
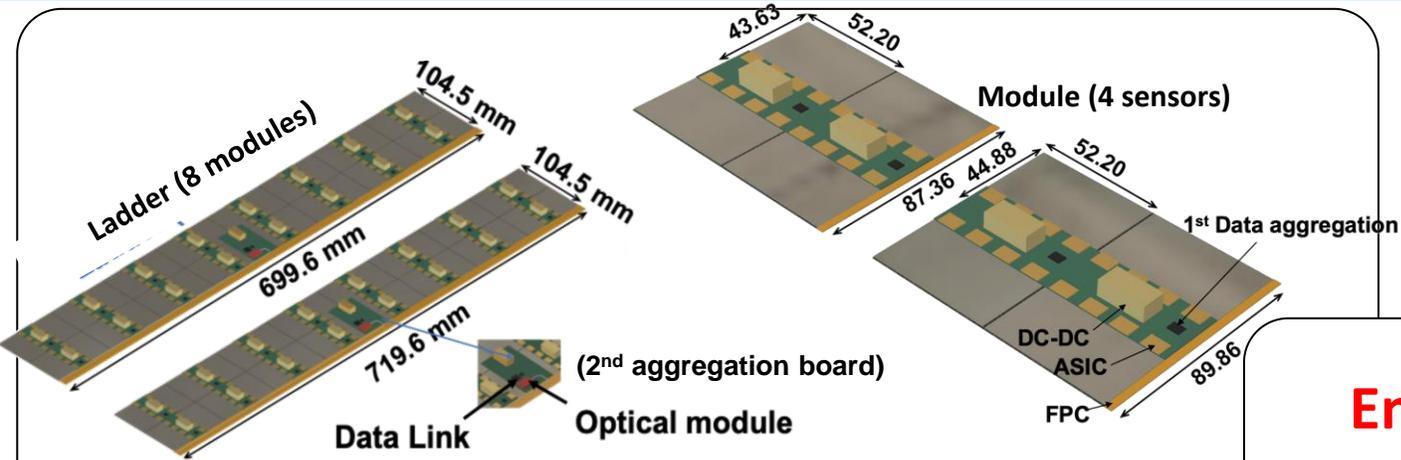
Detector Performance Requirements

Precision Higgs physics measurements requires a transverse momentum resolution at the **0.1% level** for leptons with momenta below 100 GeV/c.
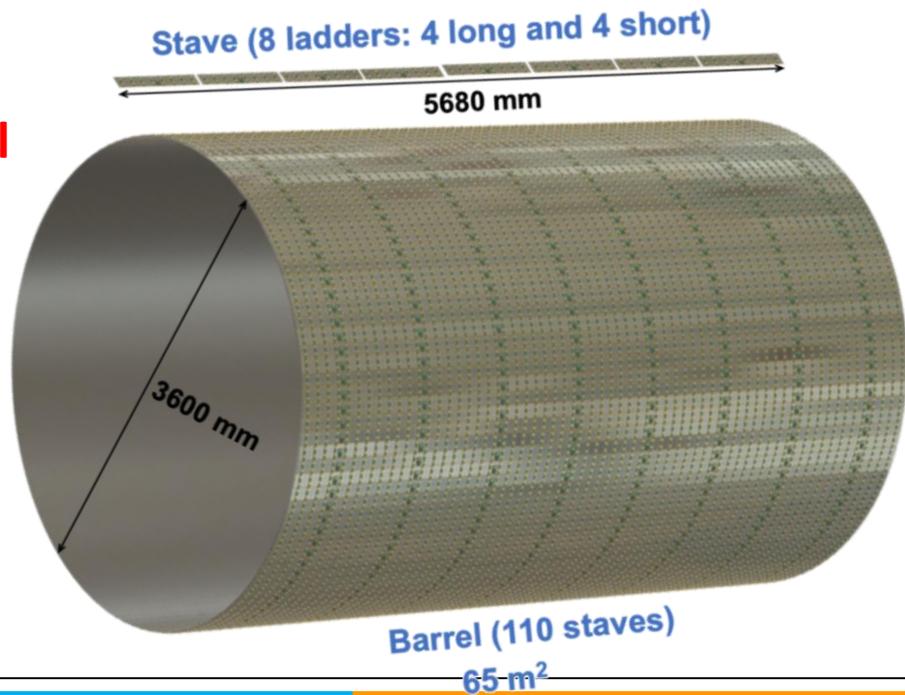
Effective Particle Identification is crucial for supporting flavor physics, searches for long-lived particles, and studies of jet substructure composition.

OTK is required to provides both high spatial (~10 μm) and timing resolution (~ 50 ps) while maintaining a low material budget of <1.6% X_0 per layer.

OTK Design

TPC
ITK
OTK

Ladder (8 modules)
104.5 mm
104.5 mm
699.6 mm
719.6 mm

Data Link

(2nd aggregation board)

Optical module

43.63   52.20

Module (4 sensors)

87.36   44.88   52.20

1st Data aggregation

DC-DC
ASIC
FPC

89.86

Barrel

Stave (8 ladders: 4 long and 4 short)
5680 mm

3600 mm

Barrel (110 staves)
65 m²

Endcap

1/16 Sector

Group D:
Group C:
Group B:
Group A:

r: 406mm - 1816mm

Group C Section

Power and FPC cable

Module (2 sensors)

FPC cable
Optical fiber module
Data Link

Design Including Cooling and Mechanics

OTK endcap 1/16 sector

Carbon Fiber closeouts

Cooling Plate
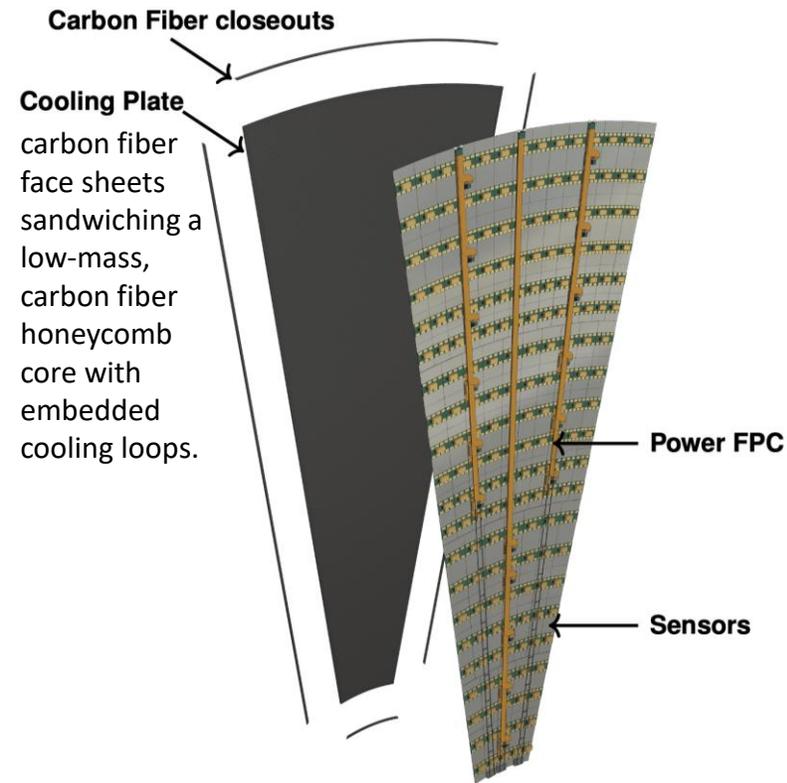carbon fiber face sheets sandwiching a low-mass, carbon fiber honeycomb core with embedded cooling loops.

Power FPC

Sensors

40 coil layer cooling loops

300 mW/cm² heat flux

Static Temperature

14.55
13.77
12.99
12.22
11.44
10.66
9.89
9.11
8.34
7.56
6.78
[C]

inlet
outlet

tube 5 tube 4 tube 3 tube 2 tube 1

❑ The OTK endcap 1/16 sector base line design uses 5-loop water cooling pipes with a pipe inner diameter of 2.3 mm, a flow velocity of 2 m/s, and an inlet temperature of 5°C.

❑ The sensor temperature is <15°C and cross sensor temperature gradient is <4°C.

Although water cooling has been adopted as the baseline due to its overall system simplicity, we have recently initiated R&D on dual phase CO_2 cooling.

Design Including Power and Readout Electronics

DC-DC (PAL48)
(48 V→12 V)

DC-DC converter
(12 V→1.2 V)

FEDI

OAT

FEDA

Optical fiber

FPC power bus 200 V
HV and 48V LV

The FEDA, FEDI, OAT, and PAL chips are under development by the CEPC team.

LATRIC

Front-End Data Aggregator (**FEDA**)

Front-End Data Interface (**FEDI**)

Optical Array Transceiver (**OAT**)

Fiber

Common data Board

Power At Load (**PAL**)

Power At Load (**PAL**)

Front End Board

Concentrator Card

Cable

Power

CLK Control

FEDA

FEDA

FEDA

FEDA

43.3 Mbps

43.3 Mbps

FEDA

1.39Gbps

347Mbps

FEDA

FEDA

FEDA

FEDA

43.3 Mbps

43.3 Mbps

FEDA

1.39Gbps

347Mbps

CHIP1

CHIP1

CHIP1

CHIP1
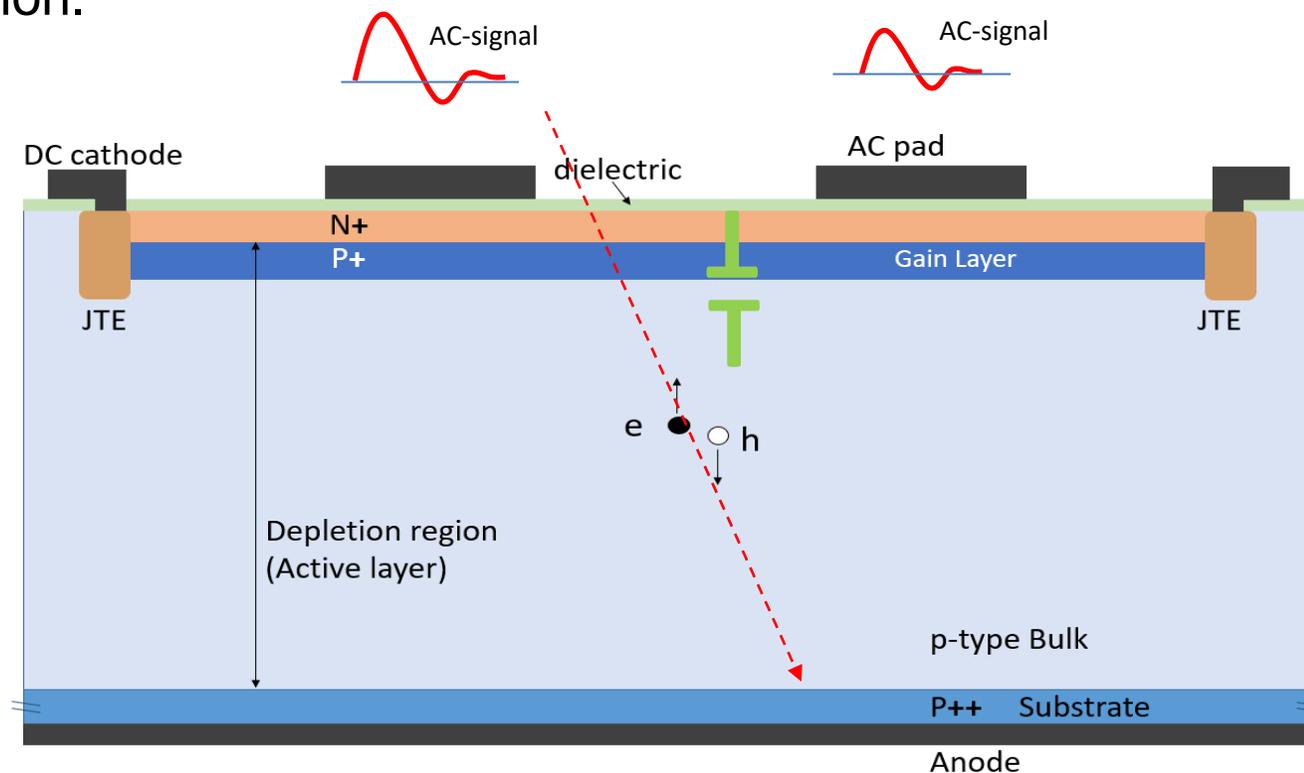
FEDI

2.77Gbps

11.09Gbps

OAT

AC-LGAD for CEPC OTK with Precision Timing

■ **AC-coupled LGAD:**

- A thin dielectric layer (Si3N4 or SiO2) separates the metal AC pads from the N+ layer.
- Position information is determined by charge shared between pads.
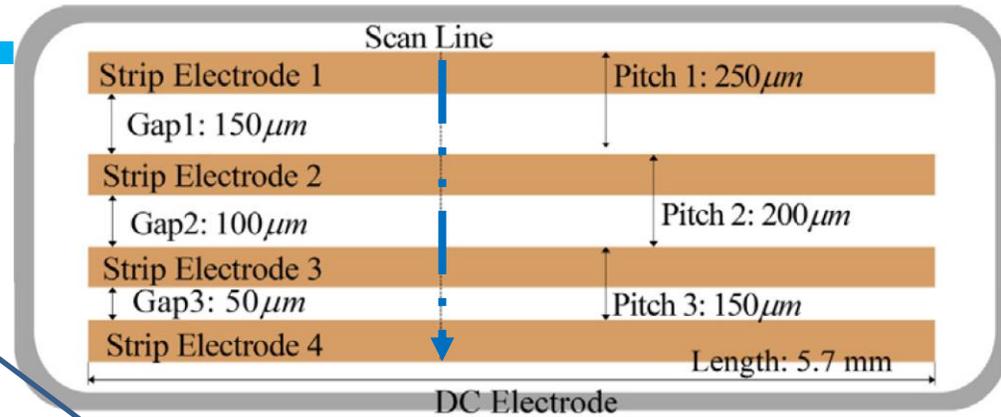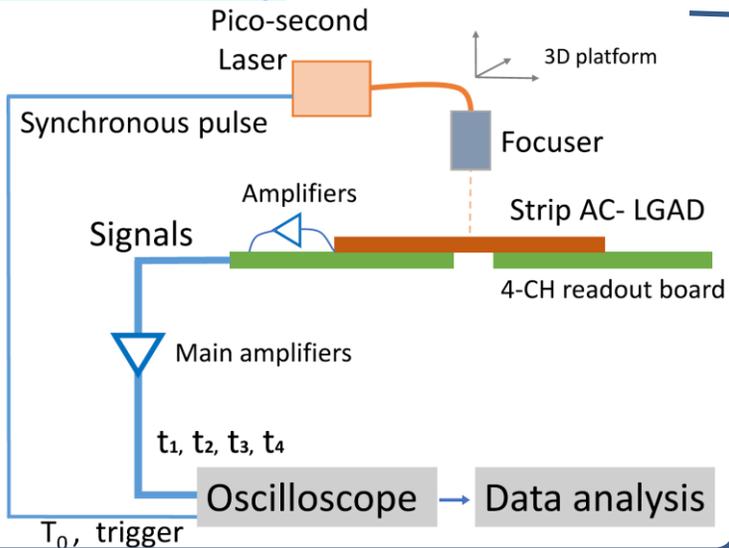- Less dead area and better position resolution.

■ Key parameters of AC-LGAD microstrip sensor for OTK:

- Sensor size: (3-4.5) cm × (3-5) cm
- Strip number: 512 or 384
- Sensor thickness: 300 μm
- Pitch size: ~100 μm
- Spatial resolution: 10 μm
- Time resolution: 50 ps
- Power consumption: 300 mW/cm^2
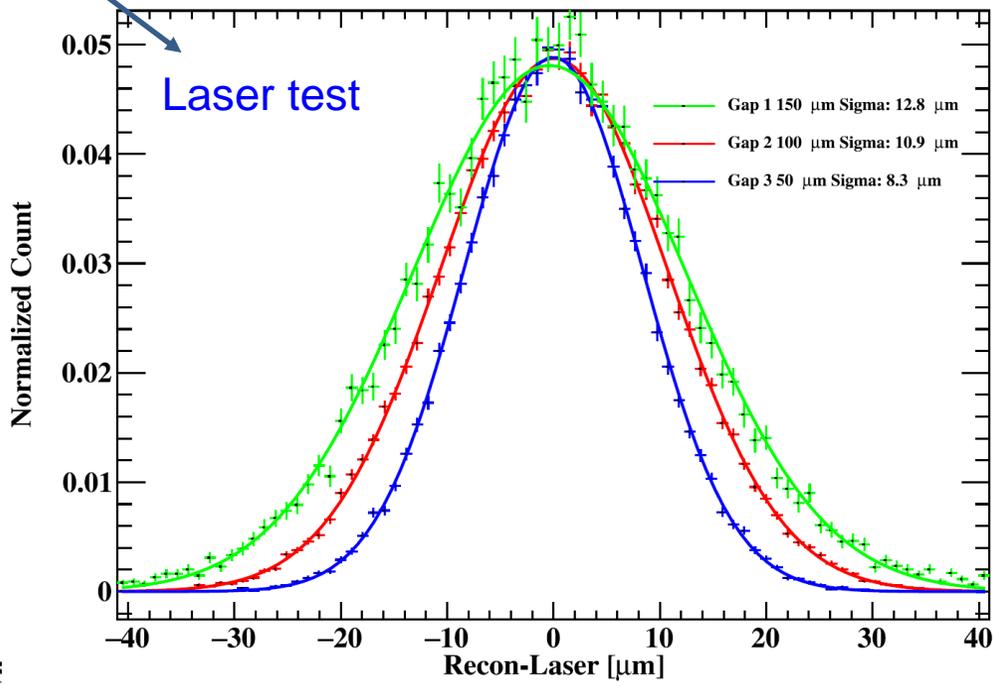
AC-LGAD V0 Performance: Time and Spatial Resolution

Laser test setup

^{90}Sr test setup

NIM A, Volume 1062, May 2024, 169203

^{90}Sr Beta source test

$$\sigma_{\text{DUT}} = \sqrt{\sigma_{\Delta T}^2 - \sigma_{\text{trigger}}^2}$$

Laser test

Scan Line
Strip Electrode 1 — Pitch 1: 250 μm
Gap1: 150 μm
Strip Electrode 2 — Pitch 2: 200 μm
Gap2: 100 μm
Strip Electrode 3
Gap3: 50 μm — Pitch 3: 150 μm
Strip Electrode 4
Length: 5.7 mm
DC Electrode

Gap 1 150 μm Sigma: 12.8 μm
Gap 2 100 μm Sigma: 10.9 μm
Gap 3 50 μm Sigma: 8.3 μm

Time resolution: 37.5 ps
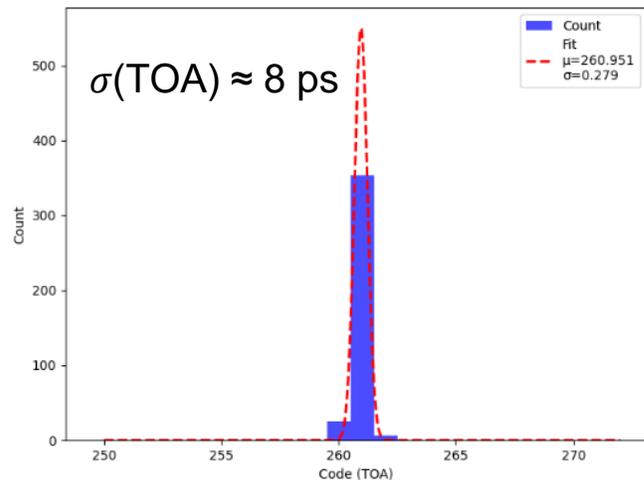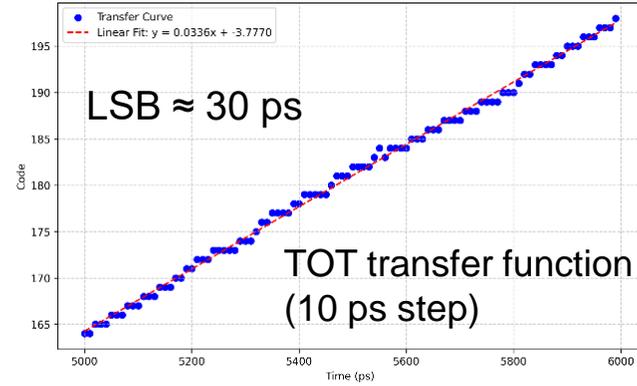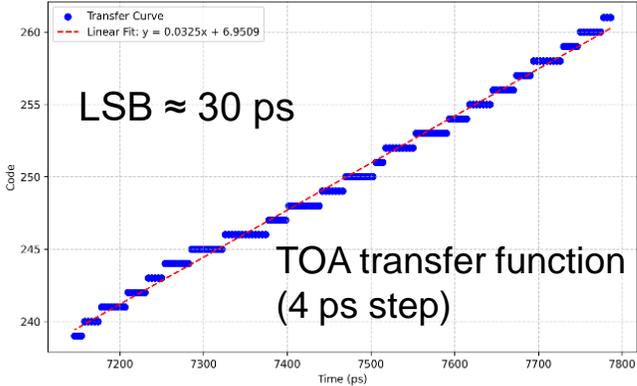
Spatial resolution:
8 μm for 150 μm strip pitch

LGAD Readout ASIC (LATRIC)

Latest result

- The **first LATRIC prototype, LATRIC-V0** integrates a pre-amplifer, a discriminator, a TDC, and a serializer.

- Tests find that the **LSB is 29.8 ps**, meeting the 30ps design goal.

- The measured TDC **power consumption is 0.1 mA (1.2 V) @ 0.5 MHz**, 0.3 mA @ 1 MHz, and 0.5 mA @ 2 MHz, agreeing with the design.
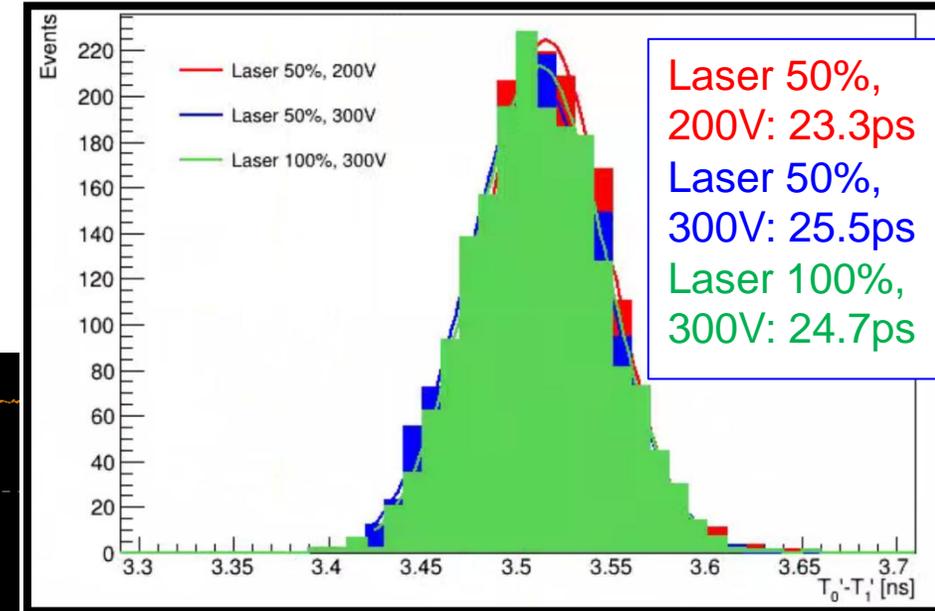

LSB ≈ 30 ps

TOA transfer function (4 ps step)

LSB ≈ 30 ps

TOT transfer function (10 ps step)

σ(TOA) ≈ 8 ps

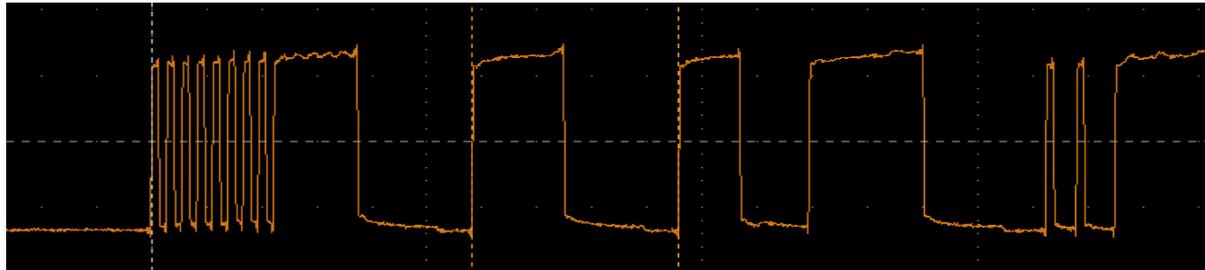σ(TOT) ≈ 12 ps

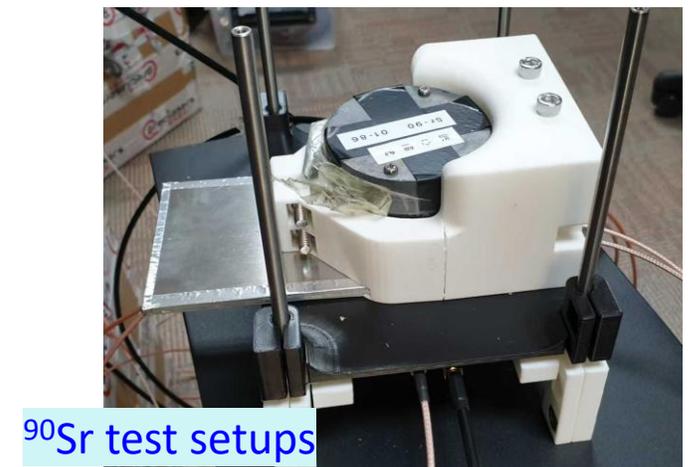LATRIC-V0 layout

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AC-LGAD and LATRIC Combined Test

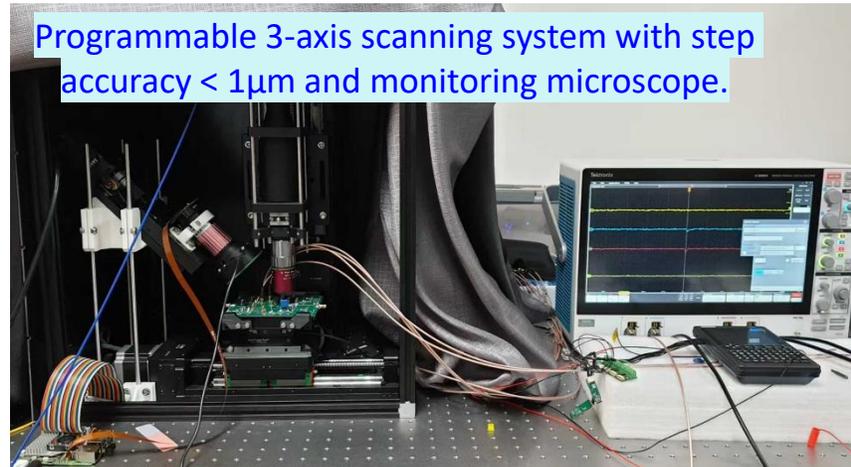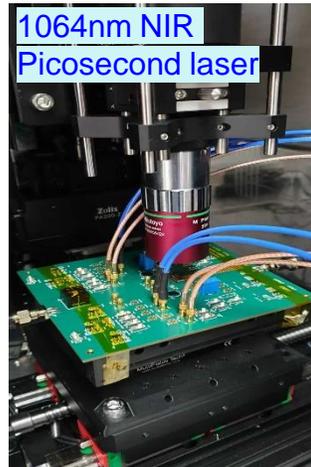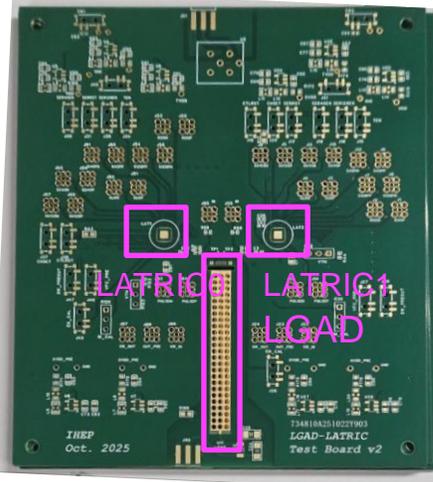Preliminary time resolution measured with two LATRICs

- **The combined test of the LGAD and LATRIC ASIC is currently ongoing:**
  - The first test board, integrating two LATRIC (V0) chips and one LGAD sensor, has been fully designed and fabricated.
- **New and improved laser and ^{90}Sr test setups** for measuring time and position resolutions have been built.

AC-LGAD signal → LATRIC's 128 bits raw data packet @720Mhz captured with oscilloscope!!!

Laser 50%, 200V: 23.3ps
Laser 50%, 300V: 25.5ps
Laser 100%, 300V: 24.7ps

Laser test setup

1064nm NIR Picosecond laser

Programmable 3-axis scanning system with step accuracy < 1μm and monitoring microscope.

LATRIC0   LATRIC1
LGAD

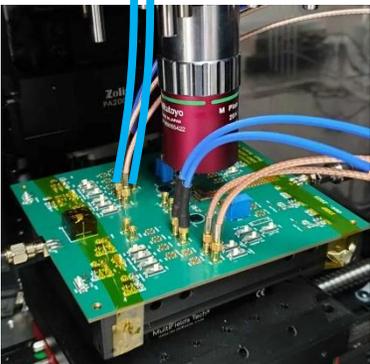IHEP Oct. 2025   LGAD-LATRIC Test Board v2

^{90}Sr test setups

DAQ Setup for AC-LGAD+LATRIC Test

- A high-speed versatile DAQ system is crucial throughout the entire lifecycle of sensor and module development, integration, and validation. It must:
  - accommodate different test setups or sensor/ASIC types.
  - implement real-time data processing, triggering, monitoring, and calibration routines.
  - provide comprehensive electrical and functional testing of fully integrated prototype module/detector.
  - support future lab tests as well as the beam test scheduled for the Q3 of 2026.

720MHz Clk

720MHz Clk

KCU105 Evaluation Board

Linux host
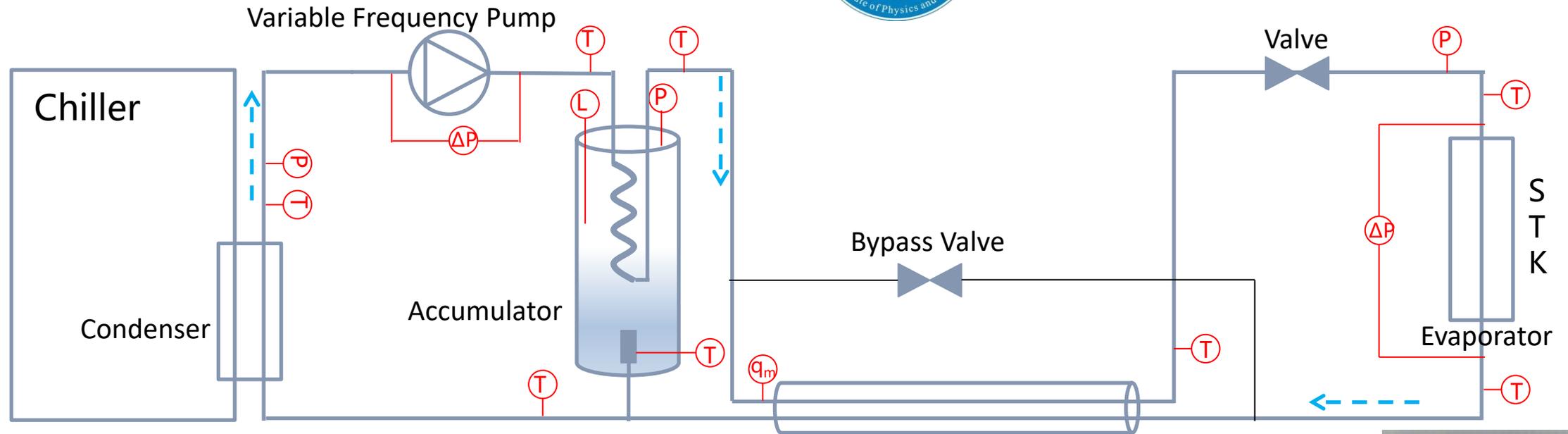
FMC LPC Fan-out Board

128-bit data @720MHz

Trigger/Control

Optical Link

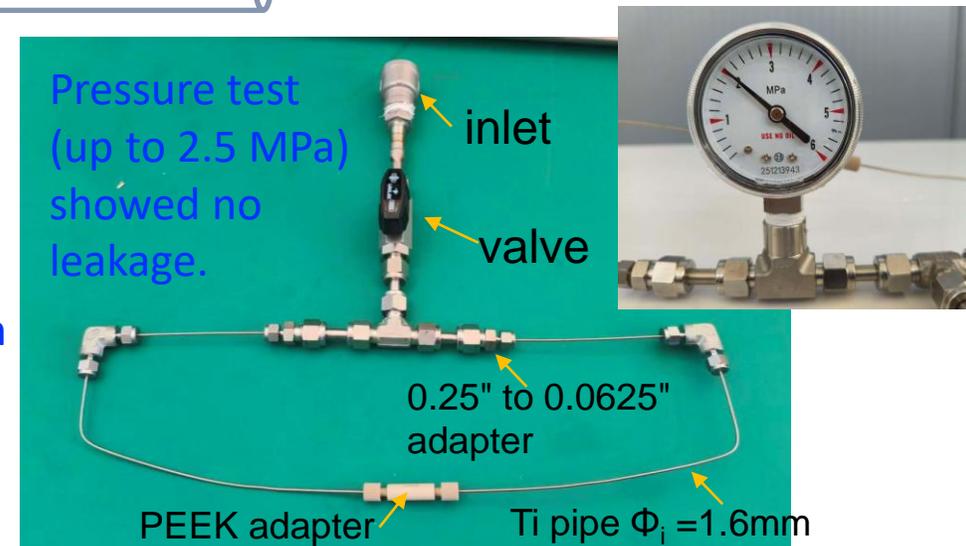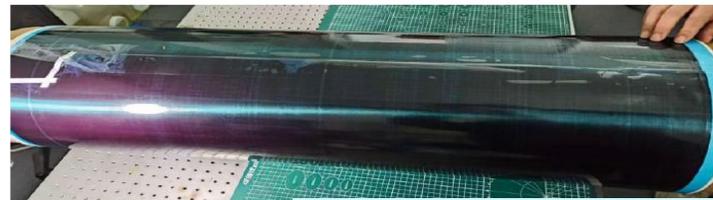**AC-LGAD + LATRIC evaluation board_v0**

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Dual-Phase CO$_2$ Cooling

- Cooling Capacity: 0.75 kW (upgrading to higher power (1.5 kW) only requires replacing the chiller)

- Temperature Range: -30 to 20°C (±0.5 °C)

- Pressure: 2 MPa (-20°C), maximum supported 7 MPa (70 atmospheres)

- Compact and versatile suitable for various heat load systems, both within and outside the scope of the CEPC
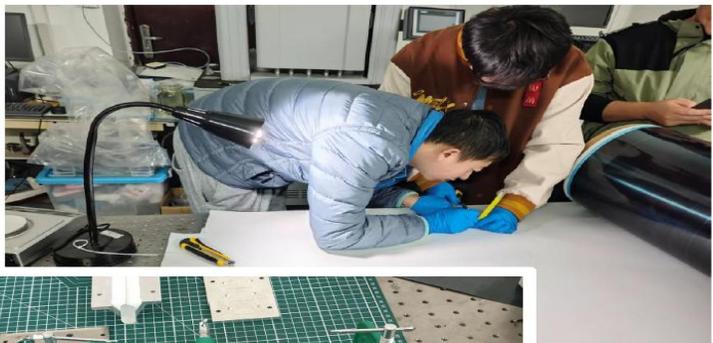
The goal is to deliver the first two-phase CO₂ cooling prototype system (including the integrated control host system) by mid-2026.
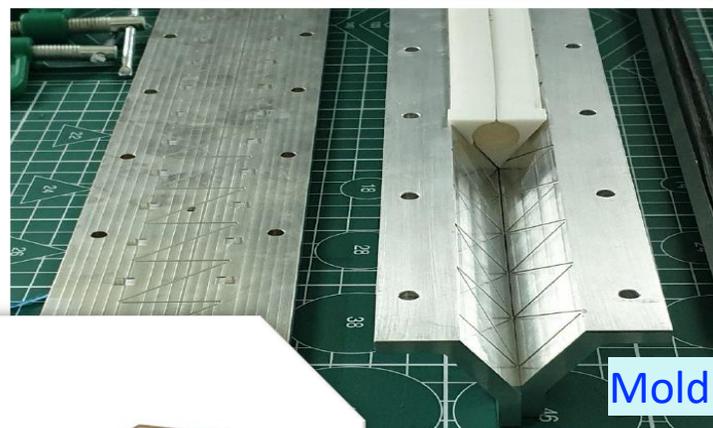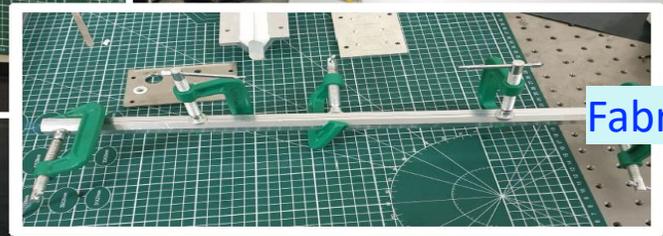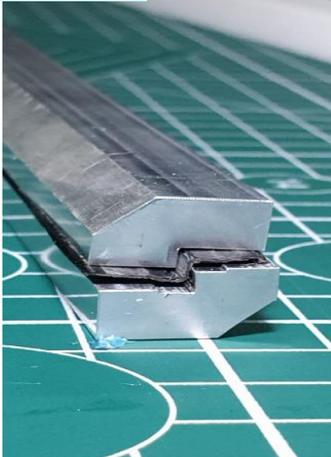
Pressure test (up to 2.5 MPa) showed no leakage.

inlet

valve

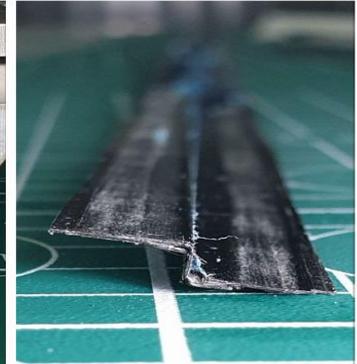0.25" to 0.0625" adapter

PEEK adapter
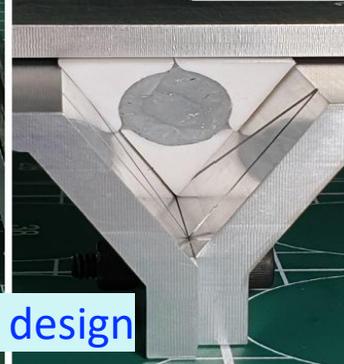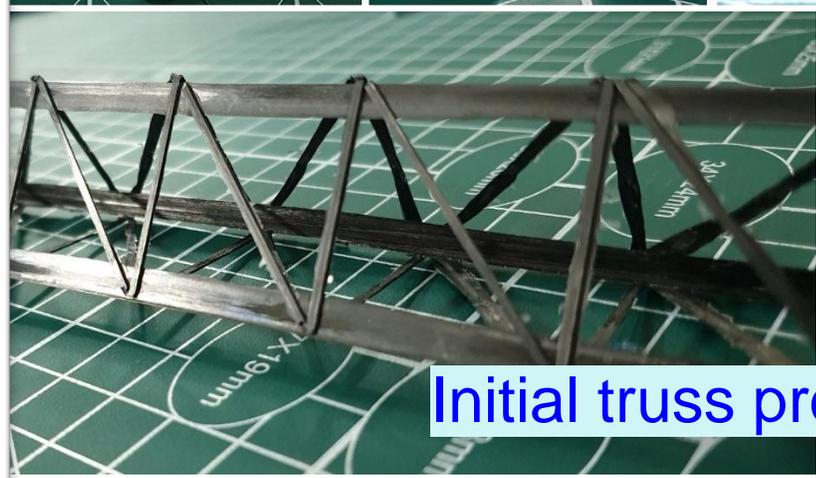
Ti pipe Φ$_i$ =1.6mm

Recent development

Carbon Fiber Support Structures

Raw material procurement

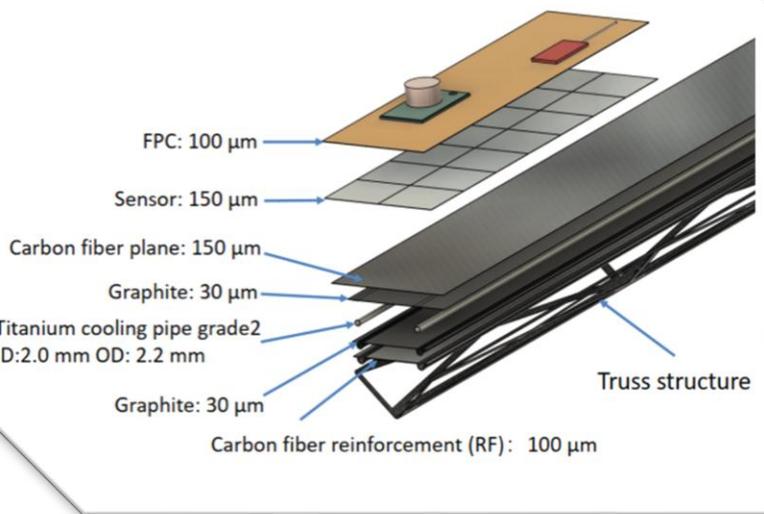Fabrication techniques

Mold design

FPC: 100 μm
Sensor: 150 μm
Carbon fiber plane: 150 μm
Graphite: 30 μm
Titanium cooling pipe grade2 ID:2.0 mm OD: 2.2 mm
Graphite: 30 μm
Carbon fiber reinforcement (RF): 100 μm
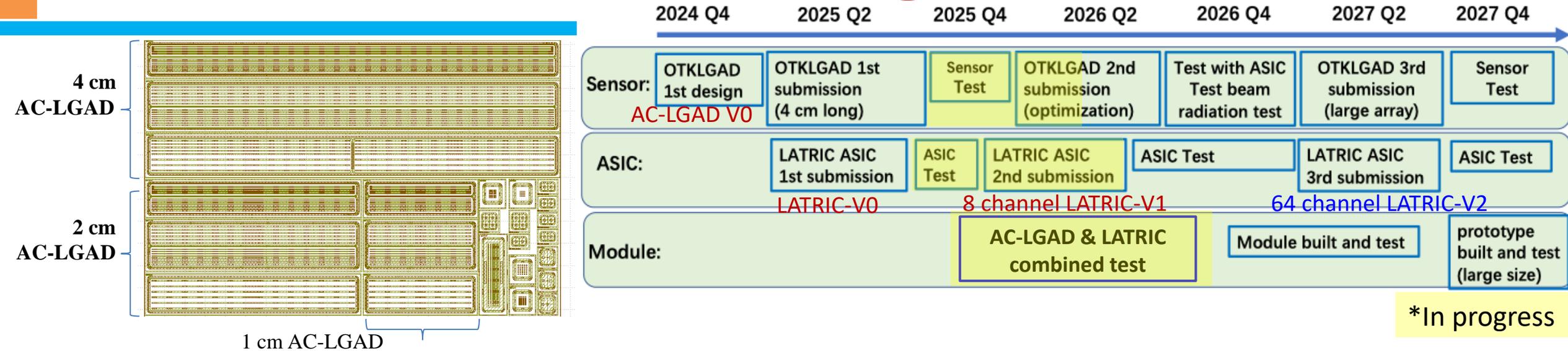Truss structure

Initial truss prototypes

R&D Plan Following the Ref-TDR

4 cm AC-LGAD

2 cm AC-LGAD

1 cm AC-LGAD

	2024 Q4	2025 Q2	2025 Q4	2026 Q2	2026 Q4	2027 Q2	2027 Q4
Sensor:	OTKLGAD 1st design	OTKLGAD 1st submission (4 cm long)	Sensor Test	OTKLGAD 2nd submission (optimization)	Test with ASIC Test beam radiation test	OTKLGAD 3rd submission (large array)	Sensor Test
	AC-LGAD V0						
ASIC:		LATRIC ASIC 1st submission	ASIC Test	LATRIC ASIC 2nd submission	ASIC Test	LATRIC ASIC 3rd submission	ASIC Test
		LATRIC-V0		8 channel LATRIC-V1		64 channel LATRIC-V2	
Module:				AC-LGAD & LATRIC combined test	Module built and test		prototype built and test (large size)

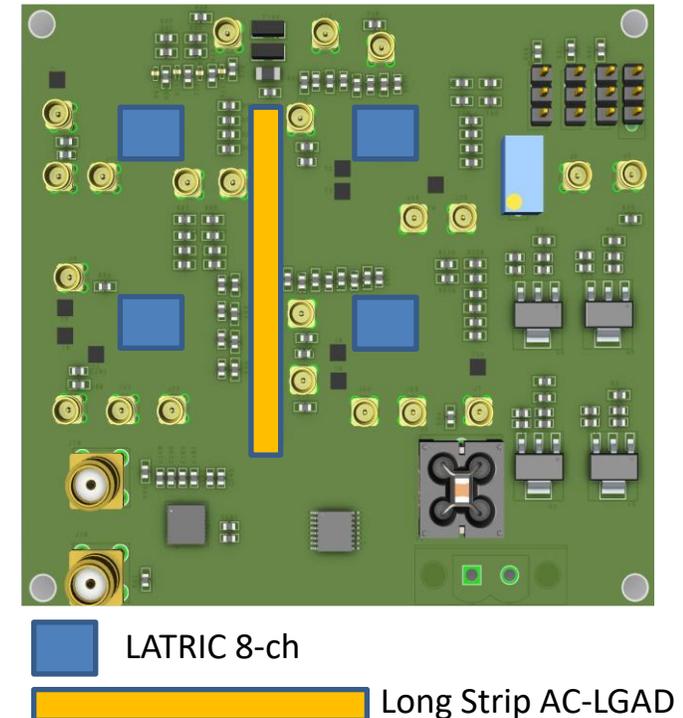*In progress

- The latest AC-LGAD sensor v1 was submitted for tape-out in Oct 2025 and is now undergoing dicing.

- **AC-LGAD** sensors are advancing toward improved process, larger size, higher performance, and lower power consumption
  - The newly developed trenched-isolation LGAD is an important step: reducing the capacitance and, consequently, power consumption.

- **LATRIC**, moving towards multi-channels:
  - The 8-channel LATRIC-V1 was submitted for tape-out in Oct 2025.
  - The next step will be the development of a 32-channel version by July 2026.

$$C = \varepsilon_0 * \varepsilon_r * A \downarrow / d$$

Isolated structure

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R&D Plan (continue)

- Improve laser and beta source test setup and produce new AC_LGAD—LATRIC test board.

- A beam telescope is under development, with a full-system beam test planned for Q3-2026.

- In parallel, the development of:
  - Multi-channels high speed DAQ system
  - Carbon fibre support structures and
  - Dual phase CO_2 cooling prototype

  are ongoing.

LATRIC 8-ch

Long Strip AC-LGAD

Goal: A functional detector prototype meeting CEPC detector requirements by the end of 2027.

Our Research Team

- Currently active: 29 institutes, 50 staff, and 50+ postdocs & students

We welcome collaboration with partners worldwide.
（欢迎有兴趣的单位和我们一道合作，从技术开始做起，一起研发，并在这一关键探测器技术领域深耕。）

Summary

- The baseline design of the CEPC Silicon Outer Tracker and the latest R&D progress have been presented.

- Our next major focus will be on R&D, aiming key technology achievements and prototype detector development. Ongoing efforts in sensor technology, readout electronics, mechanical prototypes, and cooling systems are steadily advancing toward the goal of completing a Silicon Tracker prototype by the end of 2027.

- These advancements are crucial to meet the stringent performance requirements of the CEPC Silicon Tracker and ensuring the overall success of the CEPC project.

Thank you for your attention!

CEPC Ref-TDR

IHEP-CEPC-DR-2025-01
IHEP-EP-2025-01

CEPC Reference Detector
Technical Design Report

Version: v1.0.0 build: 2025-10-08 00:09:14Z

arXiv:2510.05260v1 [hep-ex] 6 Oct 2025

The CEPC Study Group
October, 2025

❑ The CEPC Detector Technical Report (Ref-TDR) was released in Oct 2025:
arXiv:2510.05260

LGAD Sensor Development at IHEP

- The LGAD (Low Gain Avalanche Detector) sensor developed by IHEP achieves both precise position and time measurements under high radiation levels.

IHEP(2019)   IHEP (2020.9)   IHEP (2021.6)
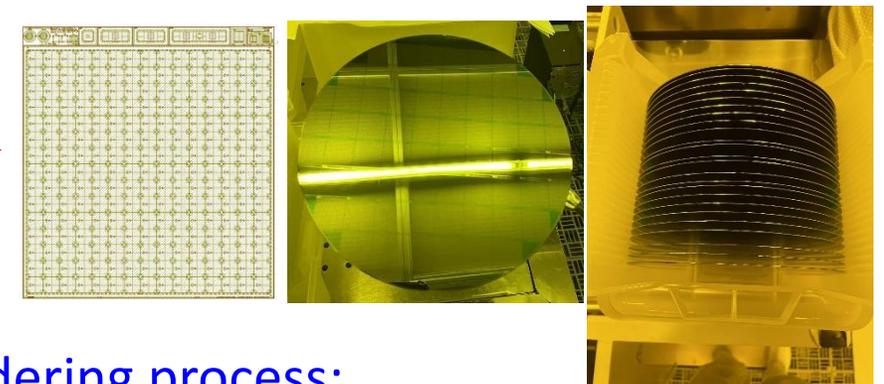

See details in Mei Zhao's talk

IHEP (2022.5)   Pre-production for ATLAS (2023.7)   Mass production for ATLAS since 2024.6

- In May 2023, CERN selected IHEP in the HGTD sensor tendering process:
  – First time a domestic silicon sensor was chosen by CERN for an LHC experiment.

OTK Endcap Design with AC-LGAD Strip Sensor
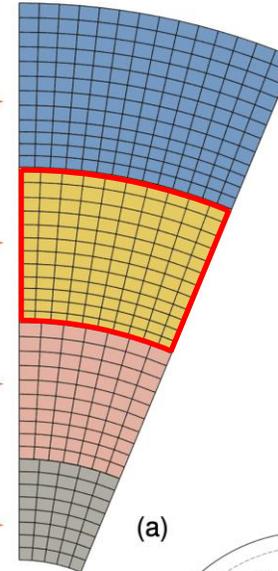
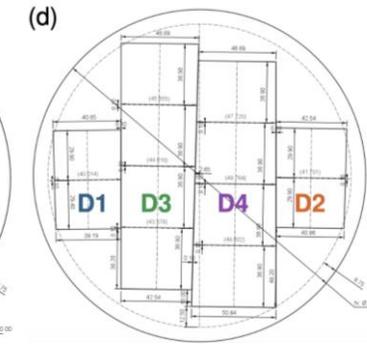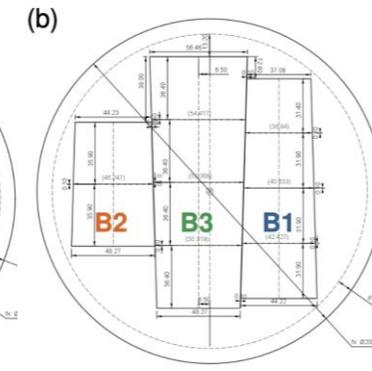Endcap (16 sectors, 10 m^2)

1/16 Sector

Sensor: 8'' wafer (group C sensors)

Group D:
1400mm-1816mm

Group C:
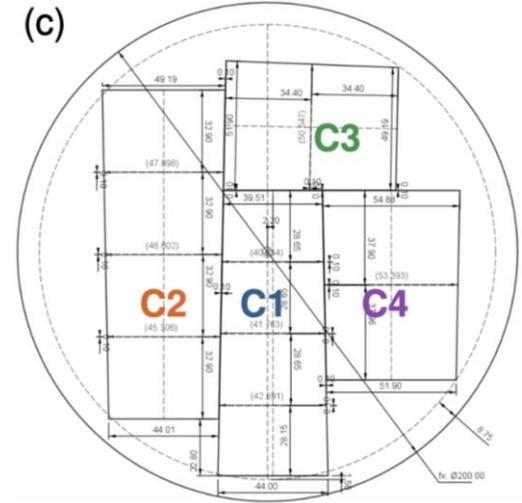1008mm-1400mm

Group B:
662mm-1008mm

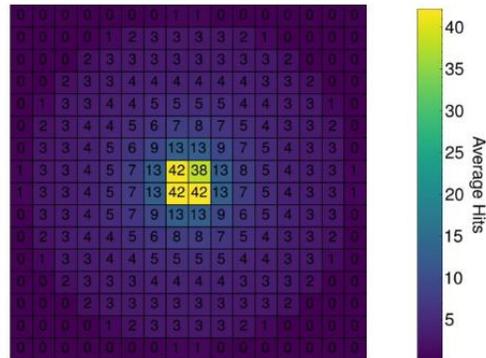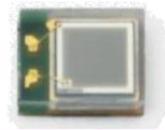Group A:
406mm-662mm

1816mm

406mm

- OTK endcap consists of 42 rings, arranged into 4 groups.
- Each group contains 2-4 subgroups of trapezoid sensors, dicing from one 8'' silicon wafer.
- Each group of sensors is aligned to a 1/16 sector.
  - Strip pitch : 80.59-113.03 μm
  - Strip length : 28.1-36.3 mm

OTK endcap has a total surface area of 20 m², including 12,736 sensors and 46,336 ASICs, with a power consumption of ~60 kW.
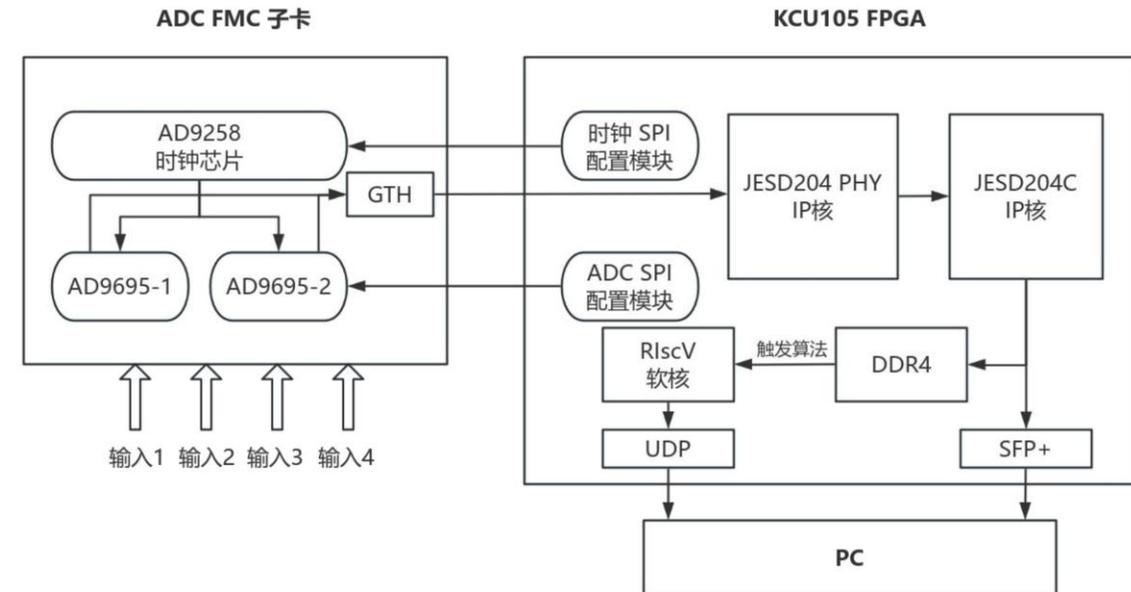
8'' wafer (group A, B, D sensors)

Maximize silicon wafer utilization and reduce masks (only 4 required), while facilitating detector assembly.

High Speed ADC Sampling

- **Standalone AC-LGAD sensor beam test:**
  - with quartz Cherenkov Telescope for trigger, which requires a low-latency, high-reliability FPGA + ADC readout solution.
- **The preliminary ADC development is based on AD9695:**
  - four channels at 1.25 Gsps,
  - 14 bits
  - 400 kHz to 500 MHz input bandwidth

Quartz (Cherenkov) + SiPM readout planed for LGAD trigger

Development of a System on Chip (SoC)

- ASIC development is costly, offers limited configurability, and difficult to implement on-chip algorithm integration. System-on-Chip (SoC) architectures—including CPU, memory, bus, and peripherals—represent the future trend of ASIC development. RISC-V–based ASICs offer unique advantages in flexibility and rapid iteration, enabling better support for the diverse requirements of HEP experiments, as well as configurable control and complex on-chip algorithms. The first RISC-V chip developed was submitted for tape-out in October, with testing planned next. The next R&D phase will focus on radiation-hardening, full integration with the LATRIC ASIC, and further applications in system-level control, front-end on-chip computing, and AI integration for HEP experiments.
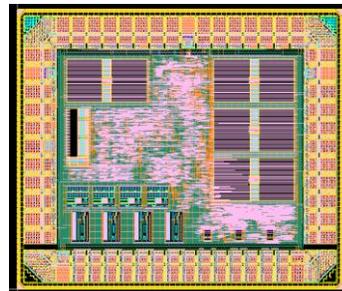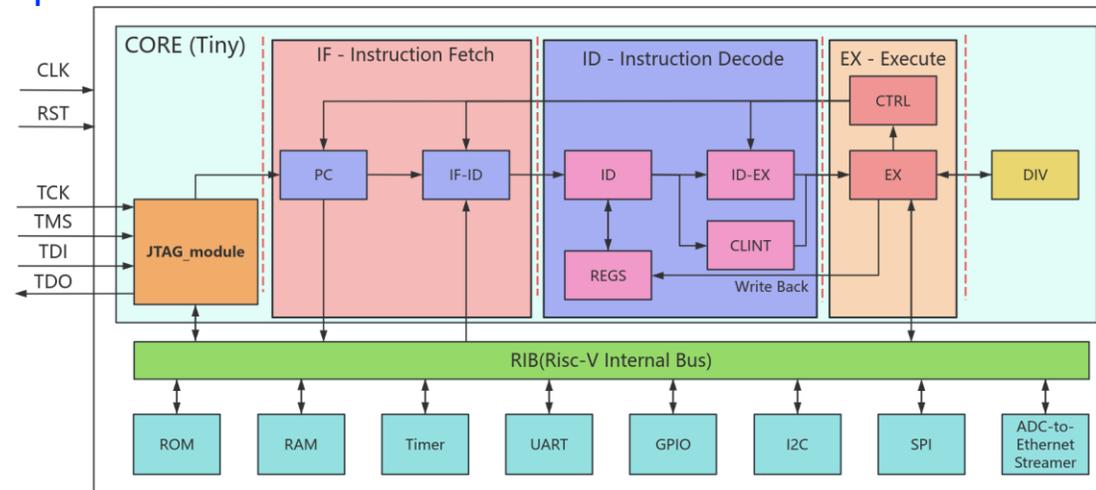
> Core (Tiny RiscV)
> - RV32IM Core
> - 3 stage pipeline
> - CoreMark/MHz = 2.4

> JTAG Interface
> - OpenOCD support
> - GDB debugging support

> Peripherals
> - 4 KB ROM, 32 KB RAM
> - Supports multiple serial communication protocols, such as I2C, UART, and SPI
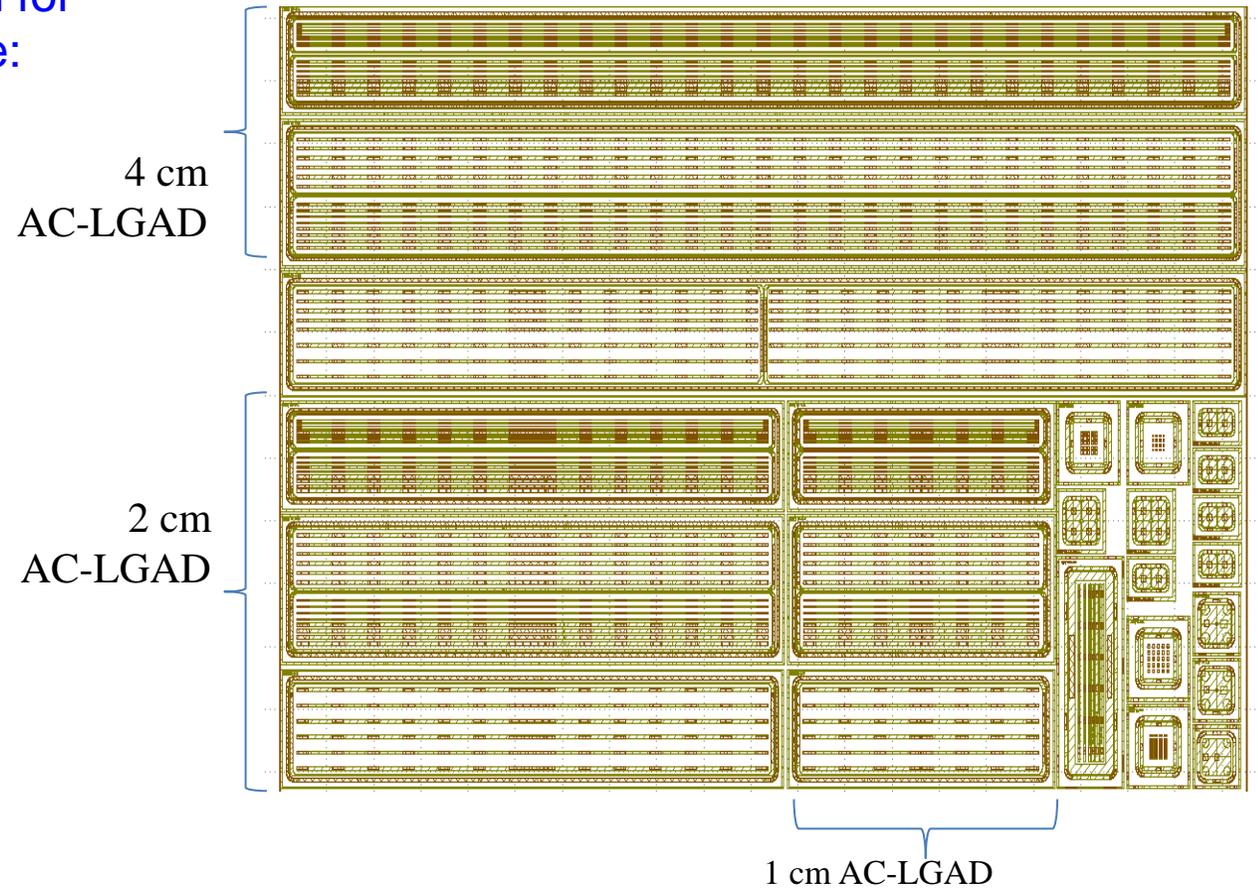> - Integrated sensor data processing and UDP forwarding

- 55 nm process technology
- Frequency 50 MHz
- Size 1020 x 1196 um
- Supply Voltage 1.2 V
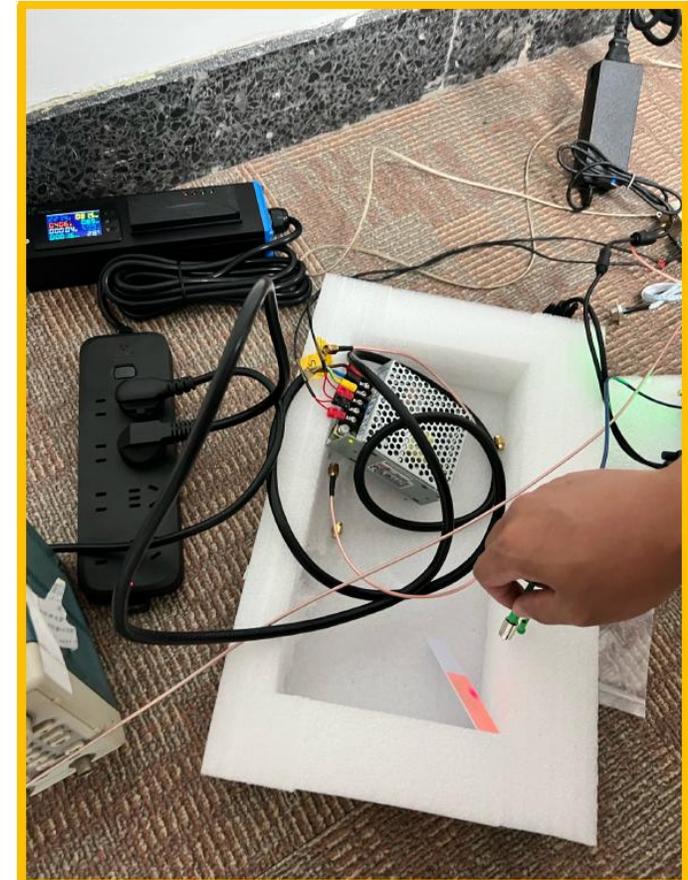- Characterization will be performed in Q1 2026

AC-LGAD with Long Strip

New IHEP AC-LGAD strip sensor prototype: summitted for tap-out in Oct 2025. The new layout and design include:

- Strip lengths: 1 cm, 2 cm, and 4 cm

- Strip pitch sizes: 100 µm, 200 µm, and 500 µm

- Electrode widths: 25 µm, 50 µm, and 100 µm

- Isolated structure design and EPI thickness(50 µm, 80 µm) to reduce sensor capacitance (correlated with power consumption)

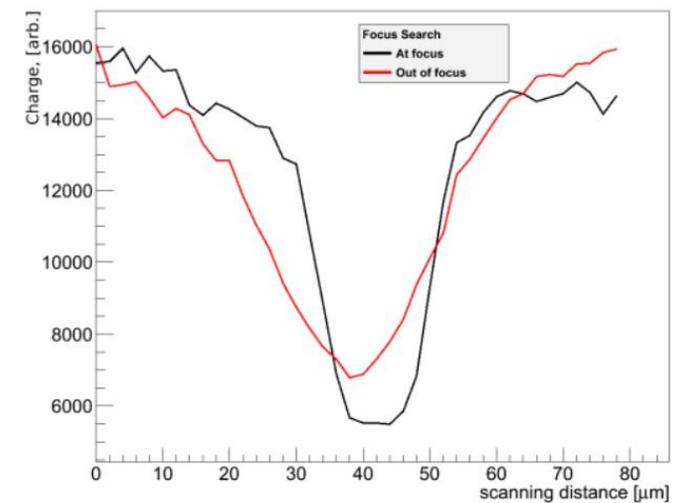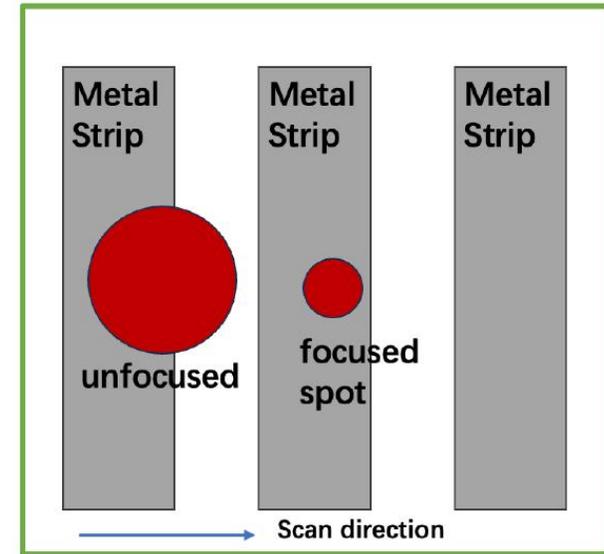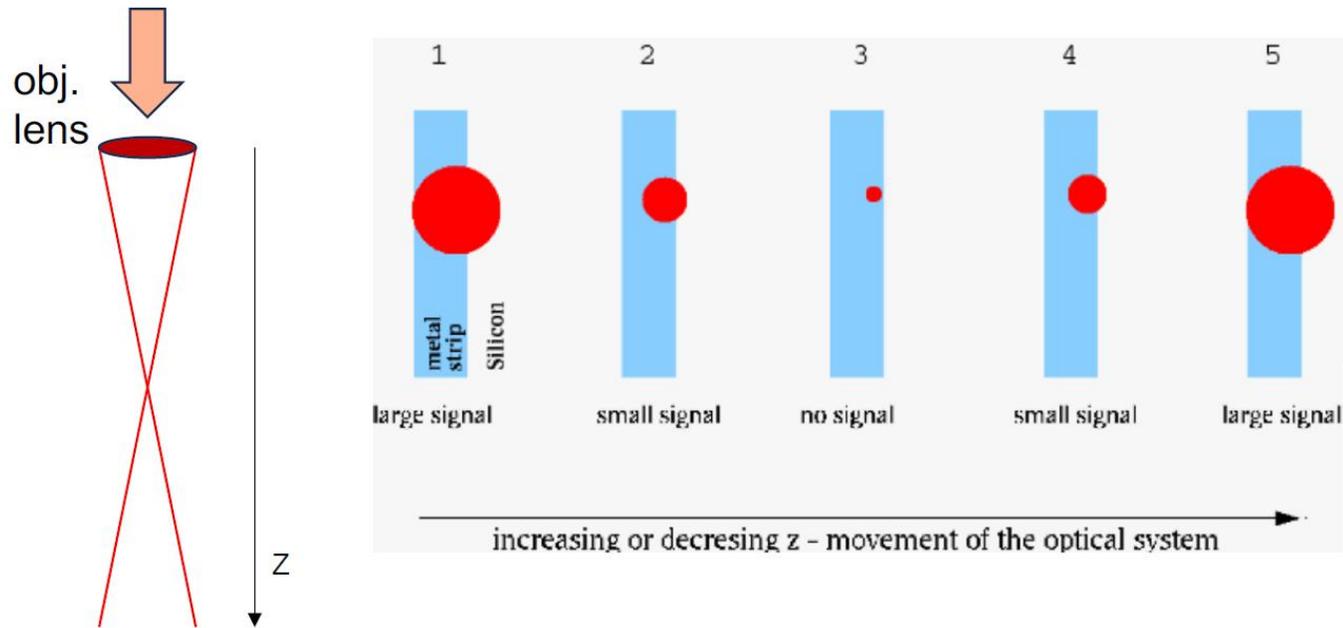- Process design optimization (n+ doping concentration) for better spatial resolution

4 cm AC-LGAD

2 cm AC-LGAD

1 cm AC-LGAD

NIR Picosecond Laser

Center wavelength: 1064 nm

Pulse width: < 8 ps

Pulse energy: 0.5 – 3 nJ

Average power: 6 – 200 mW

Peak power consumption: > 350 W

Spectral width: < 0.5 nm

Repetition rate: 20 MHz

Polarization extinction ratio: > 100 : 1

Power stability: < 1 % RMS @ 3 h

Beam quality: TEM_{00}, $M^2 < 1.1$

Output: Polarization-maintaining fiber

Cooling: Air cooling

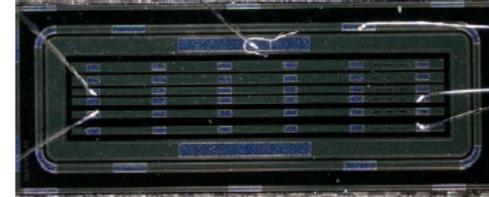# Focusing & Alignment

obj. lens

z

Two different methods for focusing adjustment
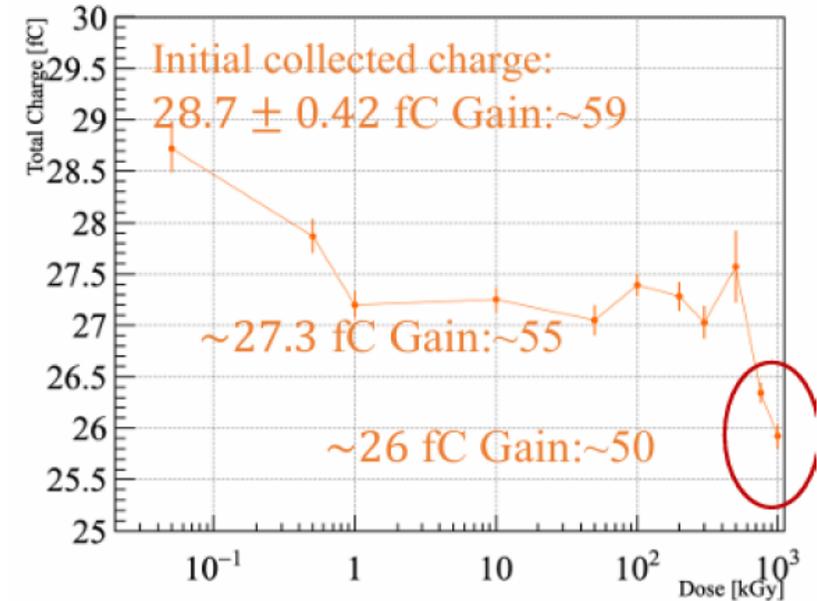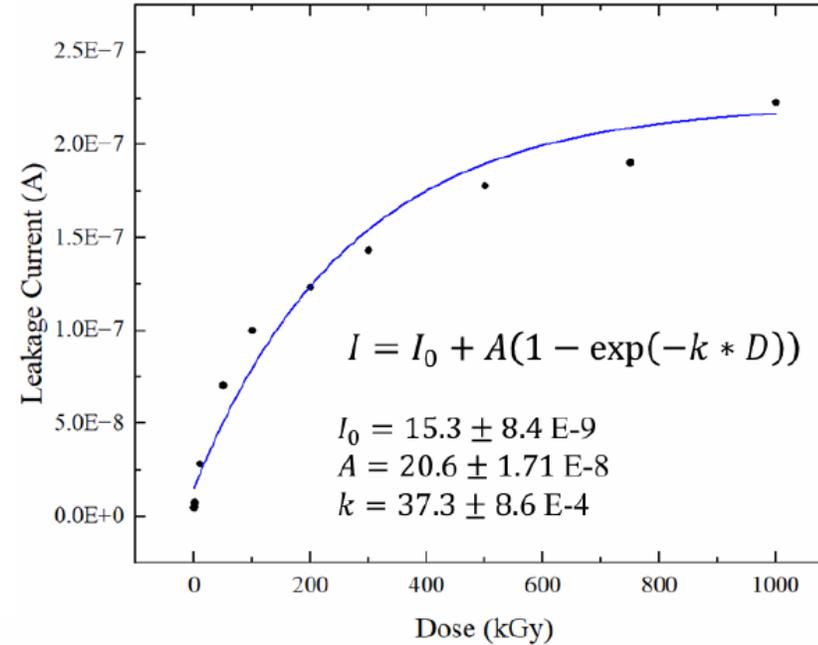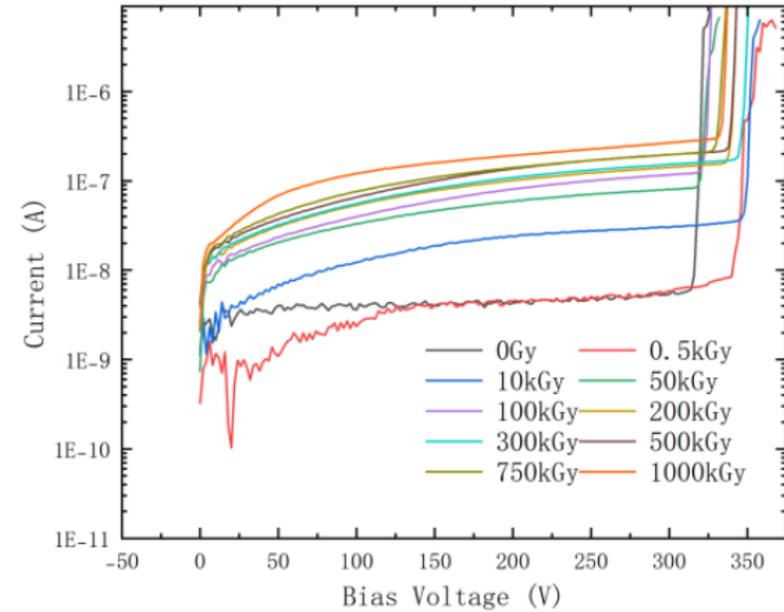
AC-LGAD test: TID

TID Impact on IHEP AC-LGAD Strip Sensors:
Irradiation: Multi-Rad 160 X-ray@40keV, up to 1MGy

Done by Weiyi Sun from IHEP

- Strip length 5.65mm
- pad-pitch size:
  100-250 um
  100-200 um
  100-150 um

$$I = I_0 + A(1 - \exp(-k * D))$$

$I_0 = 15.3 \pm 8.4 \text{ E-9}$
$A = 20.6 \pm 1.71 \text{ E-8}$
$k = 37.3 \pm 8.6 \text{ E-4}$

Initial collected charge:
28.7 ± 0.42 fC Gain:~59

~27.3 fC Gain:~55

~26 fC Gain:~50

➤ Collected charge reduces, but very less up to 1MGy.

➤ Leakage current increases by one order for sensors with TID dose as 1MGy
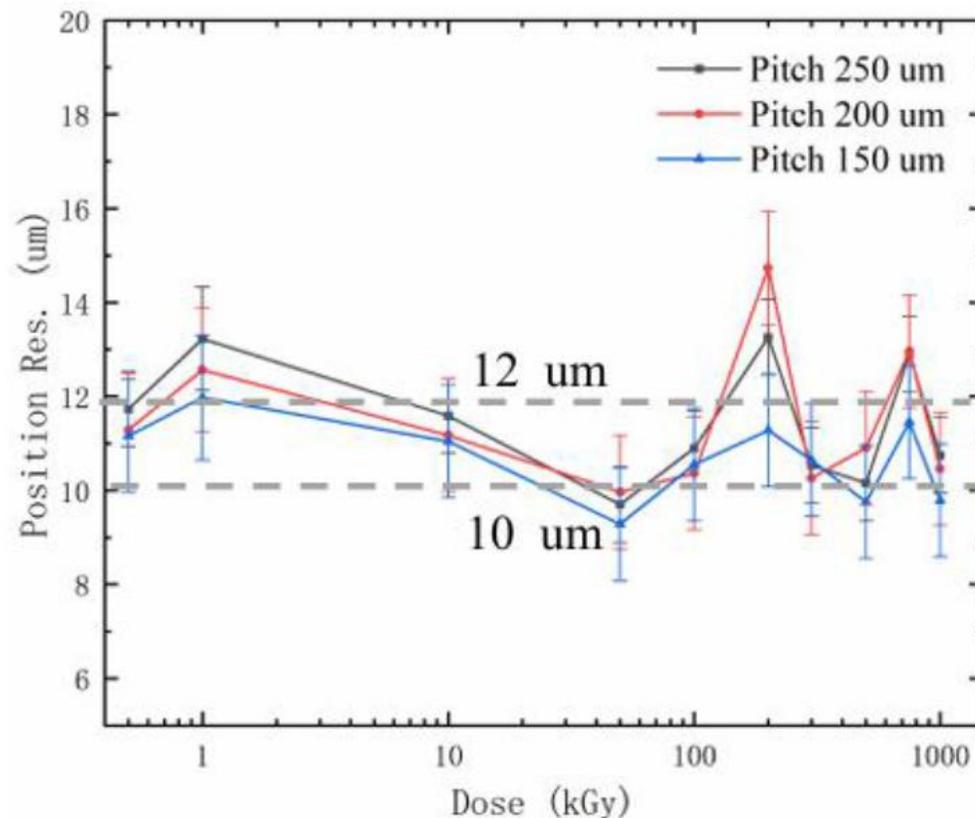
AC-LGAD test: TID

TID Impact on IHEP AC-LGAD Strip Sensors performance:

Done by Weiyi Sun from IHEP

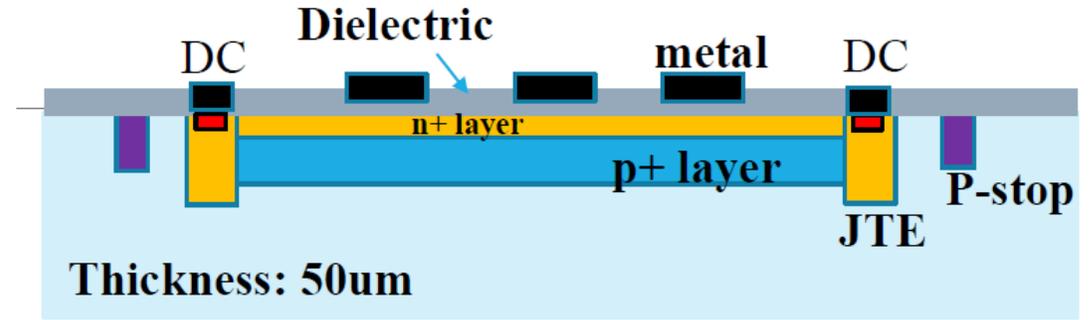➤ Time resolution degrades from 38ps to 42ps.

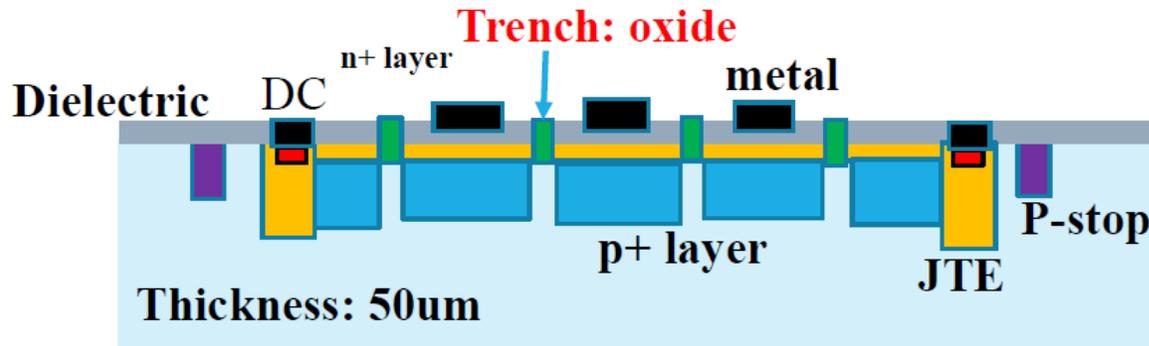➤ Spatial resolution maintained in 10-12 μm up to 1 MGy
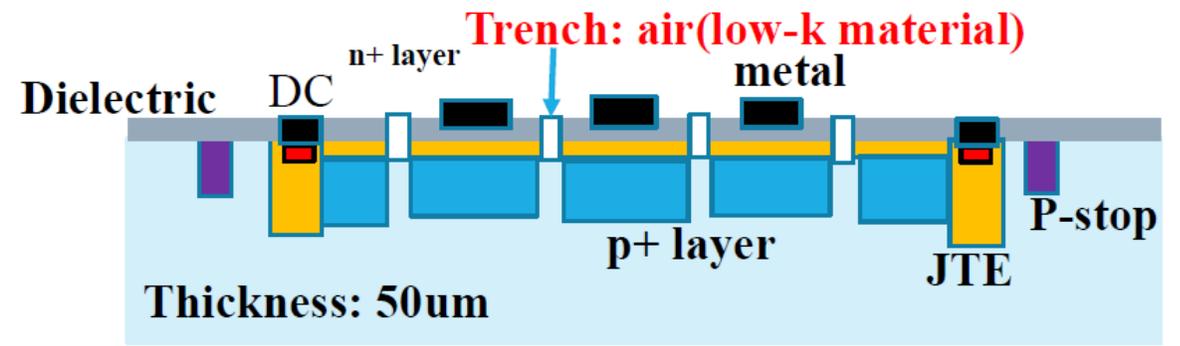
Isolated AC-LGAD simulation and design

- Trench isolation structure be added to reduce the bulk and inner-strip capacitance, critical for power consumption.
- Sensors with 3 types of structures be simulated using TCAD tools.
- Sensor performance been simulated:
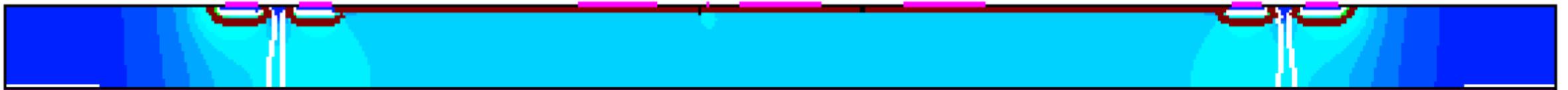 I-V; C-V: bulk capacitance, coupling capacitance, inter-strip capacitance;
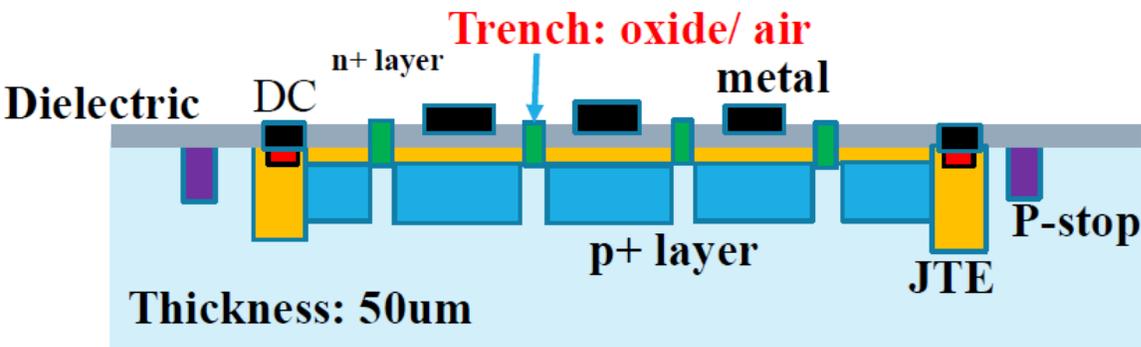

Type 1

Type 2

Type 3

Isolated AC-LGAD Simulation and Design

Trench: oxide/ air

Dielectric DC n+ layer metal

Trench: oxide/ air

p+ layer

JTE P-stop

Thickness: 50um

Type 2&3

Trench width:

➤ I-V performance will change as changing the trench width[type 2 and type 3].

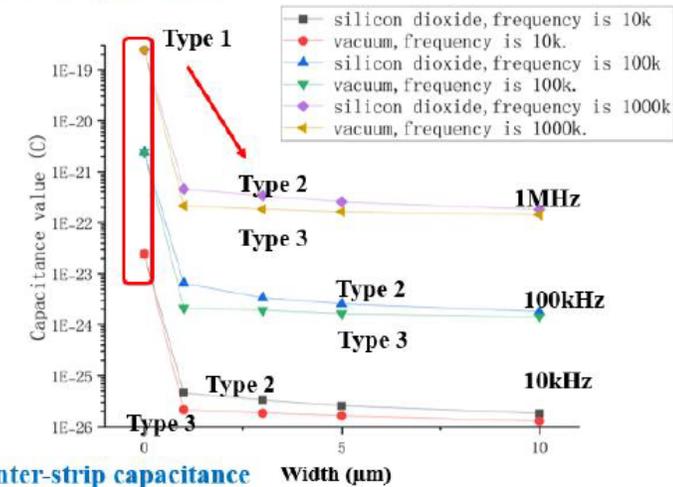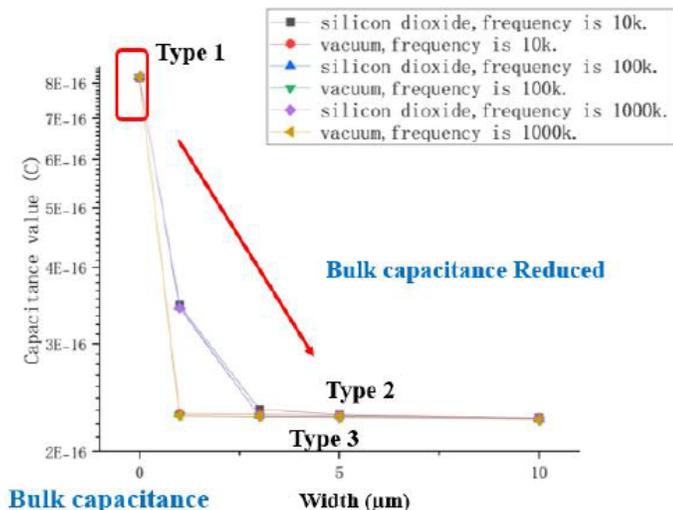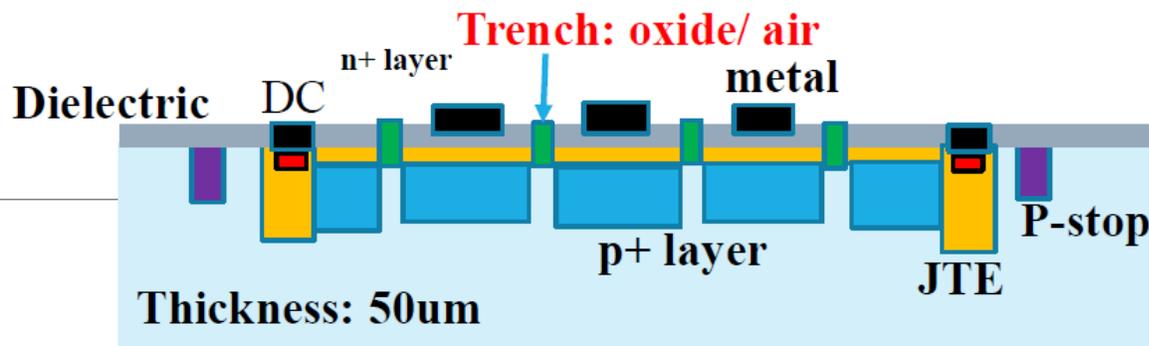➤ Depleted bulk capacitance and inter-strip capacitance significantly reduced for AC-LGAD with Si oxide and vacuum isolation structures.

Isolated AC-LGAD Simulation and Design

Trench depth

Trench: oxide/ air

n+ layer · metal · Dielectric · DC · p+ layer · JTE · P-stop

Thickness: 50um

Type 2&3

More details on Xu Huang's poster

Type 3, trench width as 1 µm

bulk capacitance

Type 3

Inter-strip capacitance

Type 3

➤ **Trench isolation depth be simulated and IV changes as changing the trench depth.**

Depleted bulk capacitance and inter-strip capacitance significantly reduced for AC-LGAD as the depth increasing.

■ Test Setup

➢ Test-pulse mode

- A 720-MHz clock (Si5347) for both serializer and TDC. Inside the TDC, the 720-MHz clock is divided down to 18 MHz and used as the reference clock for TOA measurement.

- A 2-MHz clock (Si5347) to trigger a pulse/pattern generator (81130A). Both the pulse width and relative delay of pulse signal are independently adjustable. This function enables scanning of TOT and TOA transfer curves;

- The measured standard deviation is 15.8 ps for the pulse width and 14.2 ps for the relative delay.

- The averaged and rounded TDC output code from repeated measurements are used to plot the transfer curve.

➢ FE-mode

- For functional verification of the FE-TDC integration, a passive RC differential circuit is used to generate an analog signal as input of FE.
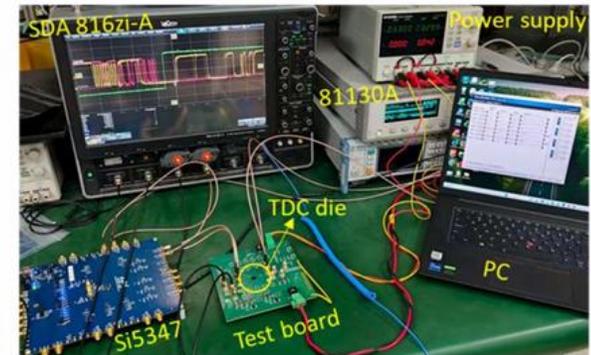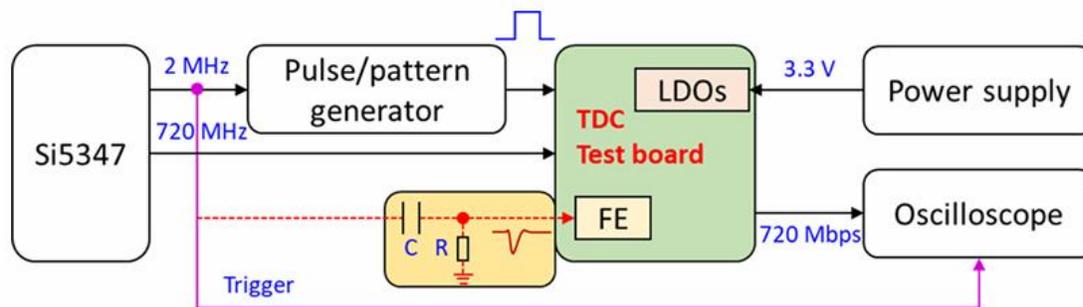

Fig 3. Test setup

Test Results

Timing performance (test-pulse mode)

- The TOA DNL and INL without FE are measured less than ± 1 LSB;
- $LSB_{toa} \approx 31.1$ ps;
- The TOT DNL and INL without FE are measured less than ± 1 LSB;
- $LSB_{tot} \approx 31.0$ ps ;

- $LSB_{cal} \approx 31.1$ ps ;
- These three LSB are very close, indicating the effectiveness of the self-calibration.
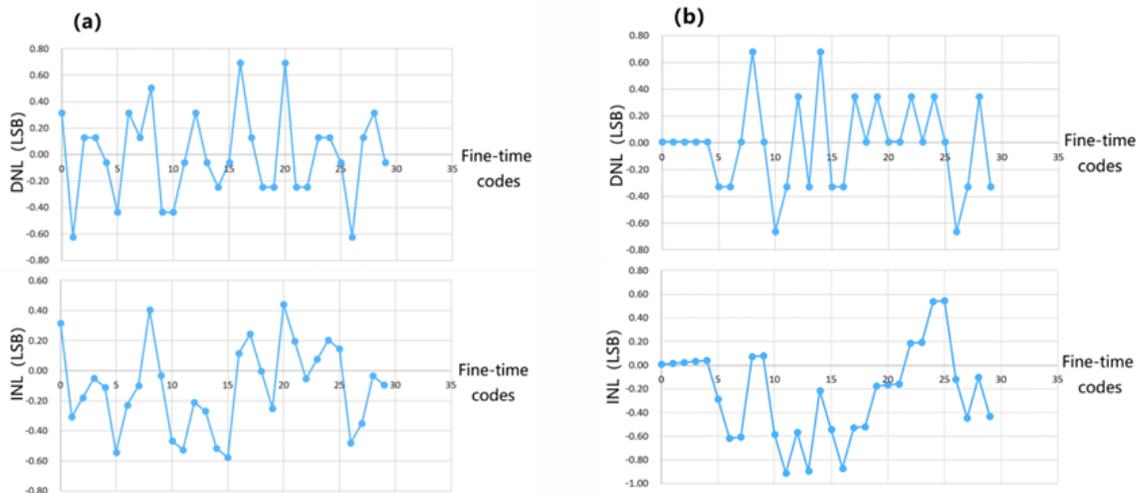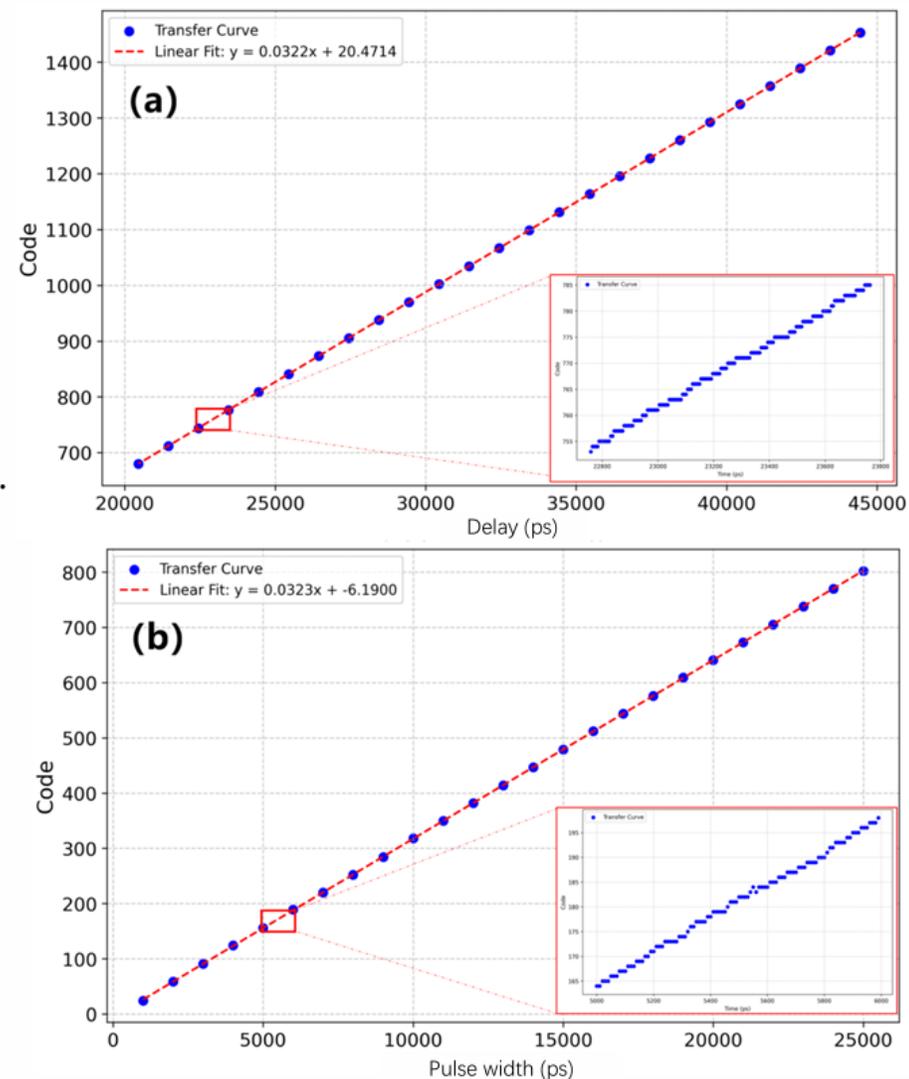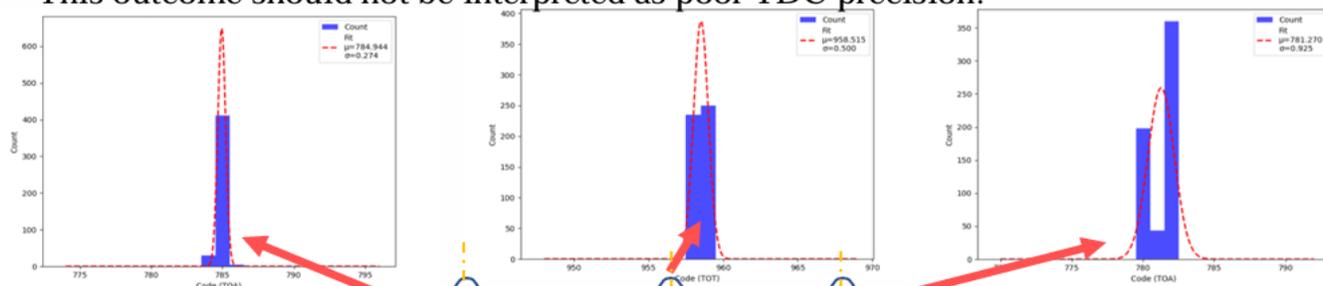

Fig 4. DNL & INL of: (a) TOA; (b) TOT

Fig 5. Measured transfer curves of: (a) TOA; (b) TOT

■ Timing performance (test-pulse mode)

➤ Figure 6 shows the distribution of the standard deviation of TOA from multiple measurements, *obtained without removing the influence of the signal source* ($\sigma =$ 14.2 ps, *The relative magnitude between σ and the code width significantly dictates the statistical results*).

➤ The standard deviation for the most of delay values is better than 0.5 LSB;

➤ The standard deviation of a few points is significantly greater than 0.5 LSB:
  - These points correspond to the regions with smaller code width in the transfer curve.
  - The jitter of the signal introduces a larger influence when the code width is smaller.
  - This outcome should not be interpreted as poor TDC precision.
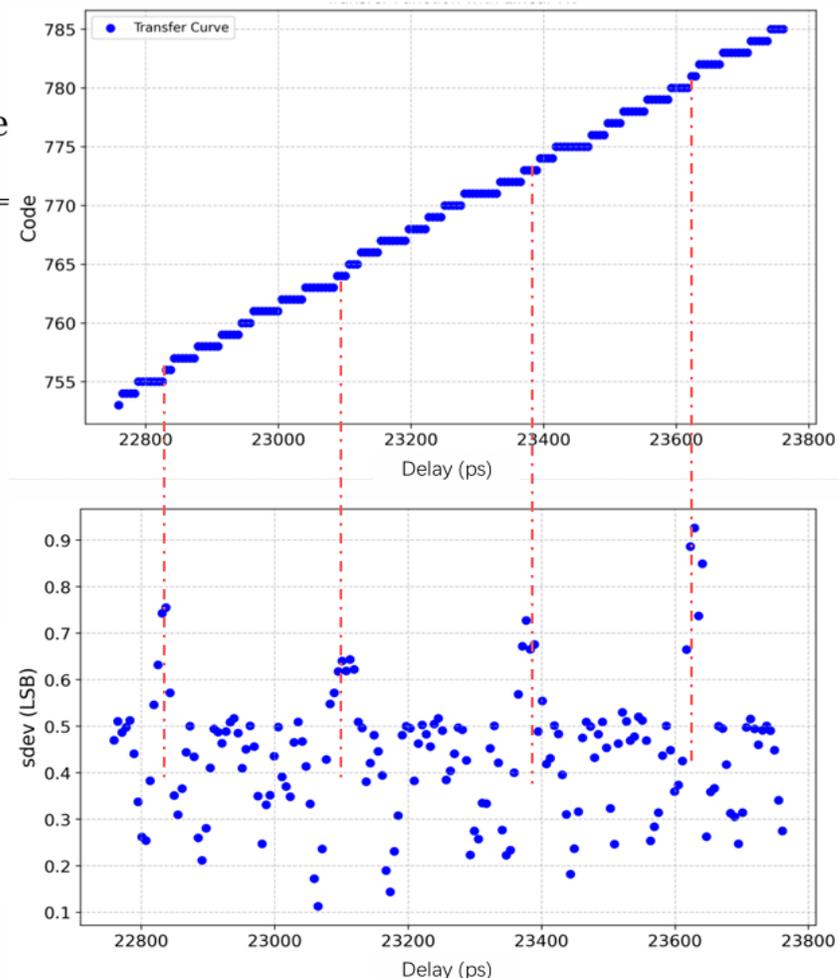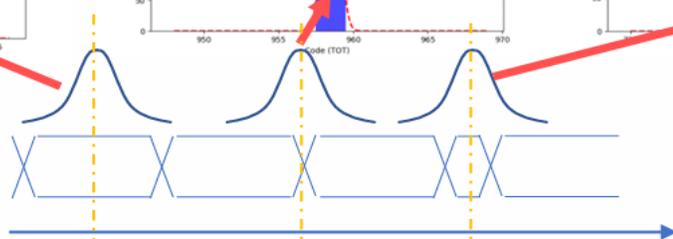
TOA_latch (distribution)

Code

Time

Fig.6 The standard deviation of repeated measurement corresponding to the transfer curve

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Test Results

■ Timing performance (FE-mode)

➢ To perform functional verification of the FE-TDC integration (Futher test with LGAD is ongoing).

➢ Figure 7 shows the FE-TOA and FE-TOT distributions for a 13.0 mV input signal.

➢ Preliminary results indicate standard deviations of less than 0.9 LSB and 1.1 LSB, respectively.

■ Power consumption

➢ The FE consumes 4.9 mA (1.2V).

➢ The power consumption of the TDC core varies with event rate.

➢ The total power consumption is measured to be 6.24 mW at an event rate of 1 MHz.

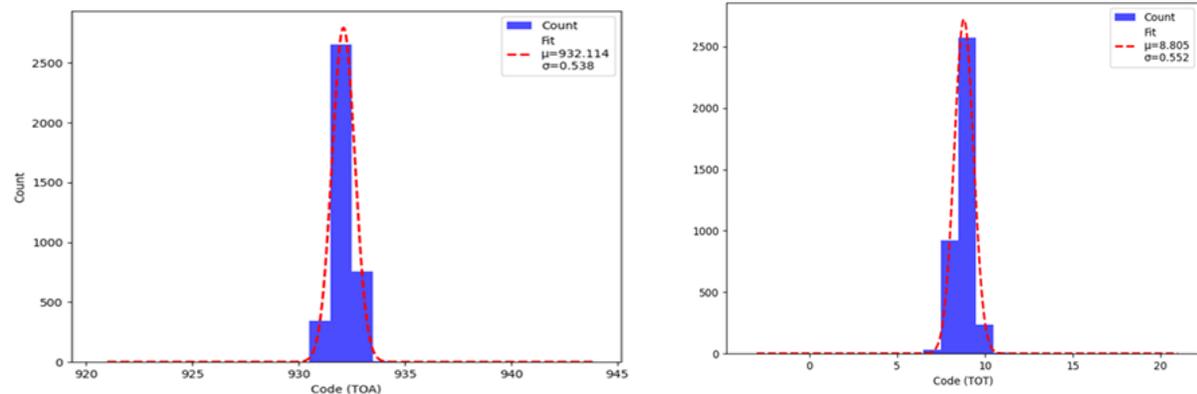| Blocks	Event rate	Operating current
TDC part	2 MHz	~ 0.5 mA
	1 MHz	~ 0.3 mA
	500 kHz	~ 0.1 mA
Pre-amplifier		~4.9 mA

Fig.7 The statistical standard deviation corresponding to the transfer curve

Xiongbo Yan's talk in CEPC Workshop 2025 @ Guang Zhou

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