Development and Validation of the iRPC Back-End Electronics Prototype for CMS Phase-2 Upgrade

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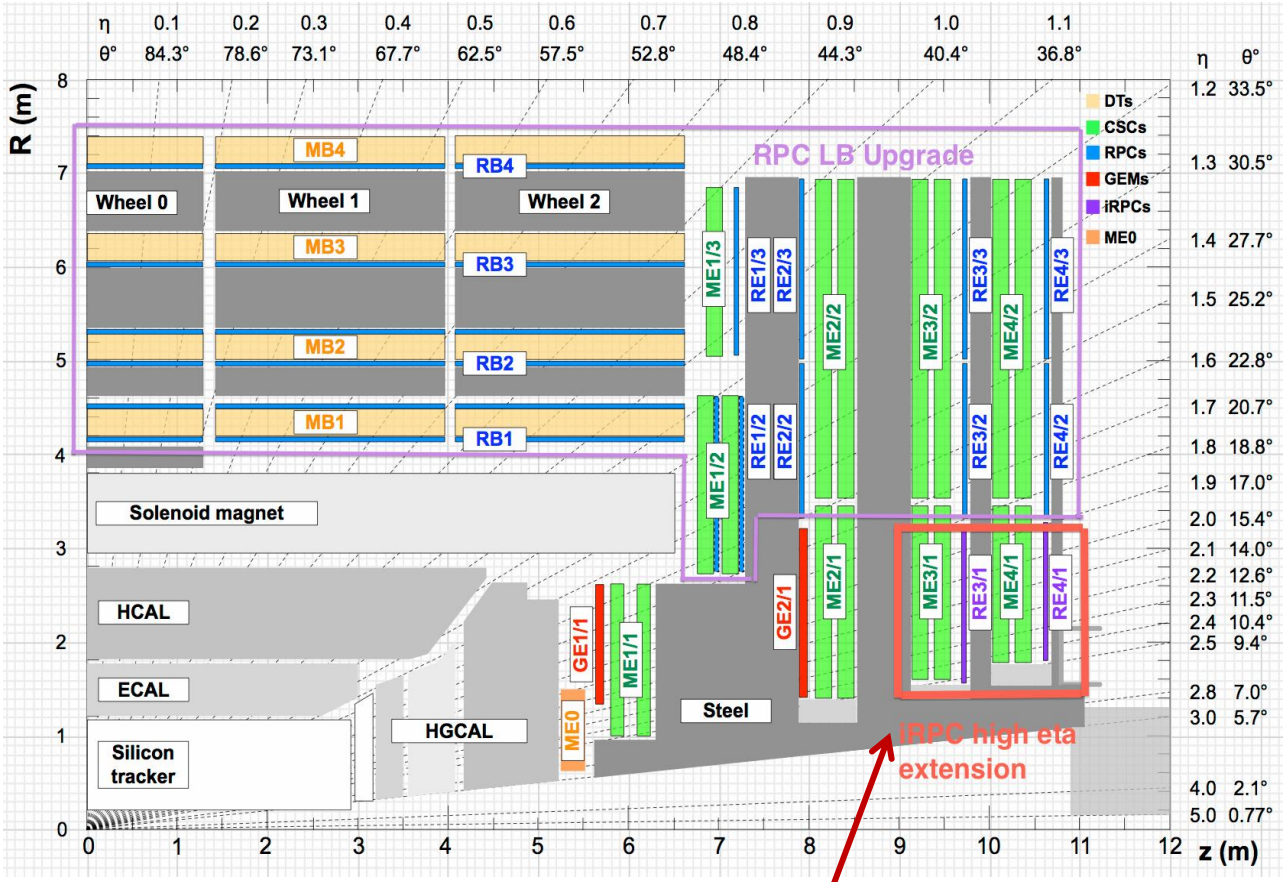
On behalf of CMS collaboration

Outline

- Background & Motivation
- μTCA (micro Telecom Computing Architecture) Prototype development
  - System Architecture
  - Firmware design
- μTCA Prototype Validation
  - Test in CERN 904 lab & CERN GIF++ lab
  - Full-Chain Integration at CERN CMS experiment
- Summary

Background & Motivation

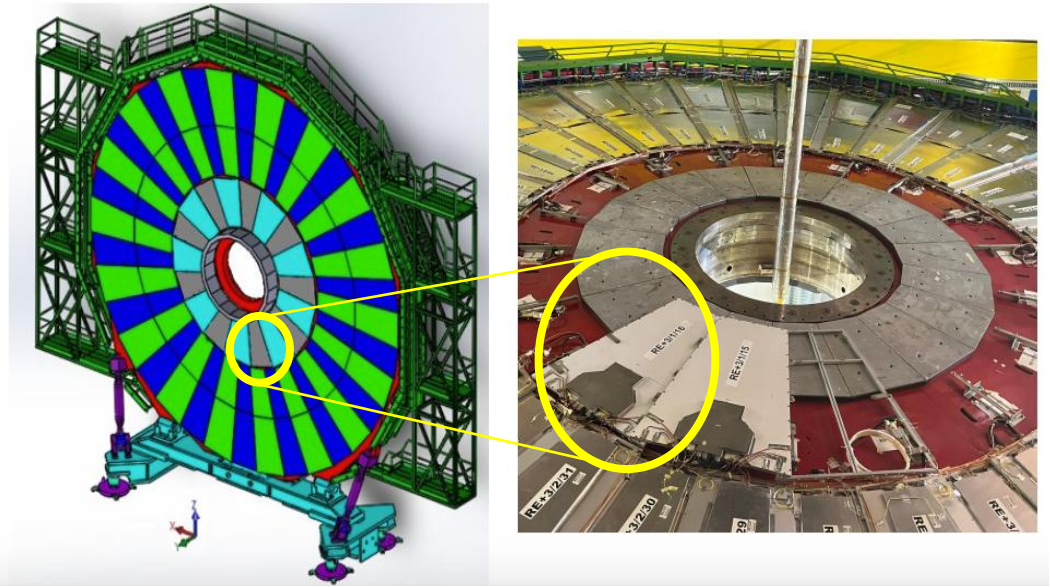


The iRPC installation location

Extend the RPC pseudorapidity coverage up to 2.4 to increase redundancy in high eta region in stations 3 and 4

RE 3/1 and RE 4/1 Improved RPC

- **Motivation:** iRPC (improved resistive plate chamber) is a key component of the CMS Phase-2 Upgrade
  - Increase rate capability (2 kHz/cm²).[1]
  - Time resolution for background rejection (1.5 ns).[1]
  - Spatial resolution in r direction (2 cm).[1]
  - Improved contribution of RPCs to muon triggering in the forward region.

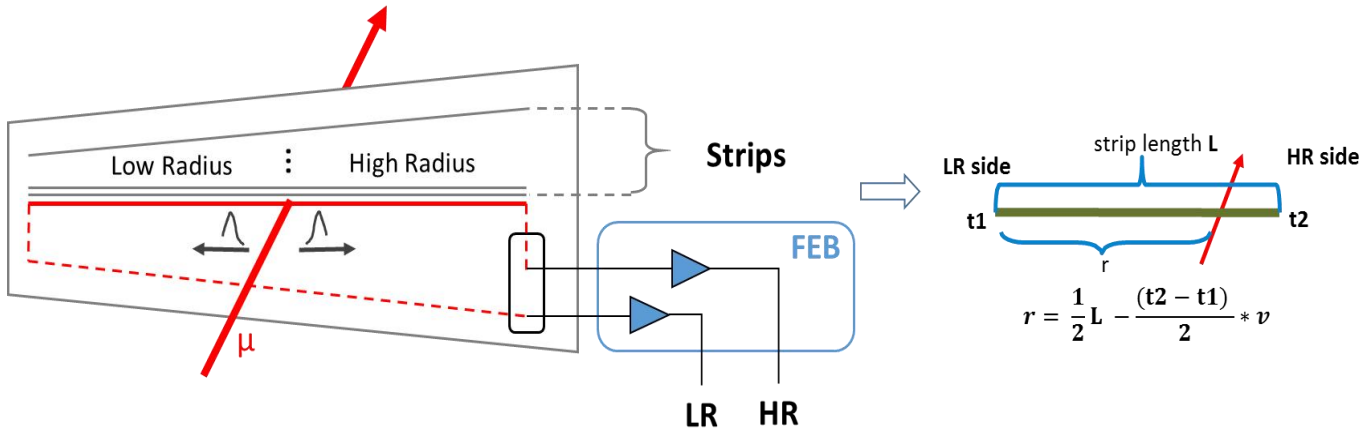


The iRPC detector installed at CERN CMS experiment

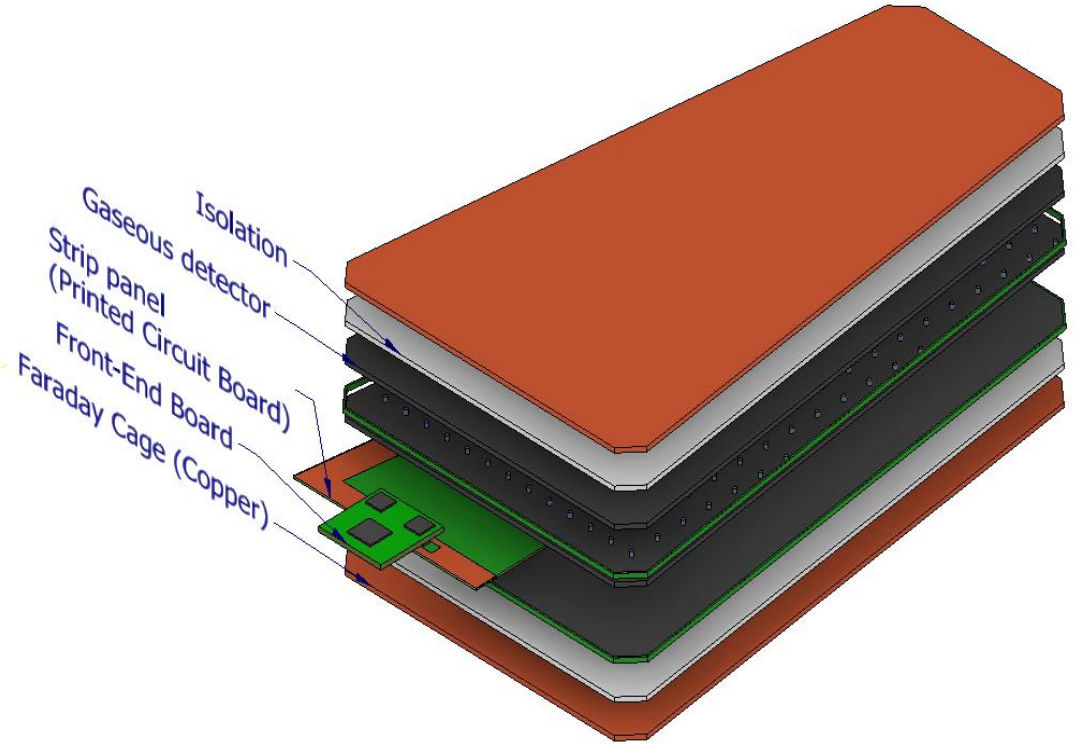
[1] CMS Collaboration, The Phase-2 Upgrade of the CMS Muon Detectors, CERN-LHCC-2017-012, CMS-TDR-016 (2017).

Background & Motivation

- **Consideration:** As the final Advanced Telecommunications Computing Architecture (ATCA)-based backend hardware was still progressing , a μTCA-based prototype was adopted to help meet the CERN CMS experiment data-taking goal
- **Solution & Value:** A prototype back-end electronics system was therefore developed and validated through the full data chain — an essential step for both iRPC detector development and the future ATCA-based system.



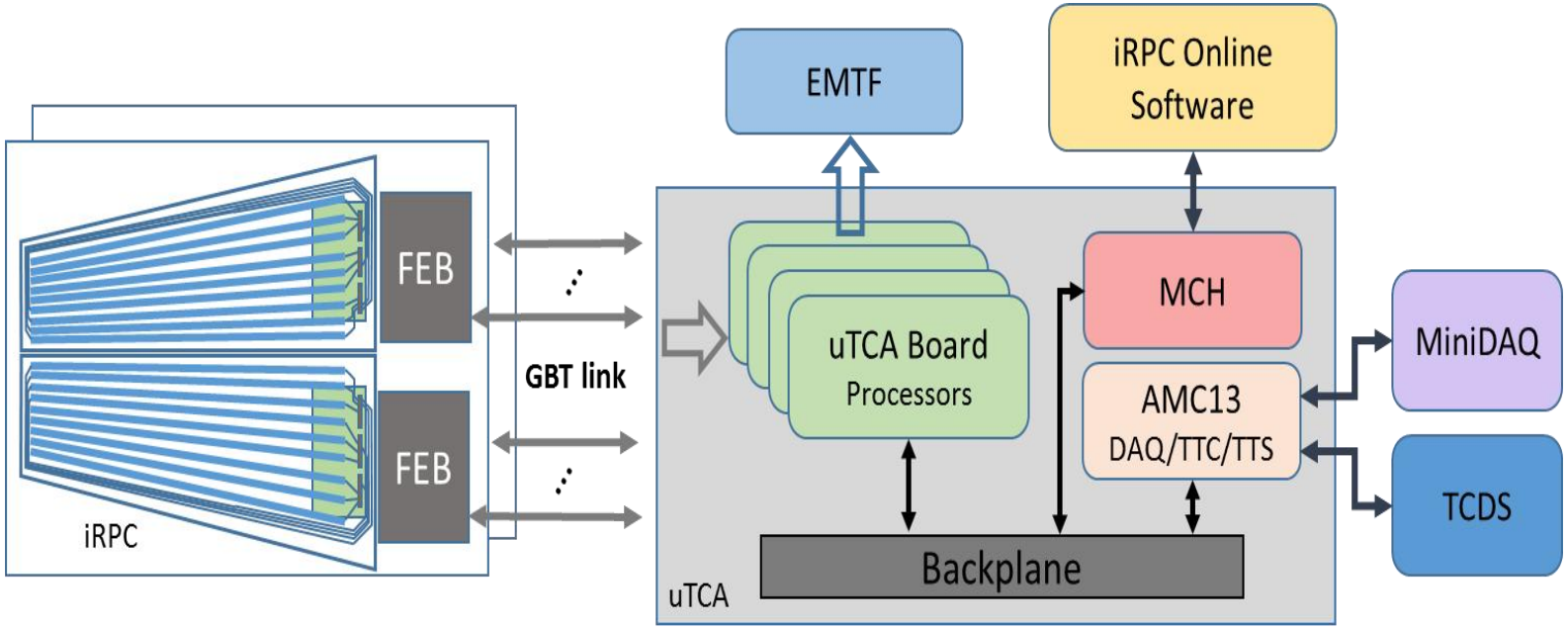
- **Electronics:**
  - **Two ends readout.** 48 strips/96 channels per half chamber
  - New frontend electronics. Providing Time-to-Digital Converter (TDC) data with a LSB (Least Significant Bit) around 10ps.
  - New backend electronics.



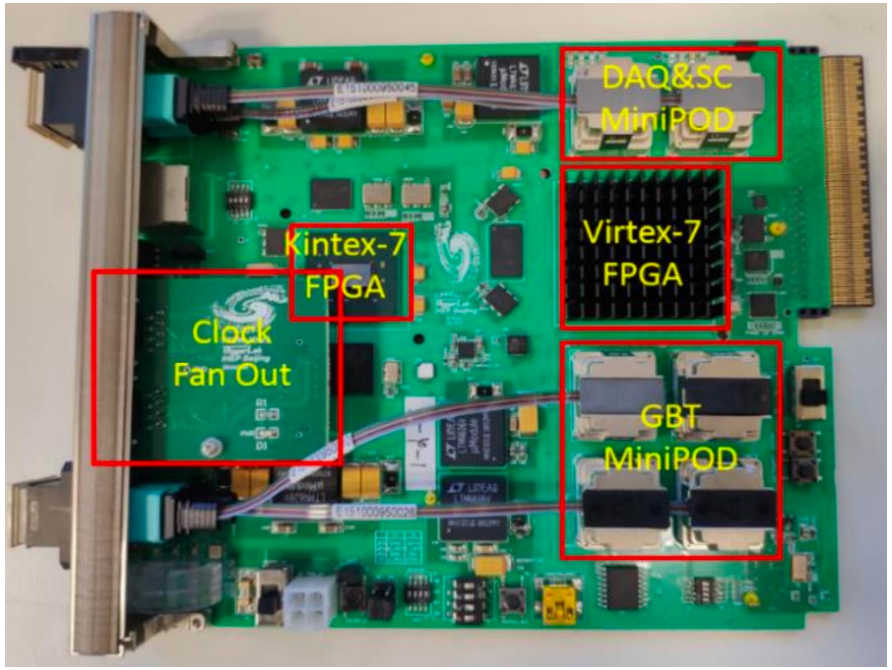
μTCA Prototype System Architecture

System-level architecture of the iRPC back-end prototype

- GBT (GigaBit Transceiver) links——Receiving Detector data from the iRPC FEB (Front-End Board).
- TTC (Timing, Trigger and Control) Links——Receiving timing and trigger signals from LHC CMS.
- EMTF (Endcap Muon Track Finder) Link——Sending cluster infromation from iRPC for Level-1 muon trigger.
- DAQ (Data Acquisition) for data readout; Online software for control and monitoring
- A back-end electronics board (BEB) was designed in-house to meet the needs of the iRPC back-end system.



System Architecture

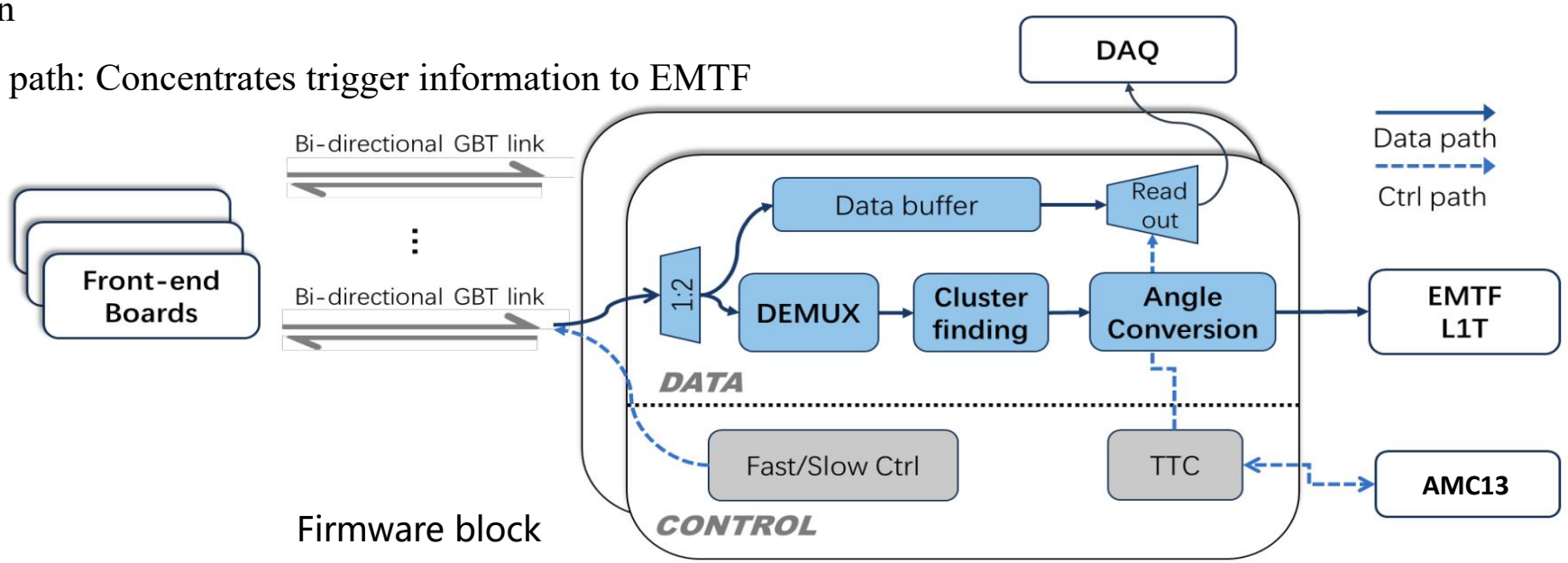


iRPC μTCA BEB

Firmware Function Overview

Firmware Functional Blocks

- Front-end to Back-end Data Link:
  - ➢ GBT protocol: Hit and control information
- Trigger Pre-processing:
  - ➢DeMux (Demultiplexer)： Ordered Processing of Disordered Detector Data
  - ➢Cluster Finding Algorithm: Muon Hit Detection and Cluster Info Extraction
  - ➢Trigger path: Concentrates trigger information to EMTF
- Data Acquisition:
  - ➢Synchronized Readout of Detector and Cluster Data
  - ➢Latency Calibration, Multi-link Integration, and BUSY Handling Mechanism
  - ➢Commercial 10G Ethernet Protocol
- Fast/Slow control
  - ➢Routes Backend, GBT, and Frontend control commands from the online control system

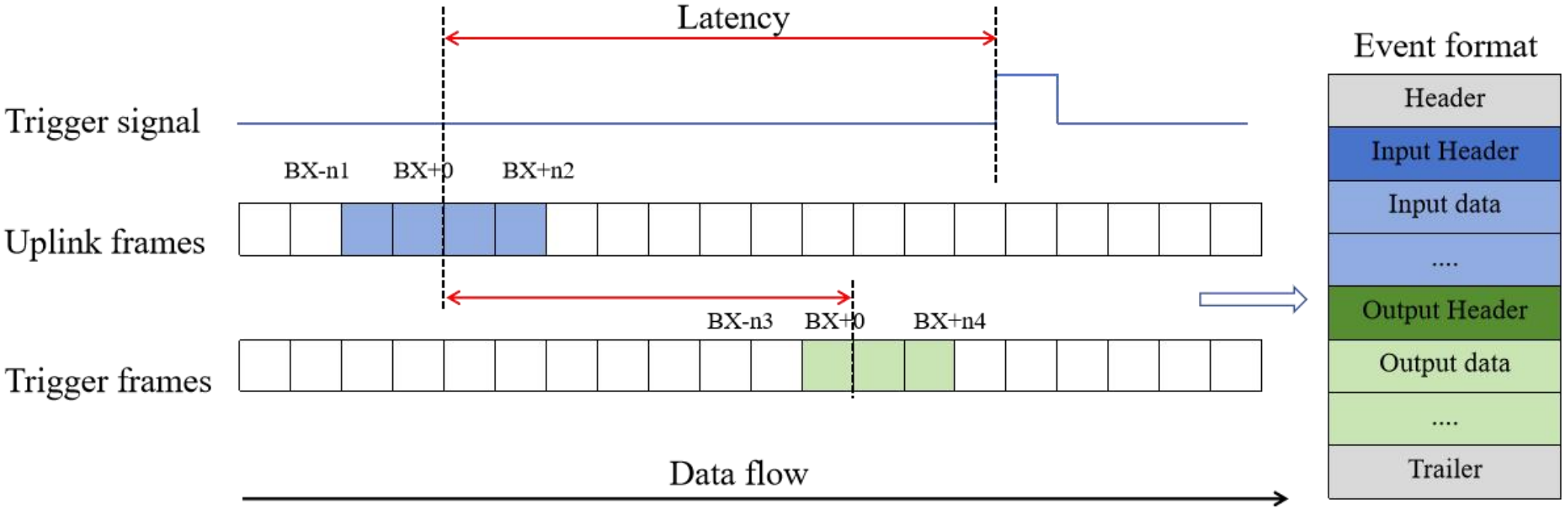


Firmware block

Firmware Function Overview

Trigger-Based Readout Principle

- Continuous pipelined buffering: uplink frames written to RAM (Random Access Memory) every BX (bunch crossing), regardless of trigger arrival
- Fixed latency → address offset: trigger-to-data latency is constant, so it directly maps to a RAM read offset
- Data readout: when a trigger arrives, the firmware computes a window extending both before (-BX) and after (+BX) the trigger position, reads the RAM across that range, and sends the data to the next packing stage.

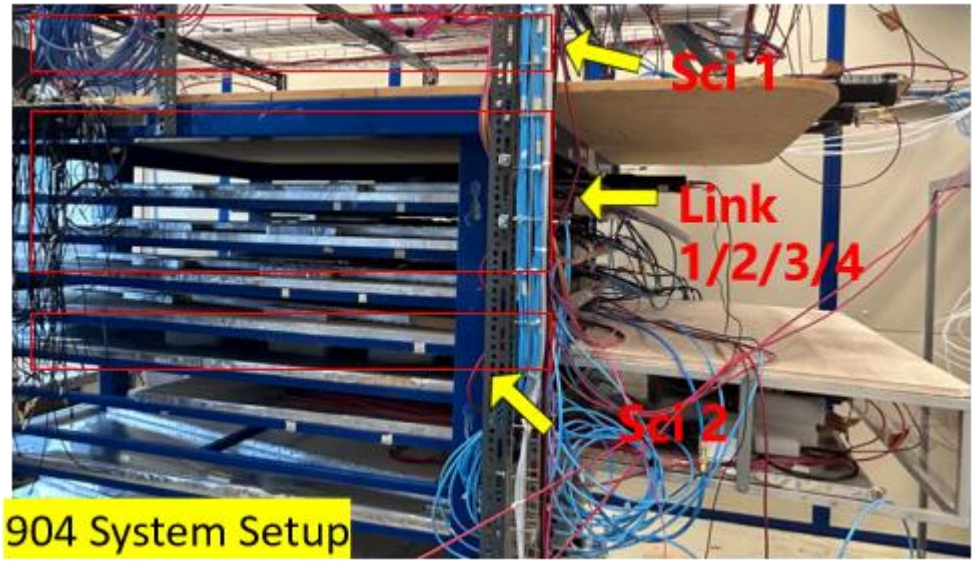


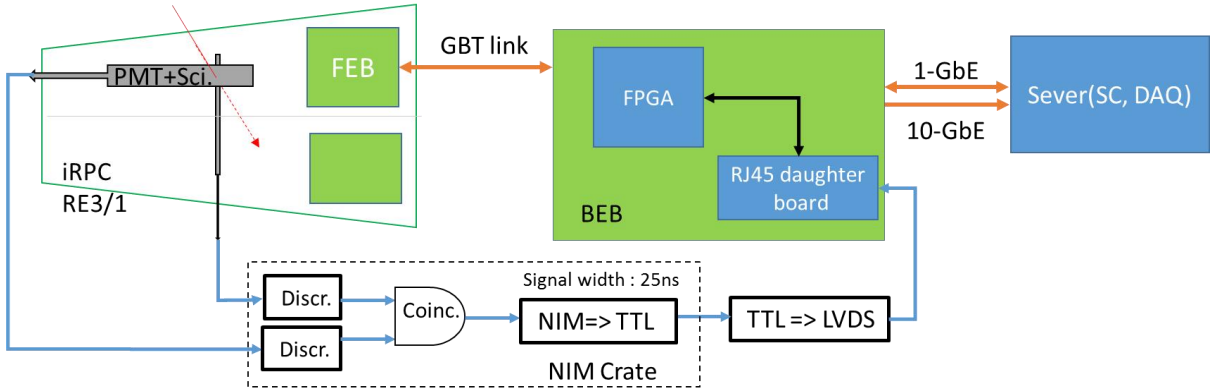
Schematic of the Trigger-Based Readout Principle

Test in CERN 904 lab & CERN GIF++ lab

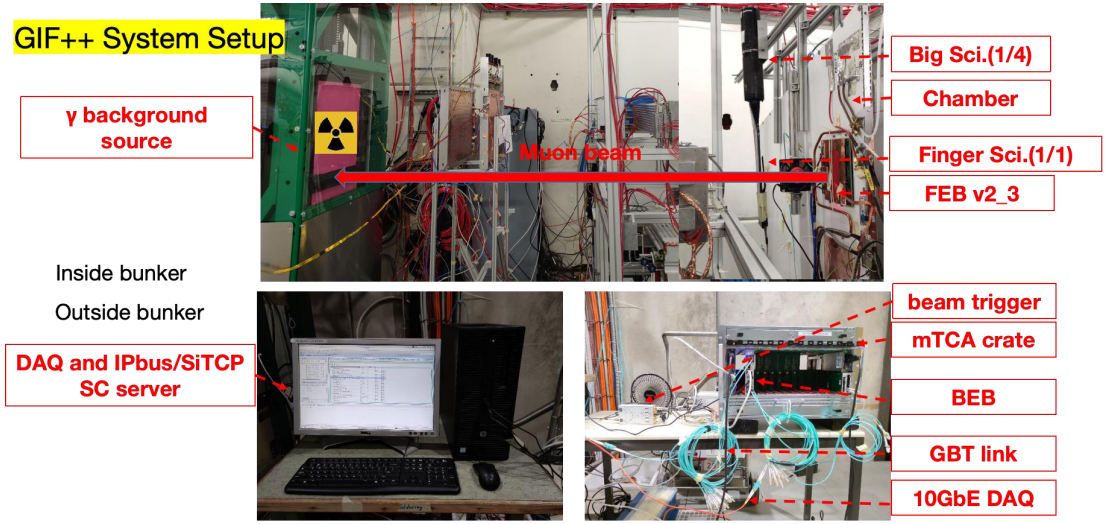
iRPC μTCA backend has joint test with iRPC chamber and FEB in 904 for cosmic data taking and in Gif++ for muon beam data taking.

- FEB channel timing alignment
- FEB calibration
- Timing reference (Bunch crossing 0) distribution correction
- FEE (Front-End Electronics) data sending window study
- Check-Sort-Push data sending



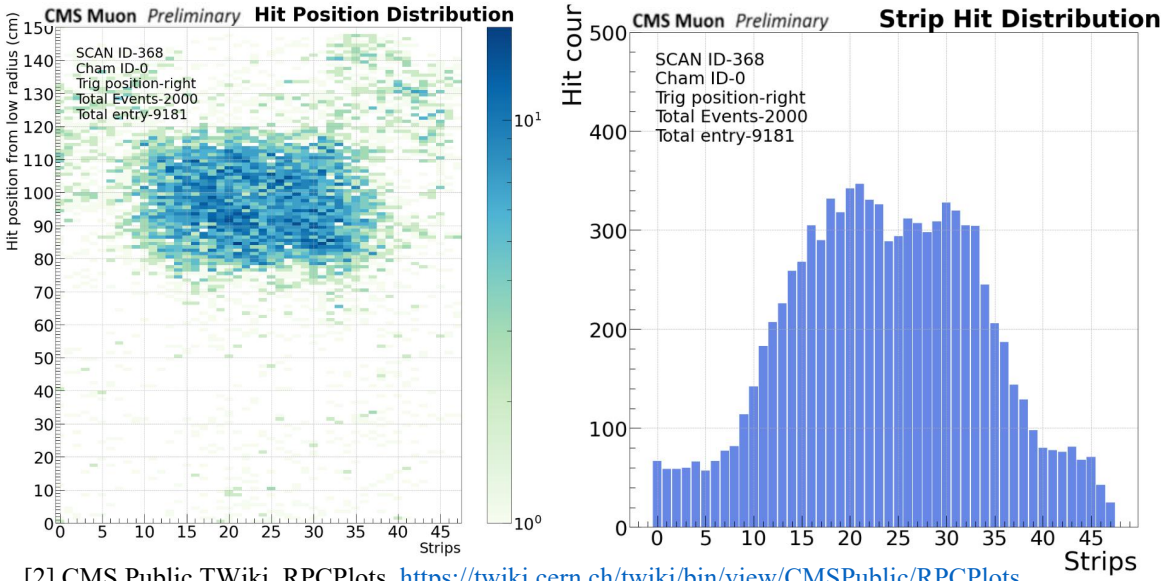


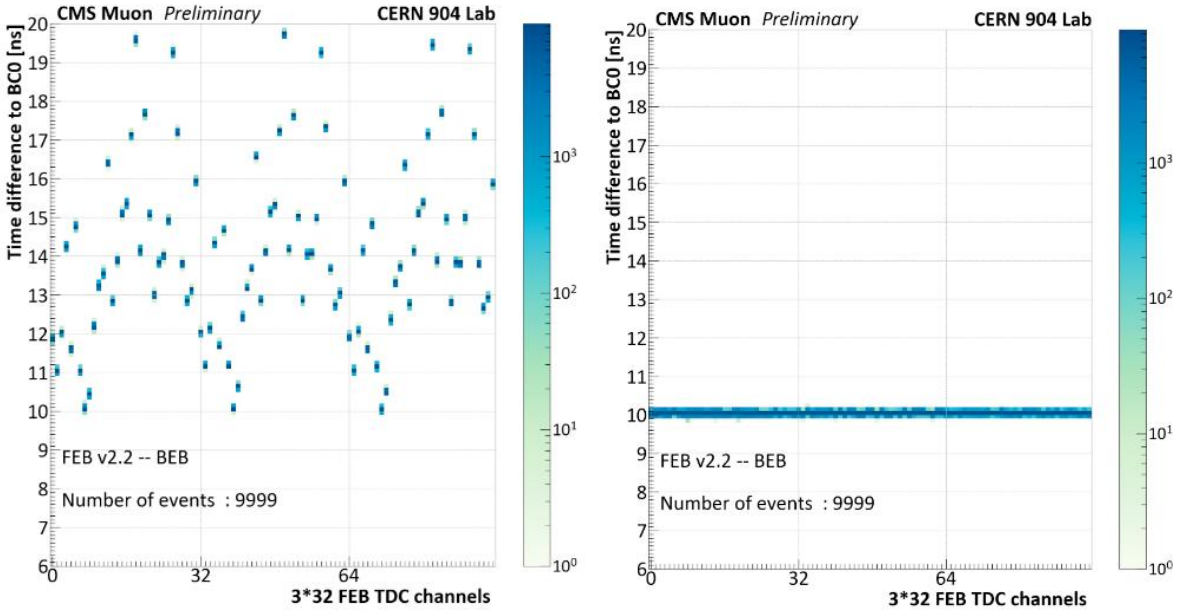
Schematic diagram of the test system



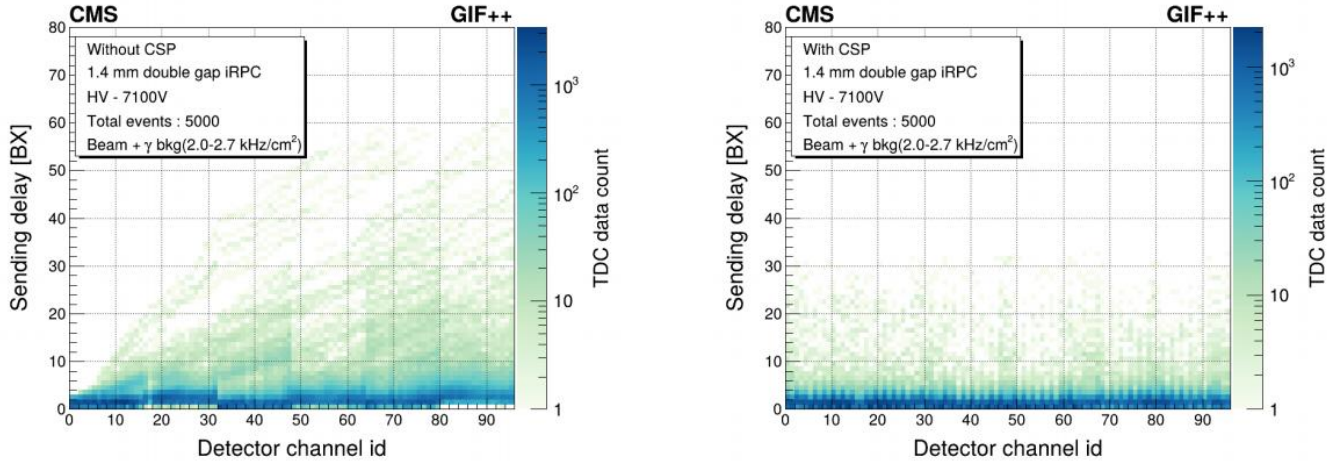
Test in CERN 904 lab & CERN GIF++ lab

These tests confirmed correct back-end operation under local clock/trigger conditions with both cosmic rays and beam, laying the foundation for subsequent LHC-synchronized validation at CMS experiment.





Timestamp distributions before and after TDC alignment [2]



Sending delay distribution without (left) and with (right) CSP (Check-Sort-Push) [3]

[2] CMS Public TWiki, RPCPlots, https://twiki.cern.ch/twiki/bin/view/CMSPublic/RPCPlots

[3] Z.-A. Liu et al., *Application of the new Check-Sort-Push mechanism in the iRPC subsystem for the CMS Phase-2 upgrade*, 2026 JINST 21 P01021, https://doi.org/10.1088/1748-0221/21/01/P01021

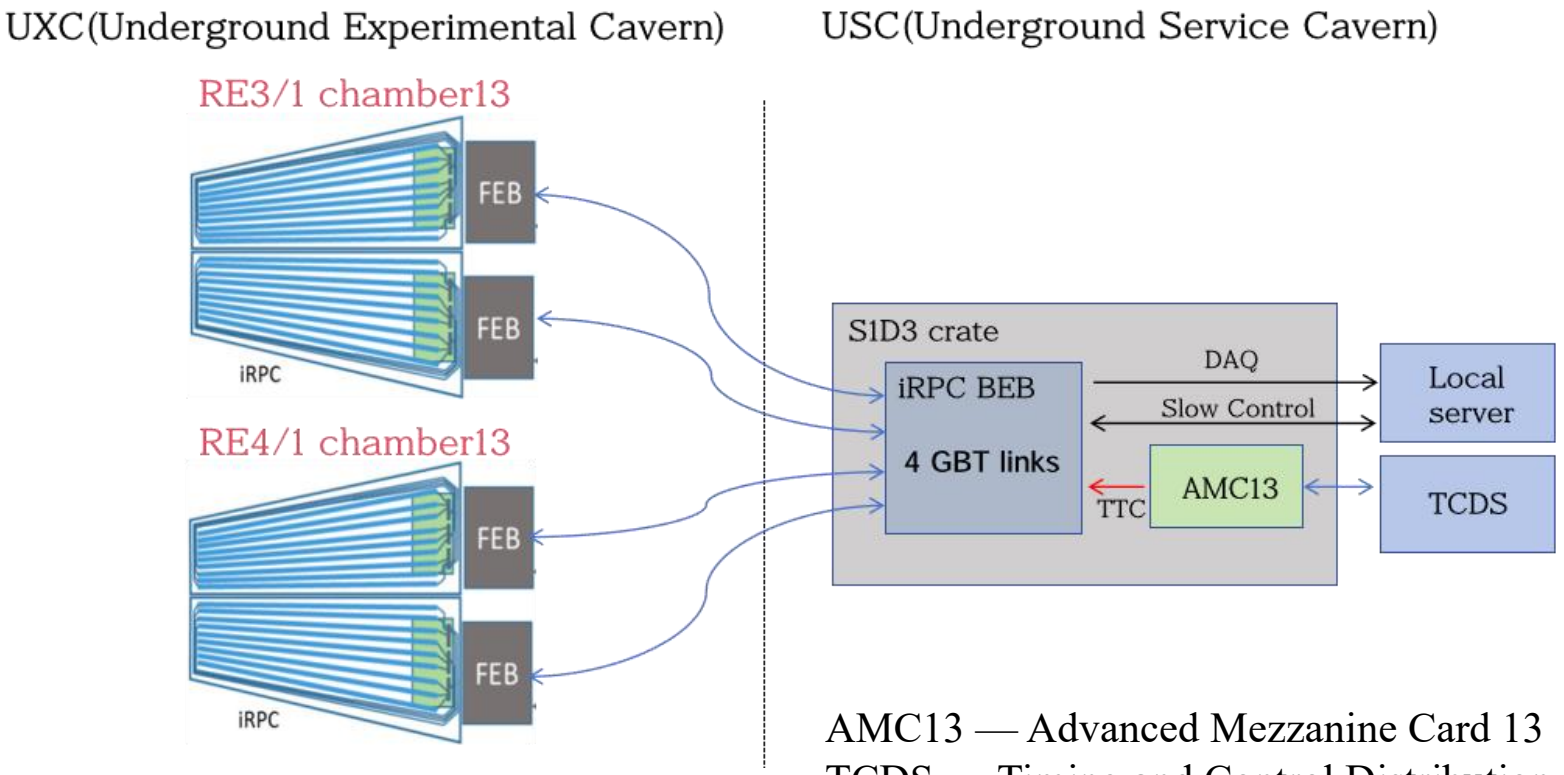
Full-Chain Integration at CMS experiment

Prototype data-taking at CMS experiment is essential to validate iRPC performance under real LHC collisions ahead of LS3 (Long shutdown).

- **Task 1 — Timing, Trigger and Control (TTC) Integration**
  - Integrate the LHC-synchronized clock, BC0 (Bunch crossing 0) signal, and Global Trigger into the back-end electronics via AMC13
- **Task 2 — Multi-Trigger Validation**
  - Validate self-trigger mode to confirm correct operation and algorithm behavior.
  - Take data with the CMS global Trigger to confirm the back-end electronics is correctly aligned and operating with the LHC system
- **Task 3 — Joint Test with EMTF (**Endcap Muon Track Finder)
  - Perform joint testing with EMTF to confirm reception of iRPC cluster data at the EMTF side, validating the iRPC trigger path within the L1 muon trigger.

Full-Chain Integration at CMS experiment

- Prototype data-taking at CMS experiment is essential to validate iRPC performance under real LHC collisions ahead of LS3.
- We used one BEB with four GBT links, connecting chamber at RE3/1 and chamber at RE4/1.
- **Data was obtained at CMS experiment during LHC heavy-ion stable beams, at an effective High Voltage of 7.13 kV, corresponding to the working point.**



AMC13 — Advanced Mezzanine Card 13
TCDS — Timing and Control Distribution System

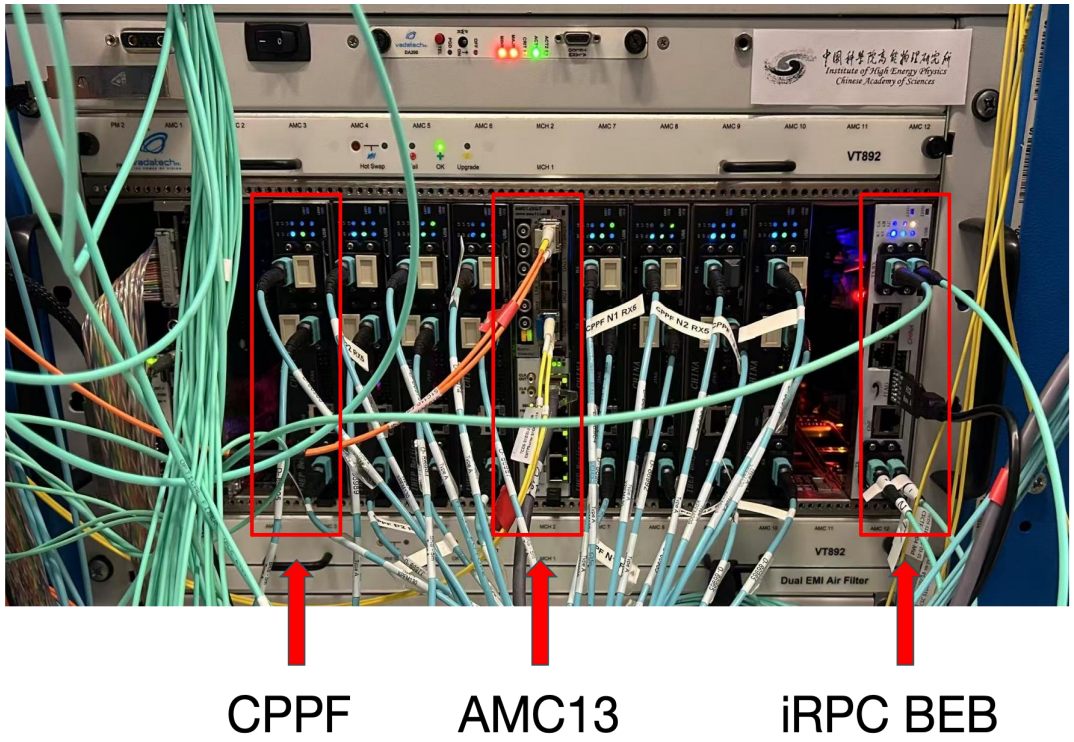
- We applied the previously developed Timing reference distribution correction method to correct the delay differences caused by fiber length.

More details for Timing reference distribution correctionin RPC2022 report: CMS iRPC Backend and Front-End Electronics joint test_RPC2022

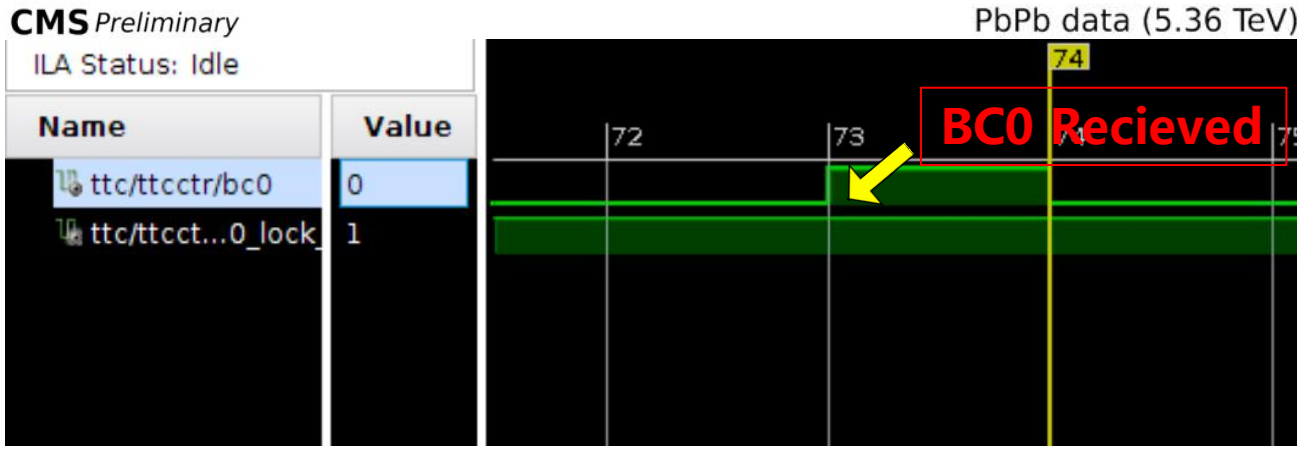
Full-Chain Integration at CMS experiment

Task 1 — Timing, Trigger and Control (TTC) Integration

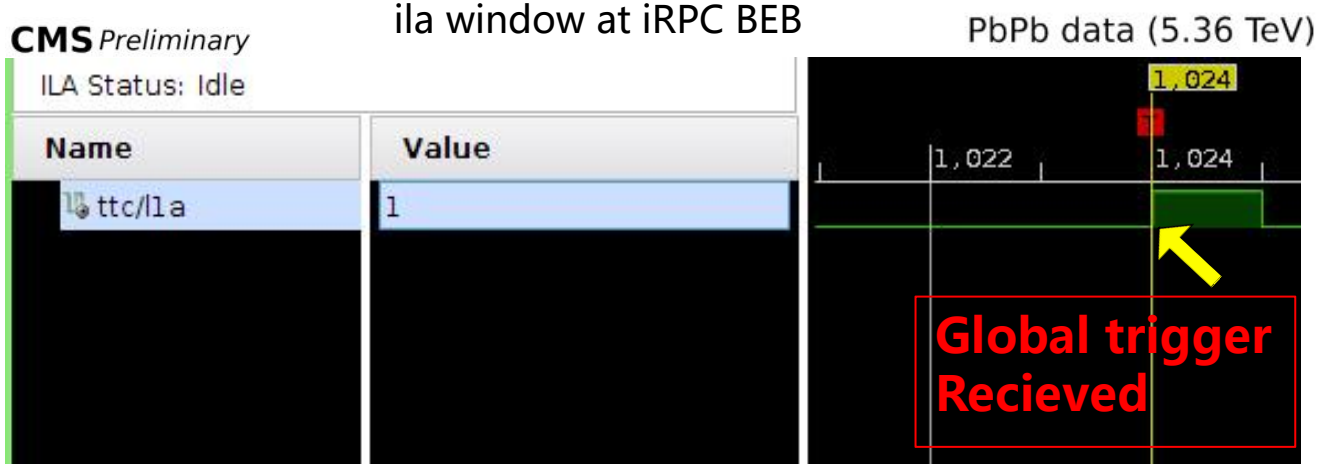
- The iRPC BEB was installed in the RPC Phase-1 Back-end crate in rack S1D3, occupying an available slot in the crate.
- Using the AMC13 already present in this crate, integration tests were performed, successfully decoding the BC0 signal, Global trigger, and LHC clock signal in firmware.



iRPC system at CMS experiment

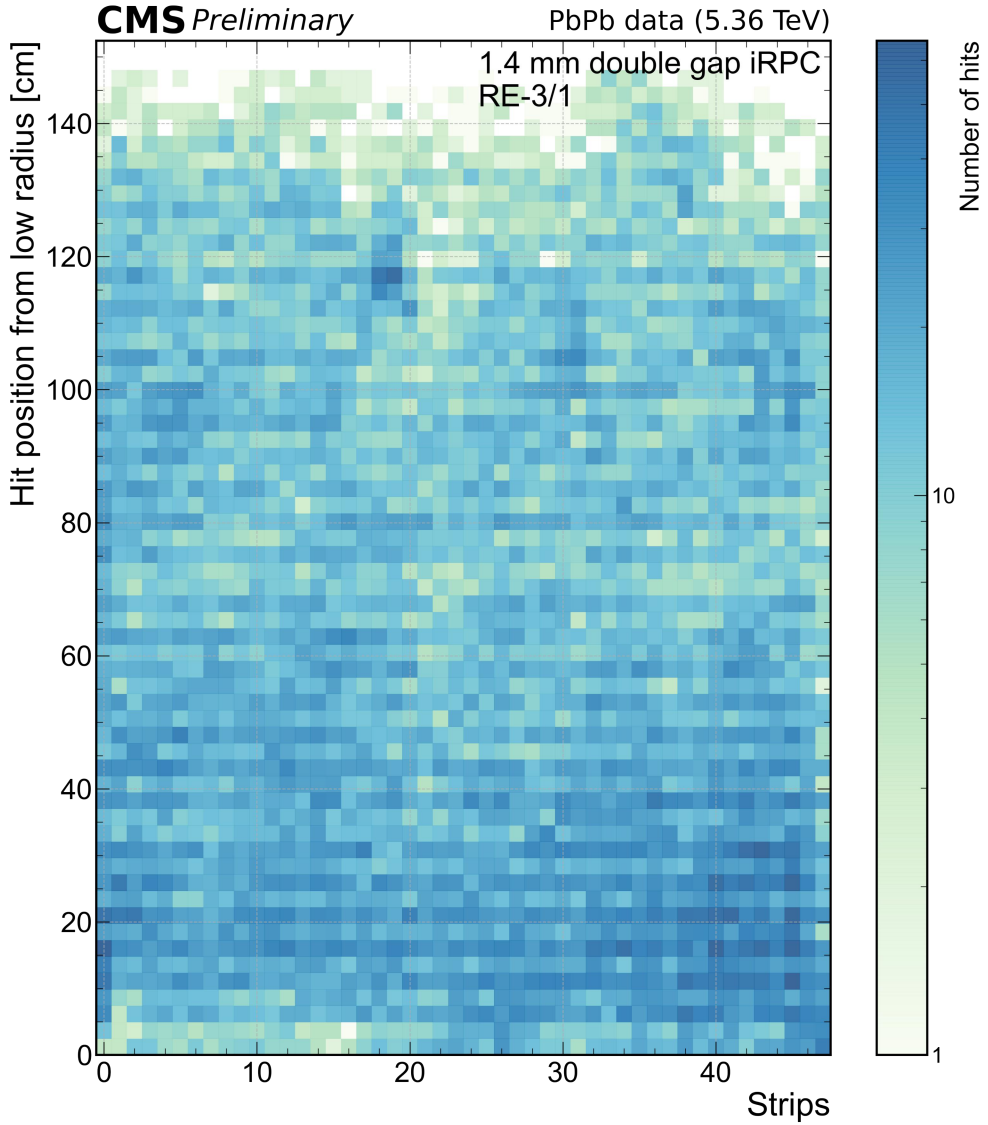


ila window at iRPC BEB



Full-Chain Integration at CMS experiment

Task 2 — Multi-Trigger Validation： Self-trigger



> The plot shows a 3D position of reconstructed hits at CMS experiment, at a working point of HV 7.13 kV was taken during LHC heavy-ion stable beams, using self-trigger mode, where the back-end algorithm generates a trigger upon detecting a valid cluster flag. The hit position accounts for the time difference between both ends of the readout strip:

$r = L/2 - v(t2 - t1)/2$, where L is the strip length, $t2 - t1$ is the arrival time difference between the low- and high-radius ends, and v is the signal propagation speed (~0.6c).

"Low radius" and "high radius" refer to the two ends of a readout strip along the radial direction, with "low radius" being the end closer to the beam axis and "high radius" the end farther away.

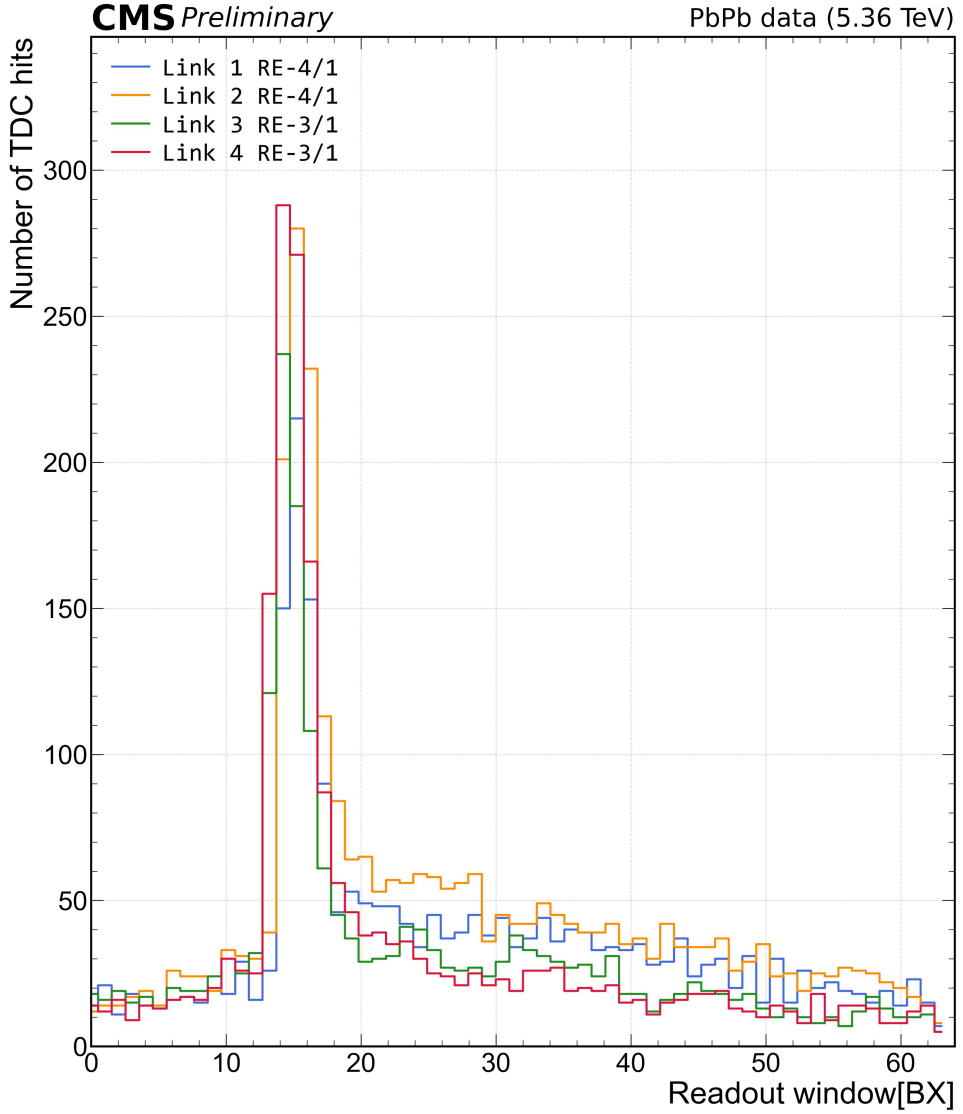
Number of events: 30000

Number of TDC hits (double ends TDC data):44613

Successful self-trigger data-taking was achieved under CMS beam conditions, providing a basis for further validation of back-end algorithm correctness

Full-Chain Integration at CMS experiment

Task 2 — Multi-Trigger Validation： Global-trigger



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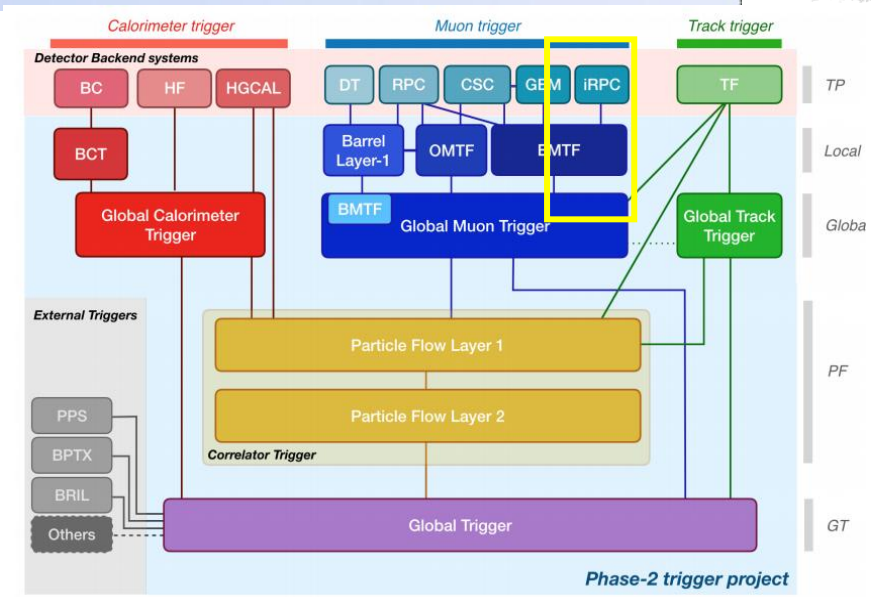
A clear data peak confirms correct delay alignment between the iRPC detector data and the CMS Global Trigger, while the tail of the peak arises from transmission delay.

Backend system was successfully integrated with the Global Trigger. By estimating the Global trigger latency and adjusting the back-end's delay values accordingly, a clear data peak was observed within the readout window

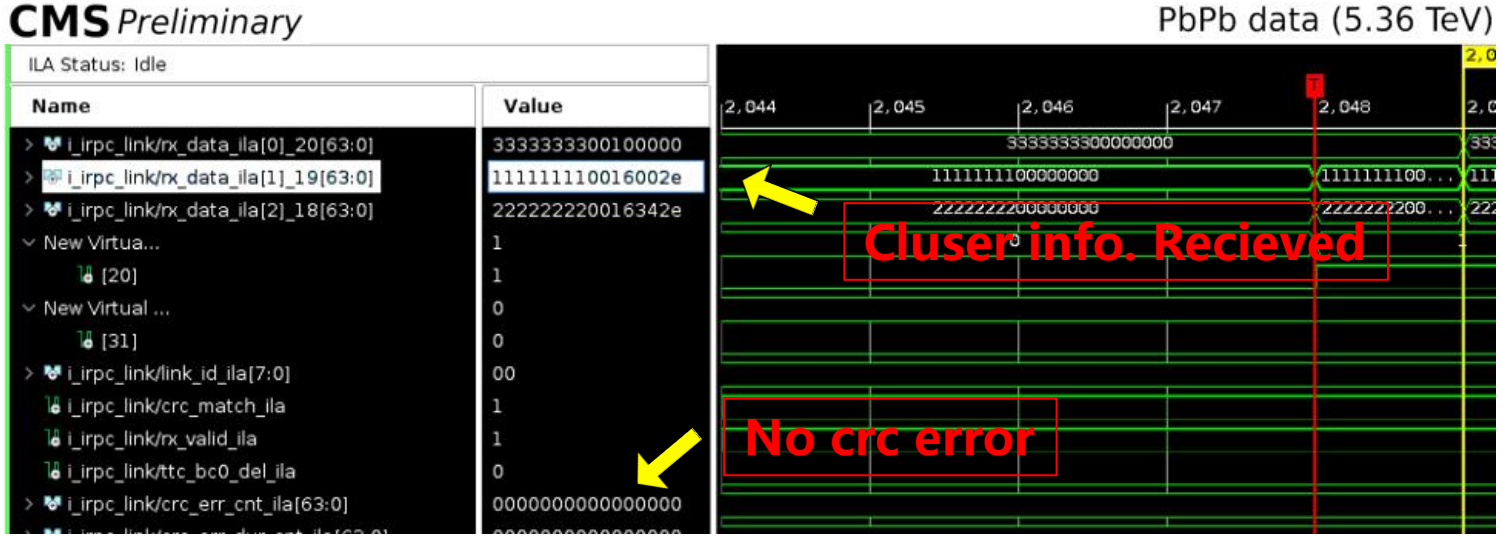
Full-Chain Integration at CMS experiment

Task 3 — Joint Test with EMTF

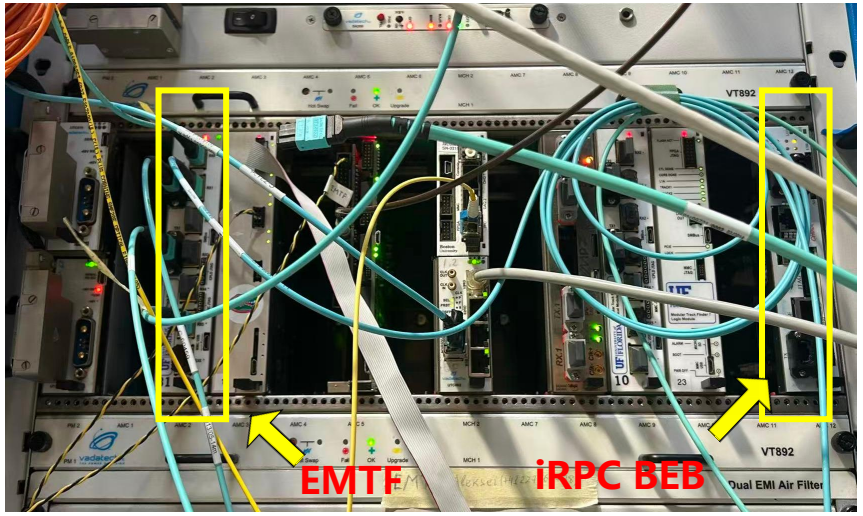
- In Phase-2, the iRPC will transmit endcap cluster information to the EMTF board, participating in the Level-1 trigger
- Preliminary tests at CERN 904 and CMS experiment indicated stable link performance and largely expected data format between the iRPC BEE and EMTF.
- These efforts made some progress ahead of LS3 and are expected to provide useful input for the subsequent Phase-2 development.



Architecture of the CMS Phase-2 Upgrade muon trigger system



Data receive window from EMTF side



Fiber connection between iRPC&EMTF

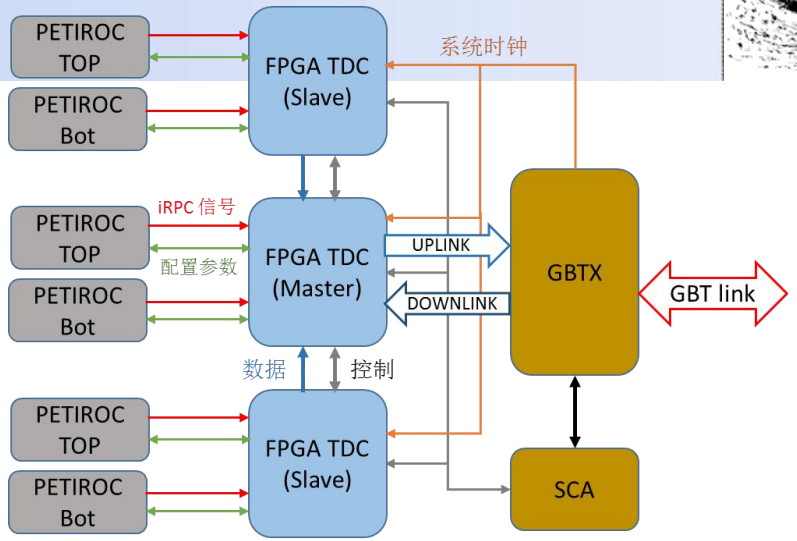
Summary

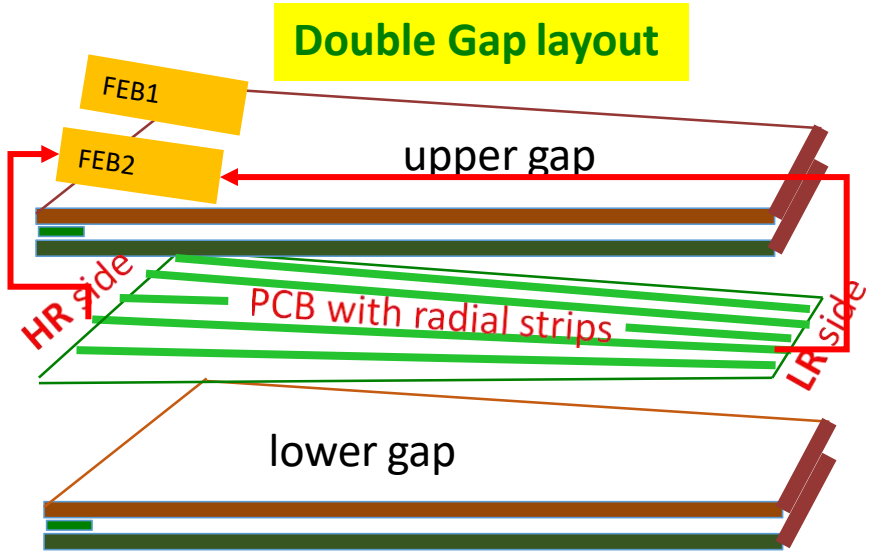
- A μTCA-based prototype was adopted to help meet the CMS experiment data-taking window ahead of LS3.
- The prototype features a complete system architecture and firmware, validated through testing at CERN 904 and CERN GIF++.
- Ahead of LS3, the prototype was successfully synchronized with the LHC system and achieved stable data-taking at CMS experiment, demonstrating the viability of the iRPC Phase-2 design.
- Current test results show that the iRPC backend electronics prototype satisfies design requirements and works as expected. More detailed data analysis is ongoing, and development of the new ATCA-based system is now underway.

- Supplemental materials

System Architecture

- **Frontend:**
  - GBTx : GBT frame
  - GBT SCA : Slow control
  - PETIROC : Digitize signal and produce trigger to FPGA
  - FPGA : Timestamp
- **Backend:**
  - GBT links
  - Trigger pre-process : Demux、Cluster finding and Angle conversion
  - DAQ : Delay calibration、multi-link integration、Busy mechanism
  - Fast/Slow control : BC0、backend slow control



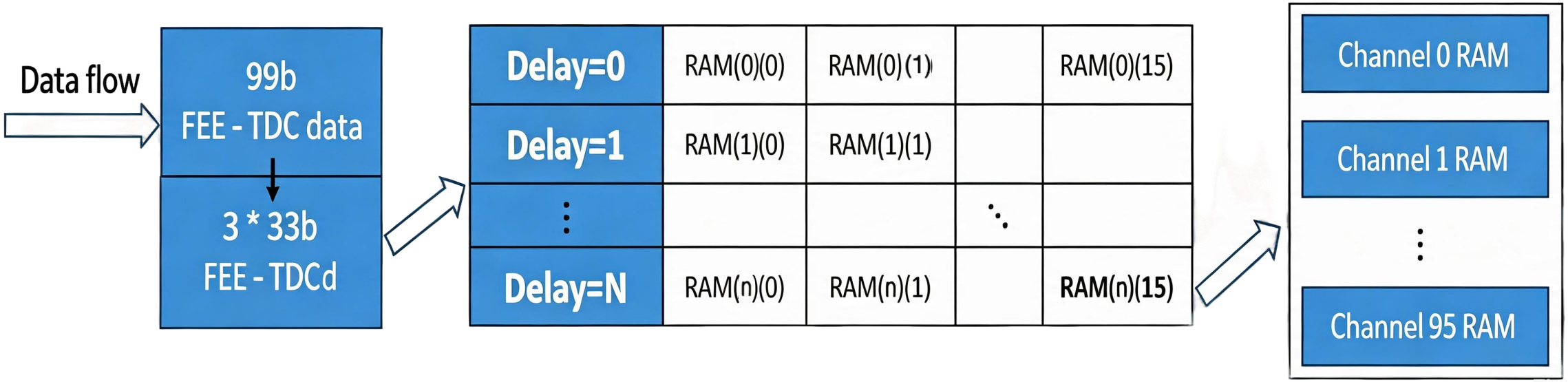


Dimensions: 165 cm x (63-114) cm

Firmware Function Overview

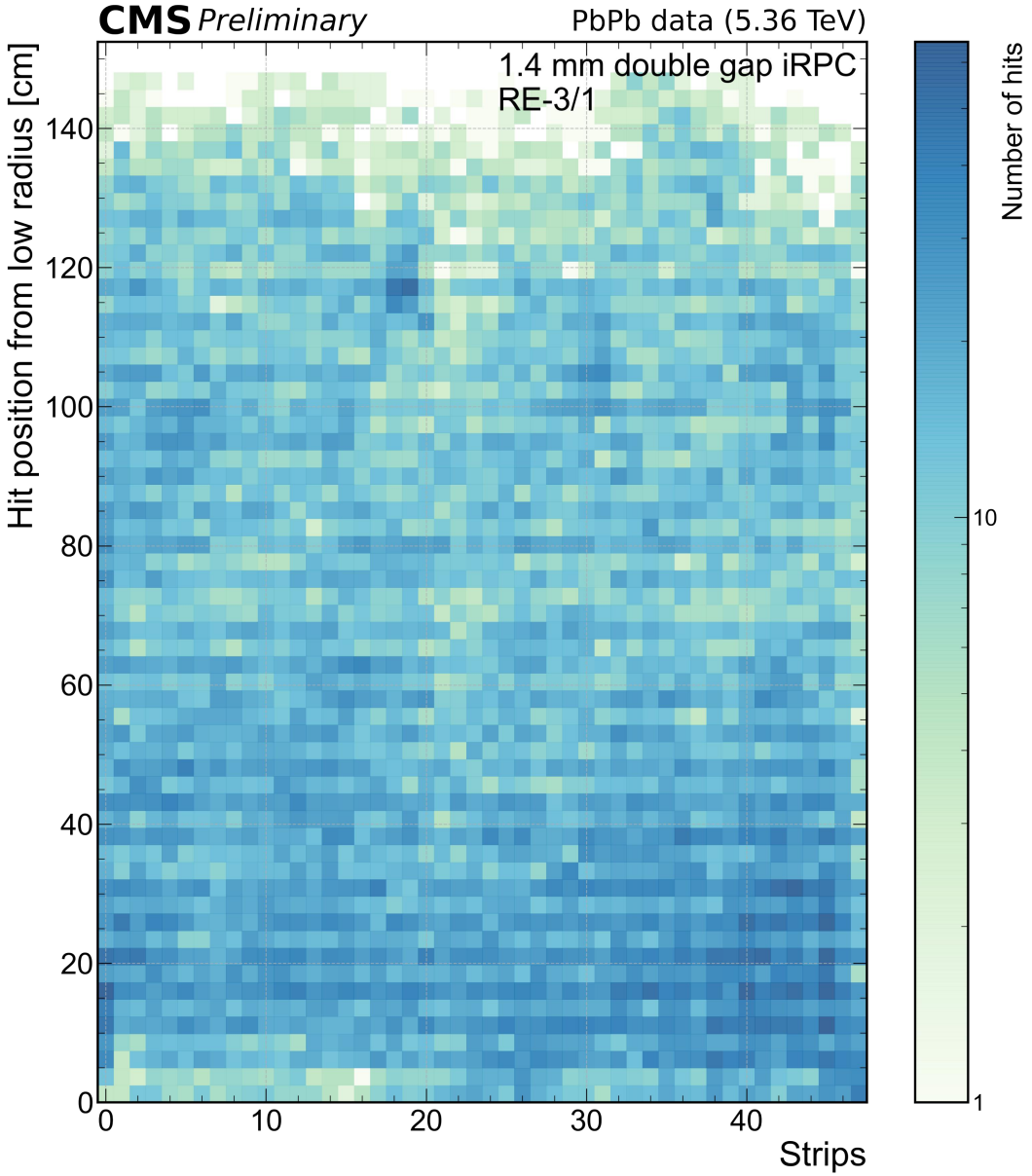
DeMux Algorithm

- Problem: the uplink can only transmit 3 TDC Data per BX (Bunch crossing); when a BX produces more than 3 datas, the extra ones get delayed in transmission — so the backend must reconstruct each hit's original timing before clustering
- Delay = backend BX number − hit's BX number , how many BX ago TDC Data was generated
- 2D delay buffer: hits are sorted into a table by delay; each BX the table advances one step, and the oldest row is read out into a 96-channel RAM to restore the hit pattern
- Readout trigger: once a hit's delay reaches the set depth limit, it is read out



Schematic of the DeMux algorithm

Hit profile in self-trigger



> The plot shows a 3D position of reconstructed hits at CMS Point 5, at a working point of HV 7.13 kV, corresponding to a charge threshold of ~40 fC.Data was taken during LHC heavy-ion stable beams, using self-trigger mode, where the back-end algorithm generates a trigger upon detecting a valid cluster flag. The hit position accounts for the time difference between both ends of the readout strip:

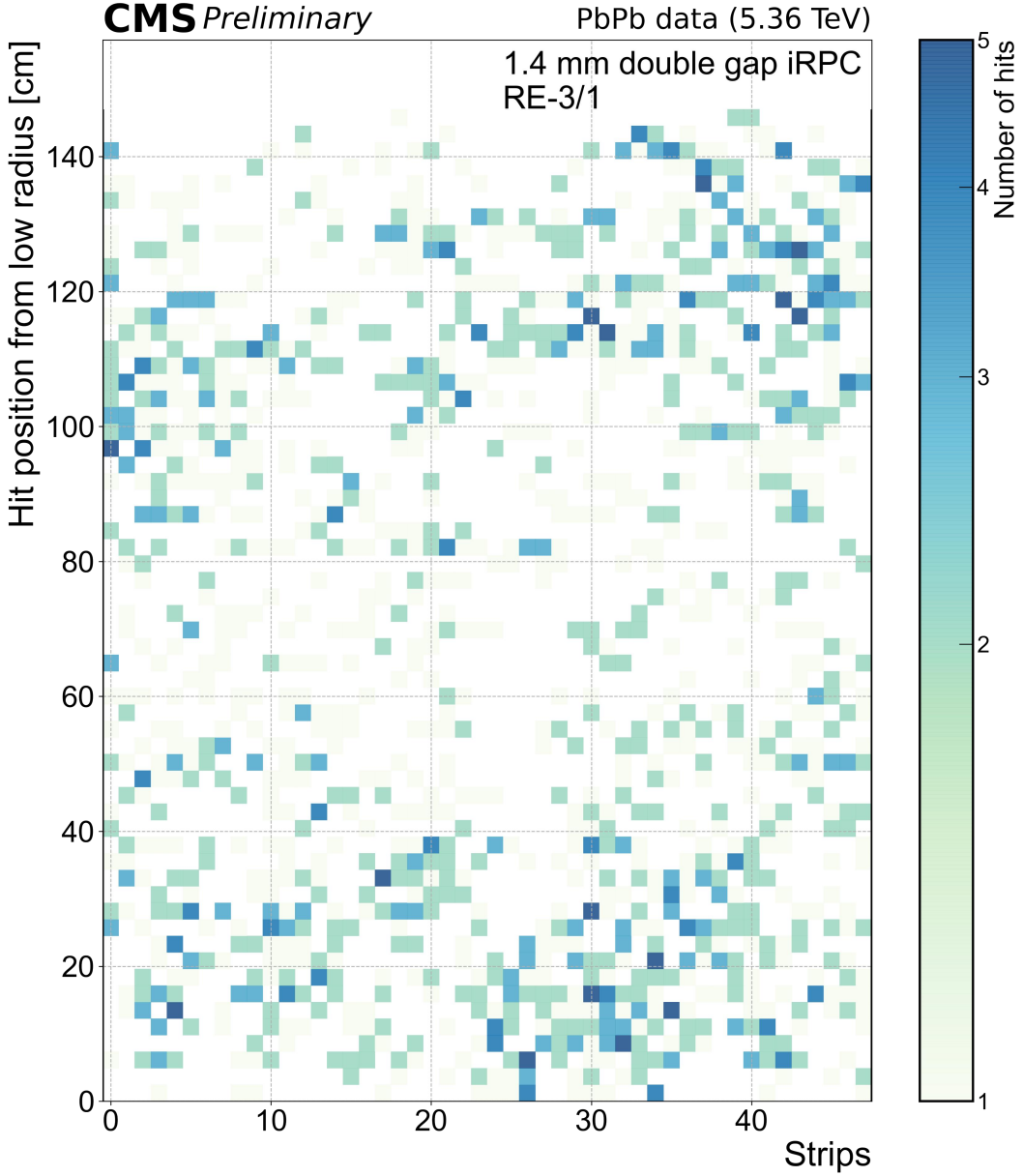
$r = L/2 - v(t2 - t1)/2$, where L is the strip length, $t2 - t1$ is the arrival time difference between the low- and high-radius ends, and v is the signal propagation speed (~0.6c).

"Low radius" and "high radius" refer to the two ends of a readout strip along the radial direction, with "low radius" being the end closer to the beam axis and "high radius" the end farther away.

Number of events:30000

Number of TDC hits (double ends TDC data):44613

Hit profile in global-trigger



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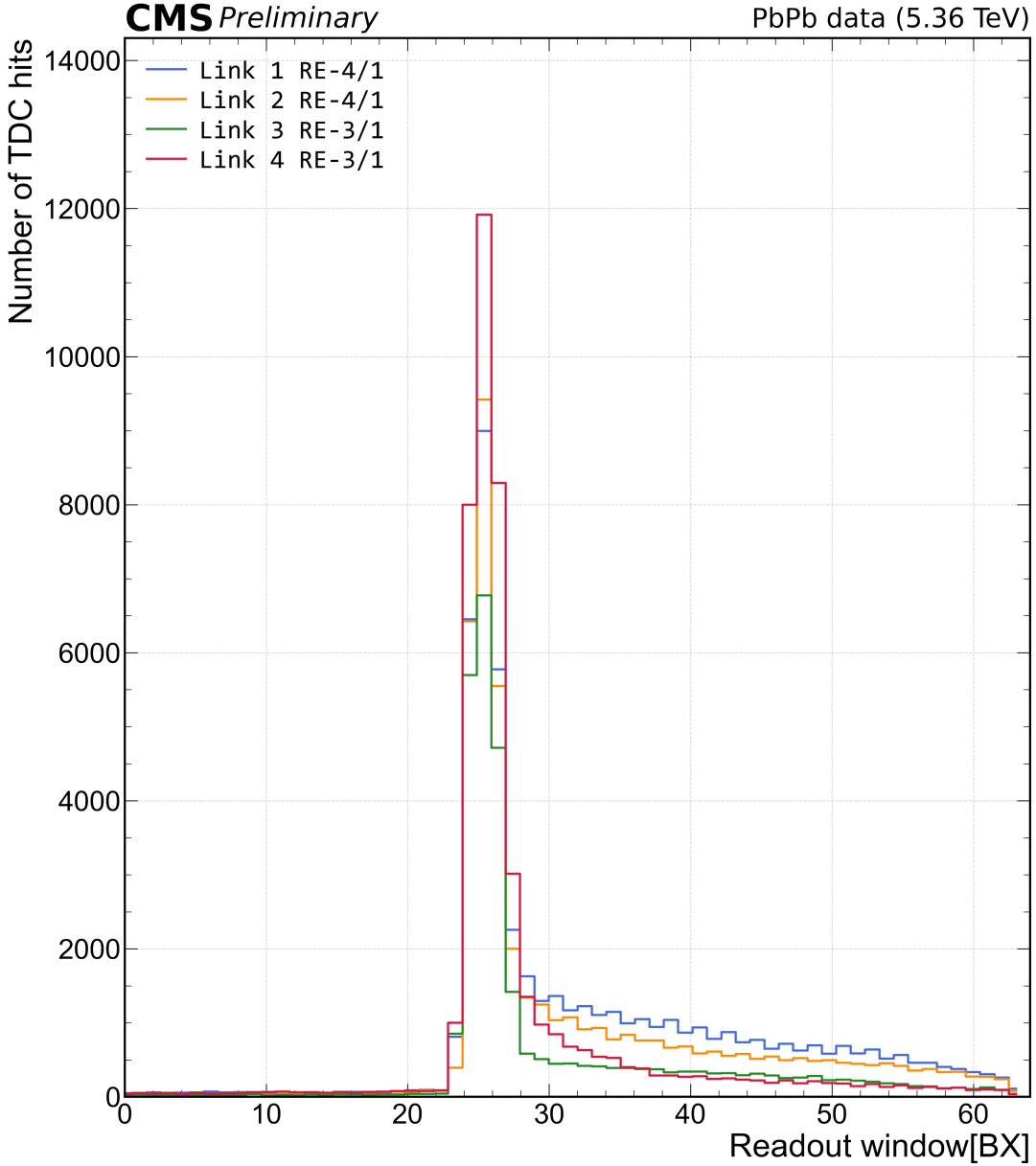
"Low radius" and "high radius" refer to the two ends of a readout strip along the radial direction, with "low radius" being the end closer to the beam axis and "high radius" the end farther away.

Number of events:40000

Number of TDC hits (double ends TDC data):1963

Readout window distribution in self-trigger



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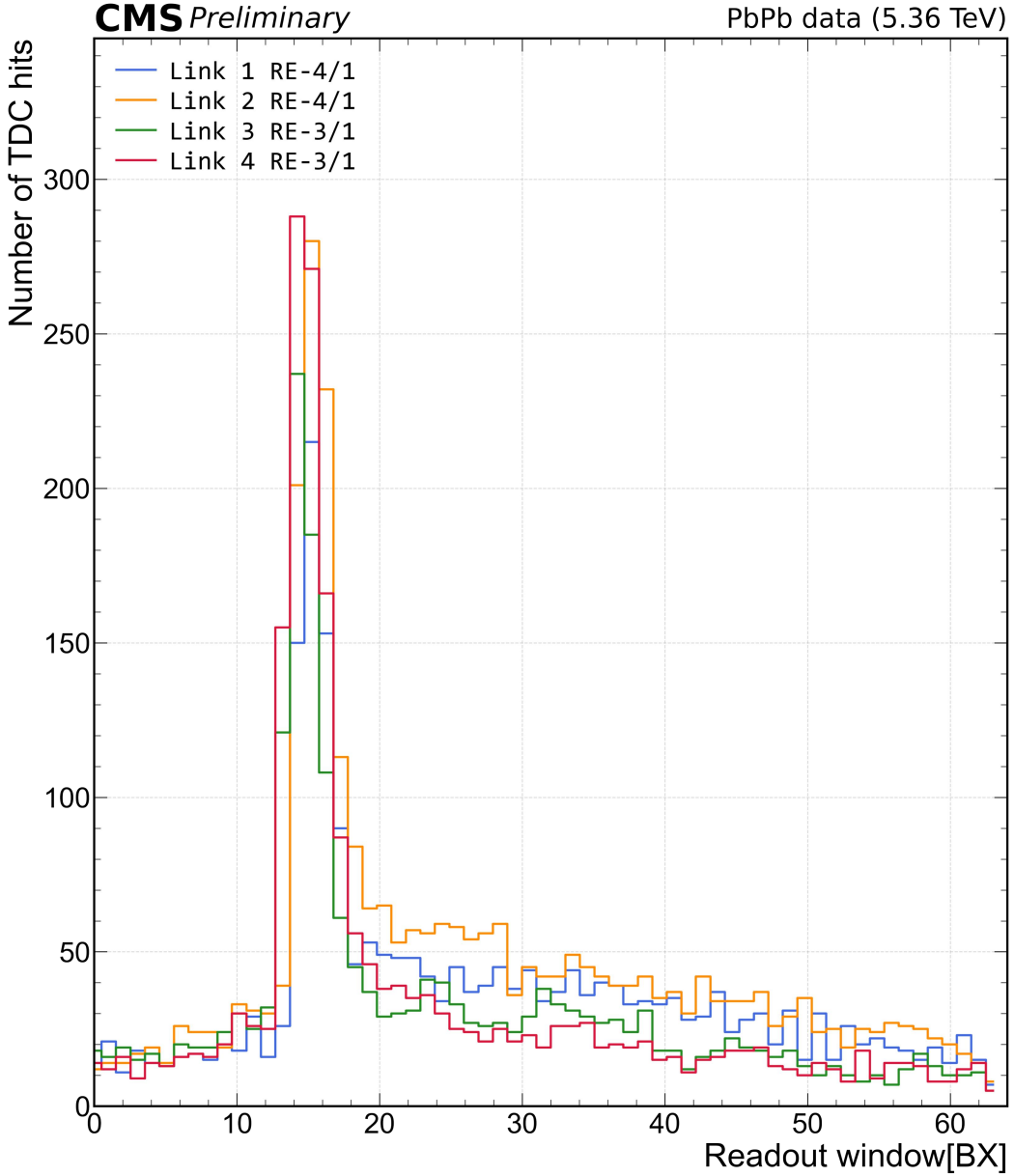
Data was taken in self-trigger mode, where the back-end algorithm generates a self-trigger signal for data-taking upon detecting a valid cluster flag.

A clear data peak confirms the correctness of the back-end algorithm, while the tail of the peak arises from transmission delay.

Readout window distribution in global-trigger



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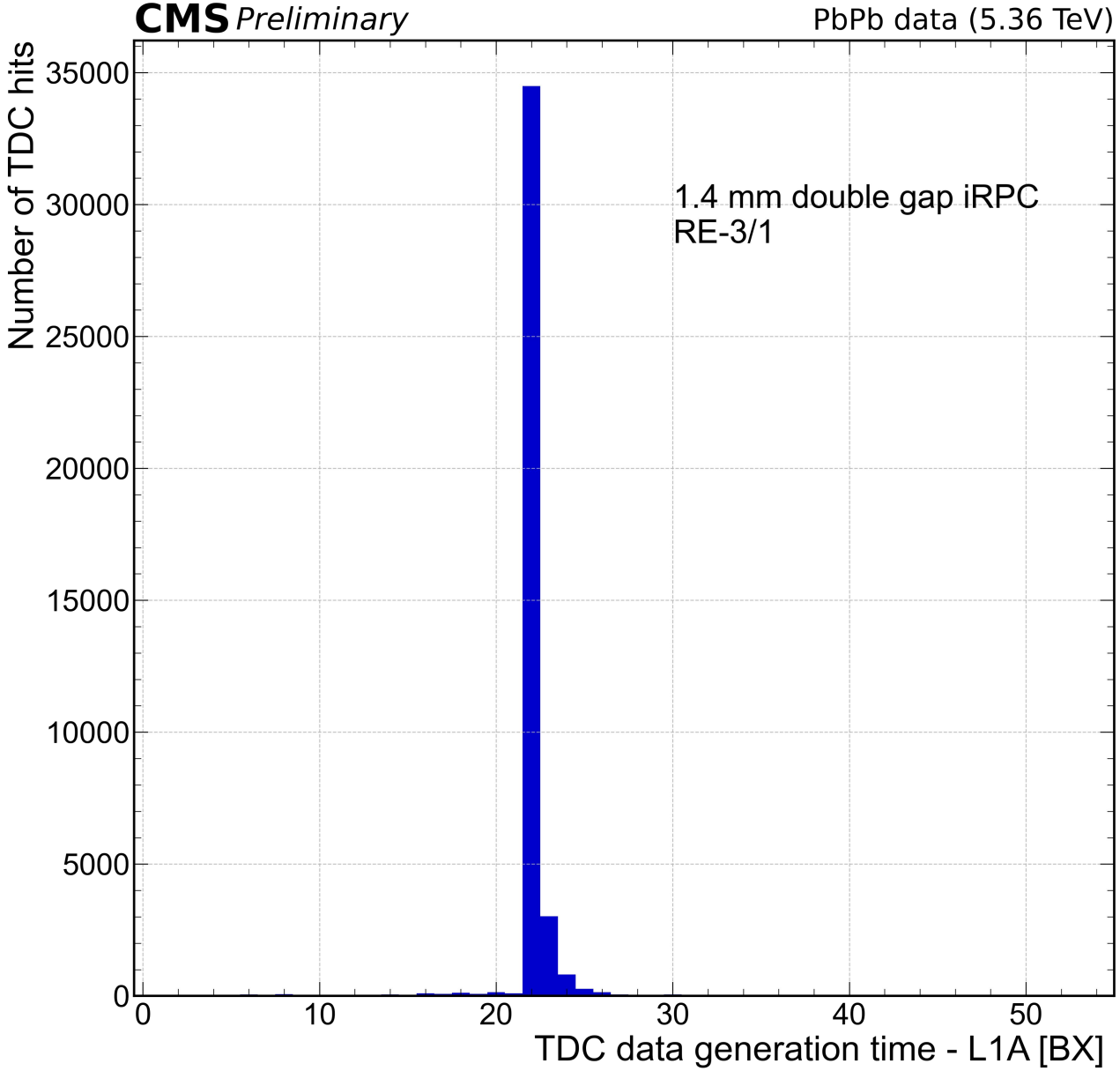
Data was taken using the CMS Global Trigger signal.

A clear data peak confirms correct delay alignment between the iRPC detector data and the CMS Global Trigger, while the tail of the peak arises from transmission delay.

Timestamp distributon in self-trigger



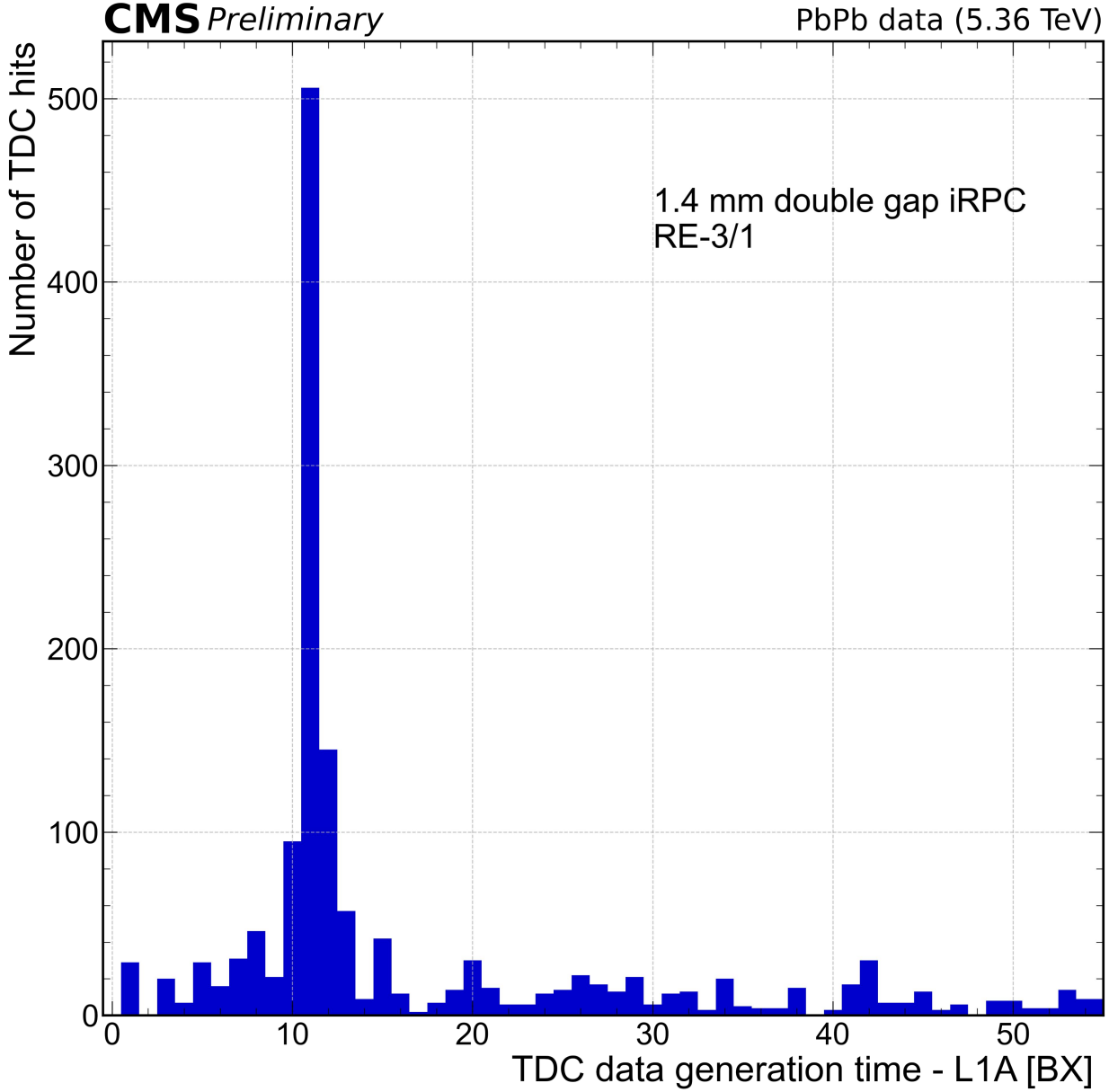
> The plot shows the difference between the TDC data generation time and the L1A (Level-1 Accept) trigger timestamp within the back-end readout window, with the X-axis representing this time difference. This distribution does not account for the order in which data arrives at the back-end, ignoring transmission delay, and directly reflects the timing relationship between the data and the L1A signal.

Data was taken in self-trigger mode, where the back-end algorithm generates a self-trigger signal for data-taking upon detecting a valid cluster flag.

Number of events:30000

Number of TDC hits:44613

Timestamp distributon in global-trigger



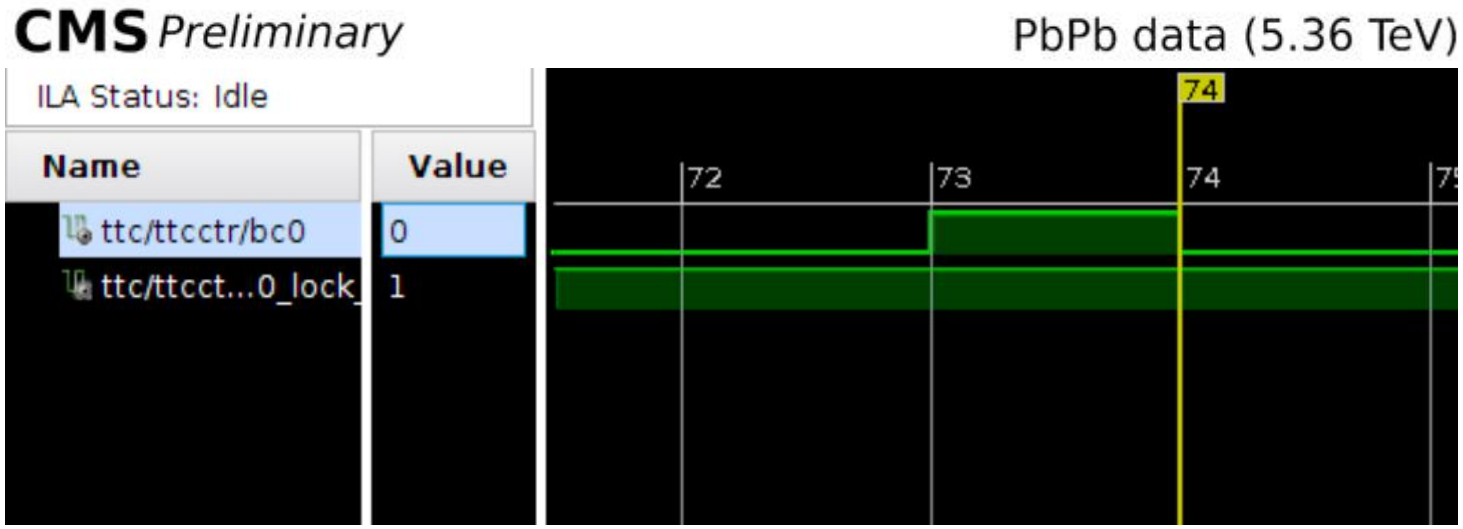
> The plot shows the difference between the TDC data generation time and the L1A trigger timestamp within the back-end readout window, with the X-axis representing this time difference. This distribution does not account for the order in which data arrives at the back-end, ignoring transmission delay, and directly reflects the timing relationship between the data and the L1A signal.

Data was taken using the CMS Global Trigger signal.

Number of events:40000

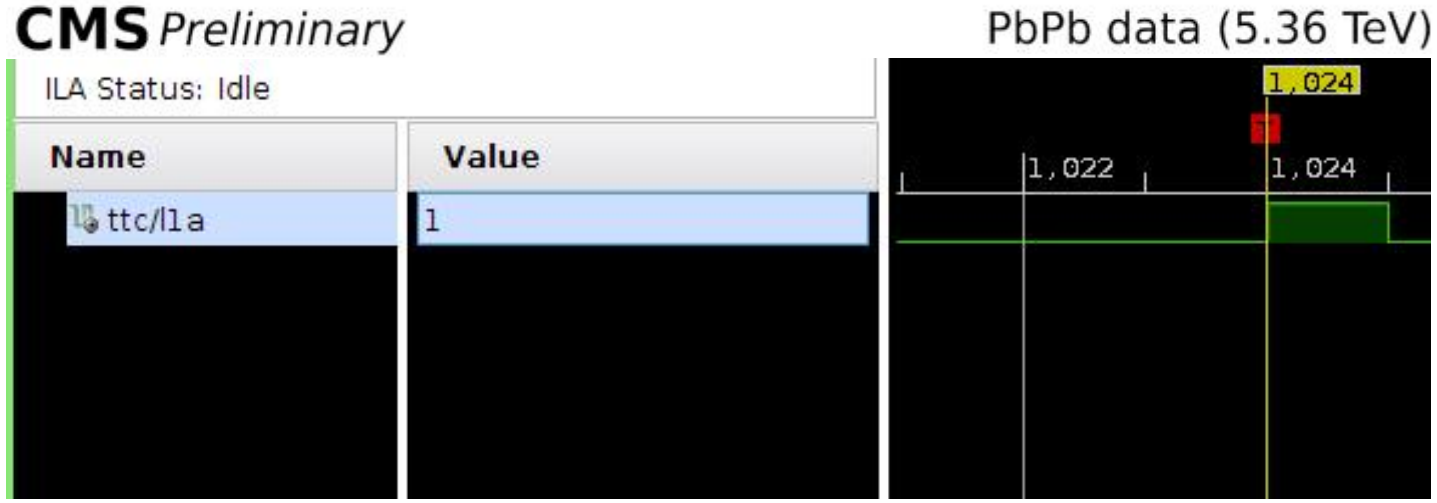
Number of TDC hits:1963

ILA window for TTC signal



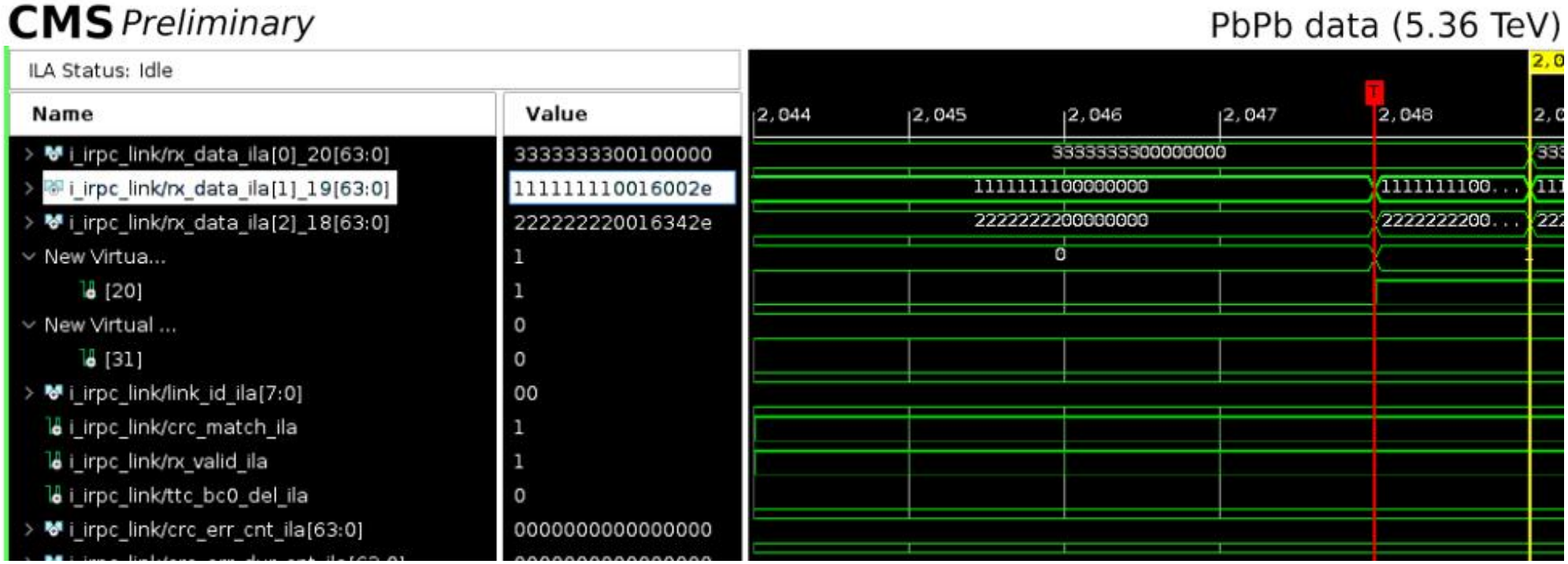
> ILA (Integrated Logic Analyzer) waveform captured within the back-end firmware, used for real-time, on-chip probing of internal signal values. This capture shows the TTC decoding module on the back-end successfully extracting the BC0 signal from TCDS via AMC13 — the rising edge of the ttc/ttcctr/bc0 signal at timestamp 73 marks the arrival of the BC0 pulse.

ILA window for TTC signal



> ILA (Integrated Logic Analyzer) waveform captured within the back-end firmware, used for real-time, on-chip probing of internal signal values. This capture shows the TTC decoding module on the back-end successfully extracting the L1A signal from TCDS via AMC13 — the rising edge of the ttc/l1a signal at timestamp 1024 marks the arrival of the Global L1A.

ILA window for EMTF data receiving



> ILA (Integrated Logic Analyzer) waveform captured within the back-end firmware, used for real-time, on-chip probing of internal signal values.This capture shows the EMTF side for monitoring the data reception window of iRPC trigger data.

The final row, crc_err_cnt_ila, remains at zero throughout the test window, indicating no CRC errors and a stable link.

The first three rx_data_ila rows show data matching the expected frame format：
Upper 32 bits [32:63] — placeholder
Lower 32 bits [0:31]:

[0:3] sub_bx	— 4 bits
[4:9] eta info (segment_info)	— 6 bits
[10:16] phi info (strip_info)	— 7 bits
[17:19] cluster size	— 3 bits
[20] cluster valid flag	— 1 bit
[21:30]	— reserved
[31] BX0 flag	— 1bit