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LHCb VELO upgrade phase II: a 4D silicon vertexing detector

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LHCb plans an Upgrade II detector for 2034 to operate at luminosities of 1.5x1034cm−2s−1, accumulating over 300 fb−1. This will result in about 42 interactions per crossing, producing approximately 2000 charged particles within acceptance. The higher luminosity requires a new VErtex LOcator (VELO) with enhanced capabilities to handle increased data rates, radiation levels, and occupancies. New techniques are needed to assign b hadrons to their primary vertices and perform real-time pattern recognition, involving a new 4D hybrid pixel detector with advanced rate and timing capabilities. Prototype front-end ASICs are under design in 28 nm technology, including large processing power and rapid analog response, which requires fast rise times and high power consumption, yet limited by vacuum operation and cooling constraints. The ASIC must handle extreme hit rates and added timing information. The sensor must provide time measurements with 35 ps resolution and resist to $2.5x10^{16}$ 1 MeV neq cm−2, while keeping the and spatial resolution below 9 μm. The mechanical design will minimize material and achieve an integrated module with thinned sensors and ASICs combined with lightweight cooling. This presentation will review the technologies for the HL-LHC upgrade, with a particular focus on achieving precision timing for vertexing in next-generation detectors. Special emphasis will be placed on the technological R&D in data acquisition and processing, which extends beyond the LHCb collaboration and is essential for handling data volumes generated by the VELO.

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