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Performance of HPSoCv2: measurements on a very high Channel Density Waveform Digitizer with sub-10ps resolution

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In recent years, the introduction of very fast optical sensors with extremely low pitches (e.g. Low Gain Avalanche detectors -LGADs) has enabled high-density designs for high energy and nuclear physics detectors offering excellent spatial and timing precision; to harness the extreme spatial and timing resolution achievable with such devices, novel high performance/high channel density readout systems are required. For this reason we studied and designed the architecture of the HPSoC, a customized multi-channel waveform digitizing readout that is capable of directly interfacing with state-of-the-art sensor arrays, can self trigger and extract relevant information from the waveform derived from each pixel and internally distill such information in a compact digital format, with timing precision at the few picoseconds level and capable of sub-pixel spatial precisions at a few tens of micrometers or less.
In order to demonstrate the feasibility of the design and test some of its critical components, a staged approach was followed, and we will report on the various measurements on the performance of the second revision of the chip, the HPSoCv2, a 4 channel device with direct interfacing to LGAD sensor array, sampling speed in excess of 10 Gsps and demonstrated timing resolution below 10 ps. In particular, we will discuss the various measurements on the input front end, composed of a sensitive TransImpedance Amplifier designed to capture the salient timing and energy features of a typical LGAD detector, both on pixels and strips. We then discuss the characterization and performance of the fast digitizer (10-14Gsps) with input calibration signals, discussing the timing resolution achievable and potential feature extraction mechanisms. We finally show some initial test of readout of pulses that are acquired using the entire chain (LGAD, TIA, digitizer).

We will conclude with a discussion on the improvements and additional features that have been added to the third revision of the chip (HPSoCv3), for which testing is imminent.

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