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Characterization of the MetaRock prototype TDC for future HEP experiments

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Detectors at future colliders will require timing precision on the order of 10 ps. Towards this goal, we've developed a low-power, high-speed prototype ASIC in 28nm CMOS named MetaRock. MetaRock is an evolution of the Pebbles ASIC. As compared to its predecessor, MetaRock includes a prototype low-power TDC based on a time stretching circuit. An on chip test bench consisting of a charge injection circuit and a second high-resolution (20 ps LSB) TDC are used for evaluating the performance of the low-power TDC. We will present the low-power TDC and testbed architecture and summarize the test results of the prototype. In addition, a characteristic study of the FE architecture, motivated by the MetaRock performance, is presented with lessons learned for future prototype structures.

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