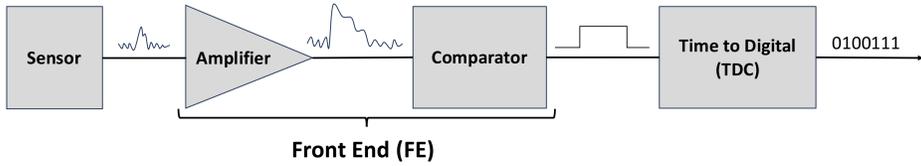


## 1. Motivation

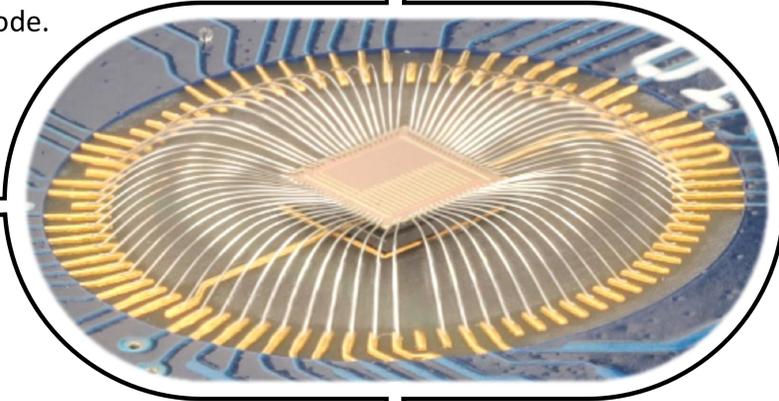
- Many future collider scenarios require precision timing of  $\mathcal{O}(50 \text{ ps})$  on **time of arrival (TOA)** for particles [1].
- They will also require resolution on the **time over threshold (TOT)** to quantify the charge of a signal.
- The time resolution of a signal has contributions from the sensor, amplifier, comparator, and digitization.



- Detector constraints create tight requirements for the **analog front end (AFE)** and **time-to-digital converter (TDC)**:
  - Small area to match a small sensor pitch.
  - High hit rate for high pileup or high beam induced background environments.
  - Low mass to minimize back scattering of particles.
  - Low power to minimize heat generation which would require more material for cooling.

Variable	Target	Note
Time Resolution	< 50 ps	at $3 ke^-$
Analog Area	$35 \mu\text{m} \times 35 \mu\text{m}$	Split with TDC analog component
Analog Power	$5 \mu\text{W}$	Split with TDC analog component
Threshold	$1000 e^-$	$100 e^- \text{ ENC}$

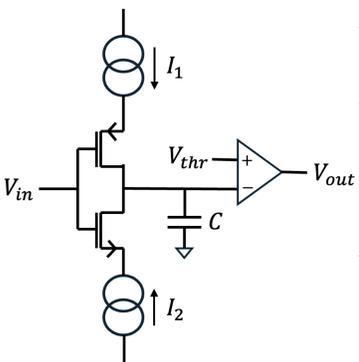
- **MetaRock** is fabricated in the **28 nm CMOS** node.
- Migrating to a small CMOS node allows for:
  - More logic elements per area, smaller propagation delays, and lower power consumption.



## 2. Design

- The MetaRock ASIC is an evolution of the Pebbles ASIC [2].
- Prototype **low-power TDC (LPTDC)** based on a **time stretch circuit** [3] which uses a 40 MHz clock.
- Characterization test-bed includes:
  - Low-jitter GHz clock
  - **Charge Injection Circuit** synchronized with GHz clock
  - **High-power TDC (HPTDC)** for characterizing the prototype devices
  - 16 channels with different input sensor capacitances (0-150 fF)

### Time Stretch Circuit

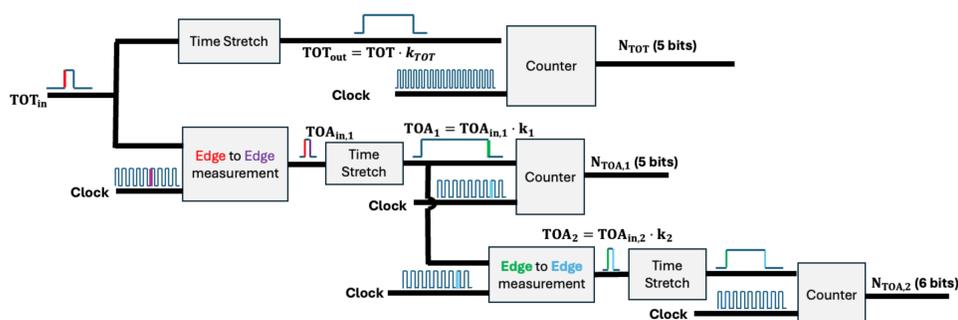


- The time stretch circuit multiplies an input pulse width by a stretch factor,  $k$ .
- A capacitor  $C$  is rapidly discharged by a constant current  $I_1$  for the input pulse duration  $V_{in}$ , then recharged at a smaller constant current  $I_1$ .
- A discriminator monitors the capacitor voltage and outputs a pulse  $V_{out}$  with width

$$V_{out} = V_{in} \cdot \left(1 + \frac{I_2}{I_1}\right) = V_{in} \cdot k$$

### LPTDC Architecture

- One stage of the time stretch circuit is used for measuring the TOT.
- Two stages of the time stretch circuit are used to measure the TOA.



## 3. Characterization Results

- The prototype is characterized at LBNL.

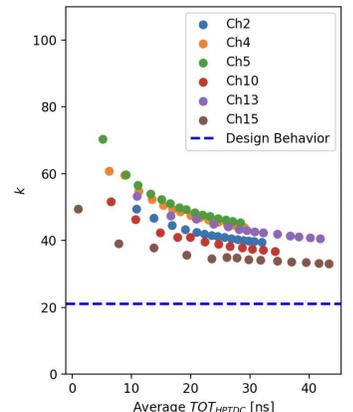
### Characterizing the Time Stretch Circuit

- The TOT pulse is an input to a stretch circuit and measured by the HPTDC, so this stage allows for characterizing the stretch factor.
- The output of the LPTDC counter is

$$N_{TOT} = \frac{TOT_{HPTDC} \cdot k}{25 \text{ ns}}$$

### Stretch Factor Observations

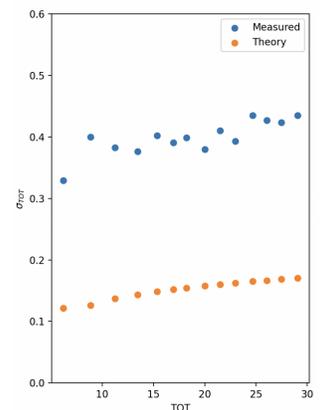
1. Higher magnitude stretch factor than anticipated.
2. Depends on the input pulse duration.
3. Depends on the channel, implying sensitivity to device mismatch.



### Characterizing the TOT Time Resolution

- The expected TOT resolution is

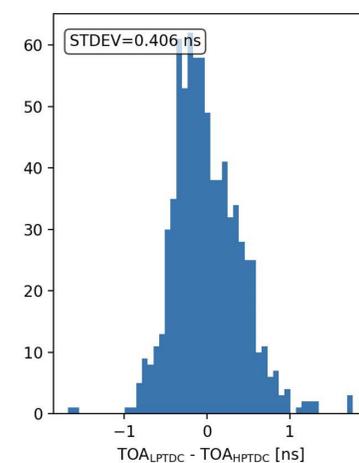
$$\sigma_{TOT}(TOT) = \frac{25 \text{ ns}}{\sqrt{12} \cdot k_{TOT}(TOT)}$$



- The TOT measured by the LPTDC can be compared to the HPTDC to measure its resolution.

- The resolution is better for shorter TOT since  $k_{TOT}$  is larger.

### Characterizing the TOA Time Resolution



- The TOA input pulse length depends on the stretch factor of the two stages ( $k_{TOA,1}$ ,  $k_{TOA,2}$ ).
- The input pulse length can be related to the HPTDC TOA measurement, but it depends on the phase between the GHz clock and the 40 MHz clock and the stretch factor.
- The stretch factor is unknown, and is therefore parameterized as

$$k(N) = A \cdot e^{-B \cdot N} + C$$

- Expected resolution:

$$\sigma_{TOA,1} = \frac{25 \text{ ns}}{k_{TOA,1}} \text{ and } \sigma_{TOA,2} = \frac{25 \text{ ns}}{k_{TOA,1} \cdot k_{TOA,2}}$$

### Time Resolution Observations

- The first stage TOA resolution  $\mathcal{O}(650 \text{ ps})$  and the first stage TOT resolution  $\mathcal{O}(500 \text{ ps})$  are comparable with differences attributable to differences in the stretch factor.
- The second stage stretching improves the time resolution to  $\mathcal{O}(400 \text{ ps})$ , but not to the expected  $\mathcal{O}(50 \text{ ps})$ . Further improvements are needed.

## 3. Outlook

- A prototype low power TDC based on a time stretch circuit has been fabricated using the 28 nm CMOS technology and tested.
- Unexpected behavior in the time stretch circuit created a difficult calibration and reduced the time resolution from the predicted value.
- Future editions of the prototype will include (1) direct measurements of the input pulse duration for the TOA circuit and (2) differential switches to stop errant charge injection.