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Low-Latency Graph Neural Network Implementation for Charged Track Reconstruction

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Graph Neural Networks (GNNs) have proven effective for edge classification in particle track reconstruction at the LHC. In this context, our GNN is trained in PyTorch to identify edge candidates—line segments connecting pairs of detector hits originating from ionizing particles. We present an FPGA-based emulator of such a GNN that achieves, to our knowledge, the fastest reported clock speed for this task, 290 MHz. Our approach replaces the original NN engines with boosted decision trees (BDTs) that regress the outputs of its three constituent models (two relational networks and one object network). These models are then mapped onto the FPGA fabric using the software package fwXMachina, enabling a design that uniquely uses no digital signal processors (DSPs). Along with its resource efficiency, the emulator is predicted to reproduce the GNN's edge-classification AUC to within three decimal places. Looking ahead, this 290 MHz design can be integrated with optimized HDL architectures to significantly reduce trigger-level latency in particle track reconstruction for the LHC, paving the way for real-time deployment of ML-based tracking algorithms.

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