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Aligning data to better than one picosecond.

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Of the many items that need to be considered in a push towards one -picosecond timing for particle detectors, we have focused on one essential component: the distribution of references clock with an inter-channel precision of 100 femtoseconds (fs) or less. Our program has been to develop the tools to measure a reference clock to this level of precision using a digital dual mixer time difference (DDMTD) circuit and to adjust the phase of a clock in steps of 200 fsec with a custom ASIC the DCPS for digitally controlled phase shifter. Our original DDMTD was built with discrete high-speed flip flops, readout with an FPGA. With this we have achieved a single measurement precision of 400 fs or better, and with multiple measurements made over a period of 10 seconds we have achieved a resolution of 100 fs. Based on this experience we have designed new circuitry to manage better the metastability of the flip flops so as to achieve an improvement of approximately a factor 10 in the precision. We have used our improved DDMTD and the DCPS to stabilize a reference clock at the end of a 1 km mono-mode optical fiber to a precision of 100 fs over a period of two days.

In the next step in our program we are designing an ASIC that includes the DDMTD circuit and the new logic. The DDMTD circuit has been designed with CML logic in the TSMC65LP process and the first version with the DDMTD and test logic has been received and is under test. The next variation of this ASIC will include the logic to manage the metastability that we have demonstrated with discretes. We will also design it to be radiation tolerant so that it can be installed on-detector, which is essential to achieving sub-picosecond timing precision across large scale systems.

Authors: RUSACK, Roger (University of Minnesota (US)); Dr SARADHY, Rohith (The University of Minnesota)

Co-authors: Mr VADNAIS, Emily (The University of Minnesota); Mr FRAHM, Erich (The University of Minnesota); Prof. TOUSI, Yahya (The University of Minnesota)

Presenter: RUSACK, Roger (University of Minnesota (US))

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