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CHARMS250: A Cryogenic Front-End ASIC for Low-Noise Readout of Charge or Light Signals

Wednesday 8 October 2025 20:00 (20 minutes)

In this talk, we will present CHARMS250V1, a cryogenic front-end application specific integrated circuit (ASIC) developed using a 65 nm process for low-noise readout of charge or light signals produced in noble liquid detectors. The design of CHARMS250V1 has evolved from the LArASIC chip, which was manufactured in a 180 nm process and has been selected as the first component in the 3-ASIC readout solution for Phase I of the Deep Underground Neutrino Experiment (DUNE). CHARMS250V1 is designed to operate at temperatures ranging from room temperature (RT) down to liquid nitrogen temperature (LNT), i.e., 77 K. It comprises of a single channel containing pre-amplification and pulse shaping stages that provide charge gain programmable in the range of ~ 4 –25 mV/fC, peaking time programmable between 250 ns and 2 μ s, and programmable baseline of either 200 mV or 900 mV for processing of unipolar and bipolar signals, respectively. CHARMS250V1 is the first prototype of this design that has been submitted for fabrication, prior to the design of the full 16-channel ASIC.

CHARMS250V1 also features enhanced digital programmability of all bias voltages and currents through 7-bit digital-to-analog converters (DACs), improving its robustness for operation at a wide range of temperatures ranging between RT and LNT. Global and channel registers used to set operational conditions of CHARMS250V1 are programmed through a two-wire I2C interface. Applications for CHARMS250V1 include light/charge readout of the Far Detector (FD) 3/4 in Phase II of DUNE, charge readout in the future circular lepton collider (FCC-ee), light readout in nEXO, and the silicon-based active target and liquid xenon calorimeters in PIONEER.

Author: MUKIM, Prashansa (Brookhaven National Laboratory)

Co-authors: ZHANG, Chao (Brookhaven National Laboratory); GORNI, Dominik (Brookhaven National Laboratory); CARINI, Gabriella; PINAROLI, Giovanni; DEPTUCH, Grzegorz (Brookhaven National Laboratory); CHEN, Hucheng (Brookhaven National Laboratory); GALLICE, Niccolo' (Brookhaven National Laboratory); MAJ, Piotr (Brookhaven National Laboratory); RESCIA, Sergio (Brookhaven National Laboratory); GAO, Shanshan (Brookhaven National Laboratory); MANDAL, Soumyajit (Brookhaven National Laboratory)

Presenter: MUKIM, Prashansa (Brookhaven National Laboratory)

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