Cryogenic Testing of CRYO ASIC for Photon Readout

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1. UC San Diego, 2. U Hawaii, 3. SLAC

Silicon Photomultiplier (SiPMs) for Noble Liquid TPC

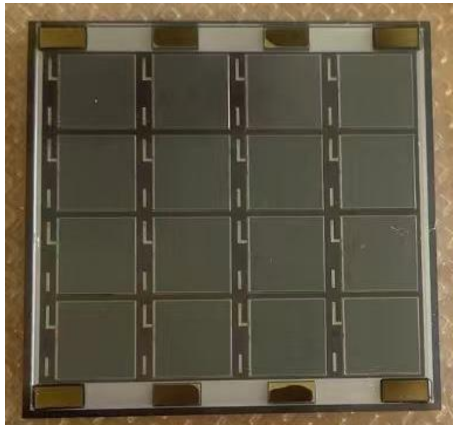
SiPM have increasingly become the technology of choice for noble liquid detectors.

Pros:

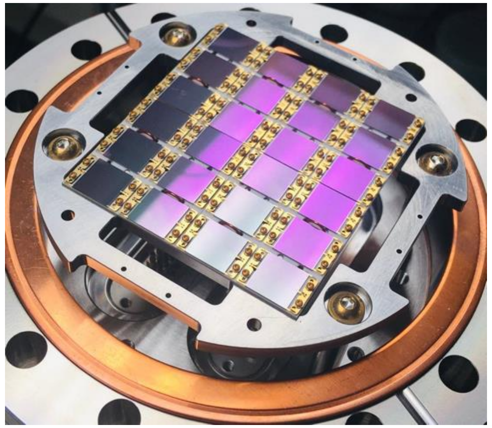
- High gain (~1e6)
- Low radioactivity
- Immune to magnetic field
- Compact

Cons:

- High dark rate
- After pulse and cross talk
- Large capacitance per unit area



Hamamatsu Minitile



FBK SiPM Array

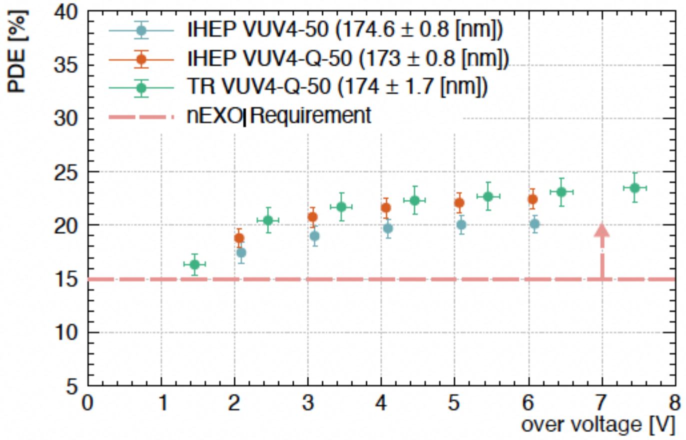
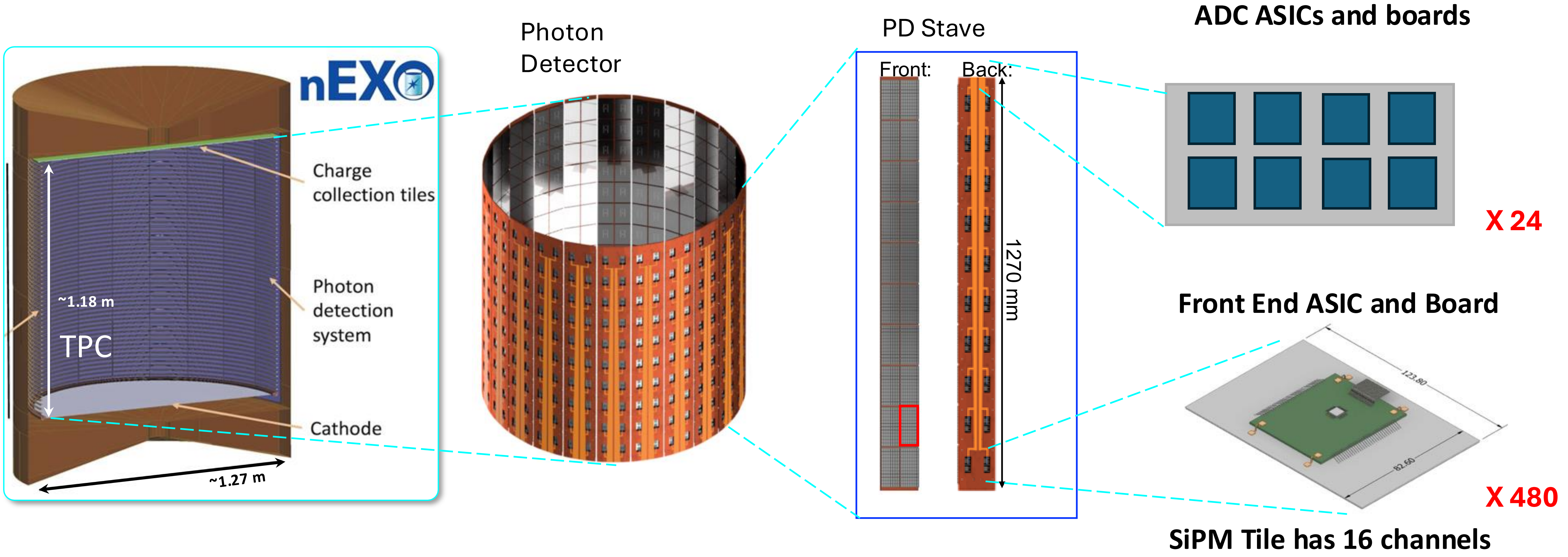


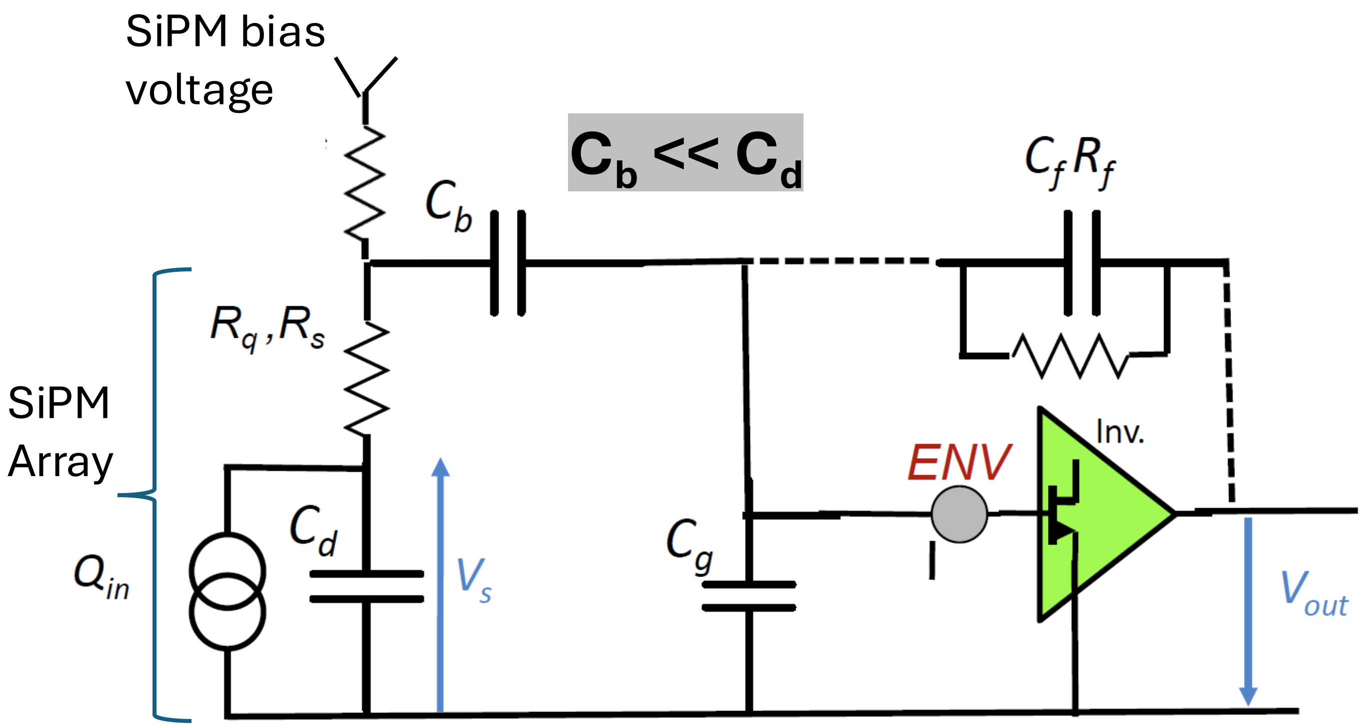
Photo detection efficiency of HPK VUV4 MPPCs

nEXO Light Readout System Conceptual Design



- The photon signals are collected by SiPMS then amplified by Front End ASIC
- The analog signals from 20 SiPM tiles on a photodetector stave are and digitized by ADC ASICs
- Digitized signals (waveform snippets) are multiplexed and transmitted to DAQ
- The system has a total of ~ 7,680 channels

Readout for SiPMs: Weak coupling to amplifier



Q_{in}= avalanche charge
C_d =capacitance of SiPM array in parallel

Readout challenge:
Large capacitance/channel,

- **~5-12 nF** (series connection C_{2s})
- **~20-50 nF** (SiPMs in parallel).

SiPM Signal Detection with small coupling C_b:

***S/N analysis** shows: C_b must be larger than C_g, but can be **much smaller** than C_d:*

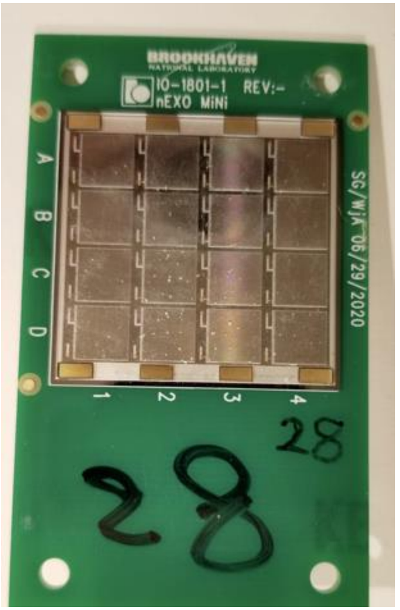
C_d>>C_b>>C_g
e.g., 20 nF>>0.5 nF>>25 pF

Concept, realization, tests by
H. Chen, S. Gao, V. Radeka, S. Rescia, T. Tsang

SiPM Readout with LArASIC (BNL)

Concept, realization, tests by
H. Chen, S. Gao, V. Radeka, S. Rescia, T. Tsang

HPK minitile board

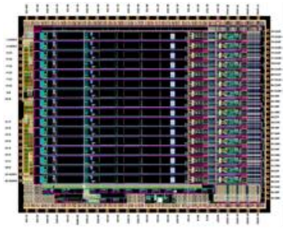


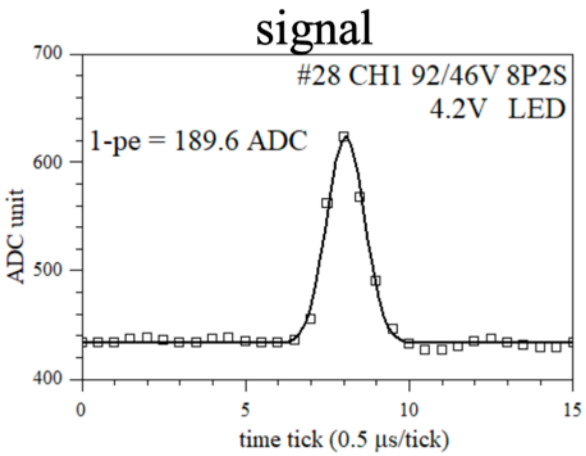
16 x (0.6 x 0.6) cm^2
active area=5.76 cm^2

C_{total}(16P) SiPM tile ~ 20 nF

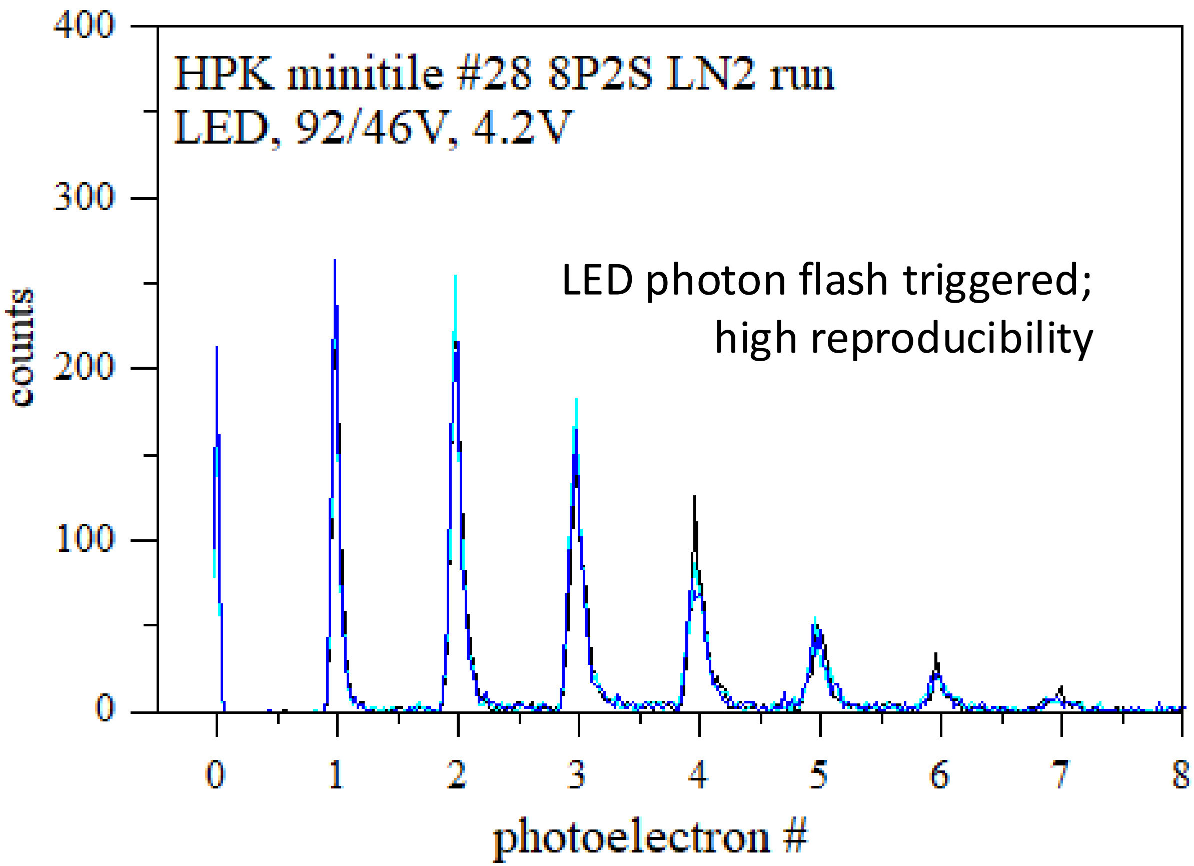
C_{total}(8P2S)
SiPM tile = 4.8 nF

LArASIC (180 nm)





Single p.e. waveform information provided by a "snippet" of samples

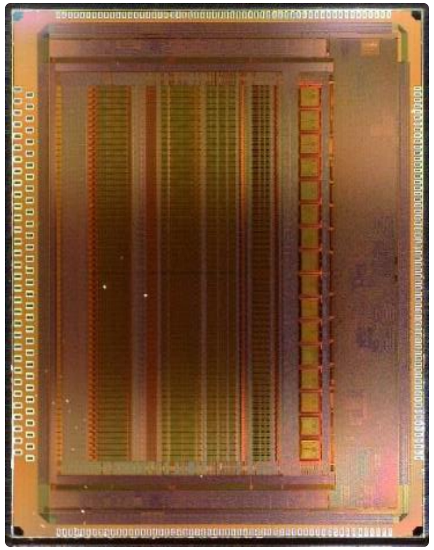


LED photon flash triggered;
high reproducibility

- A demonstration of the readout concept was performed using LArASIC and HPK SiPMs
- 1-p.e. S/N ~ 60 ; avalanche = 0.4 pC at OV=4 V, 1-p.e. resolution (δE): 3 to 3.5% rms
- 1-p.e. coincidence resolution <u>between two subarrays</u> < 20 ns

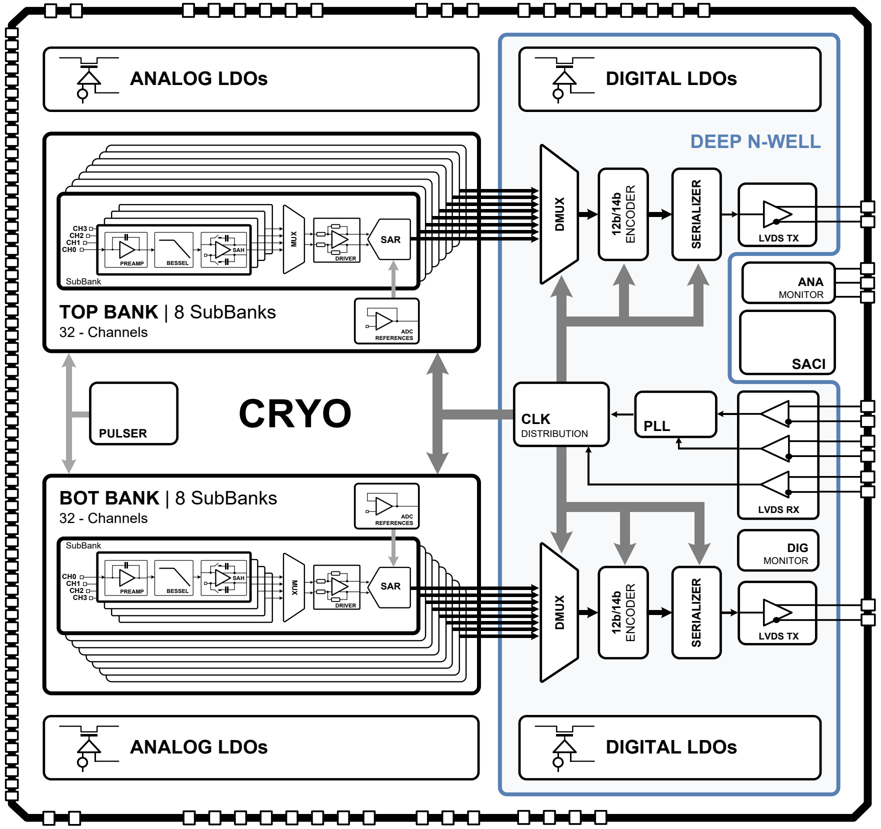
CRYO ASIC Design and Specifications

CRYO Photograph R&D Prototype
~7mm x 9mm



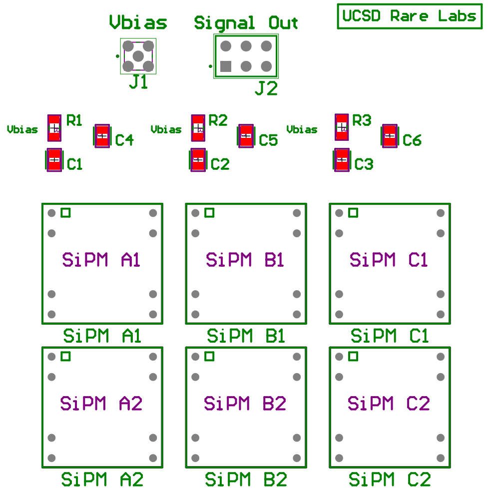
TPC Experiment	DUNE			
CMOS process	130nm			
Supply voltage	2.5V (2V, 1V internal)			
Input capacitance	~ 220pF			
Anti-aliasing filter	5th order Bessel architecture			
Peaking times	0.6us, 1.2us, 2.4us, 3.6us			
Gain settings	6.0X (28.6mV/fC)	3.0X (14.3mV/fC)	1.5X (7.1mV/fC)	1.0X (4.8mV/fC)
Max. input charge	50fC	100fC	200fC	300fC
Noise	~500e- @ 3.0X and 1.2us			
Resolution	12 bit			
INL and DNL	±1LSB			
Sampling frequency	2MSPS			
Temperature	87K (-186°C)			

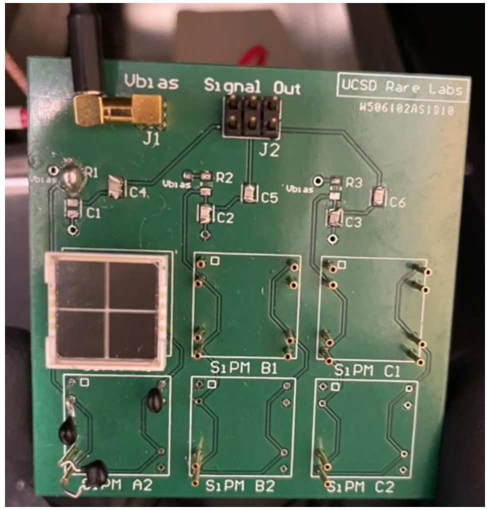
Architecture
System-On-Chip CRYO ASIC R&D Prototype

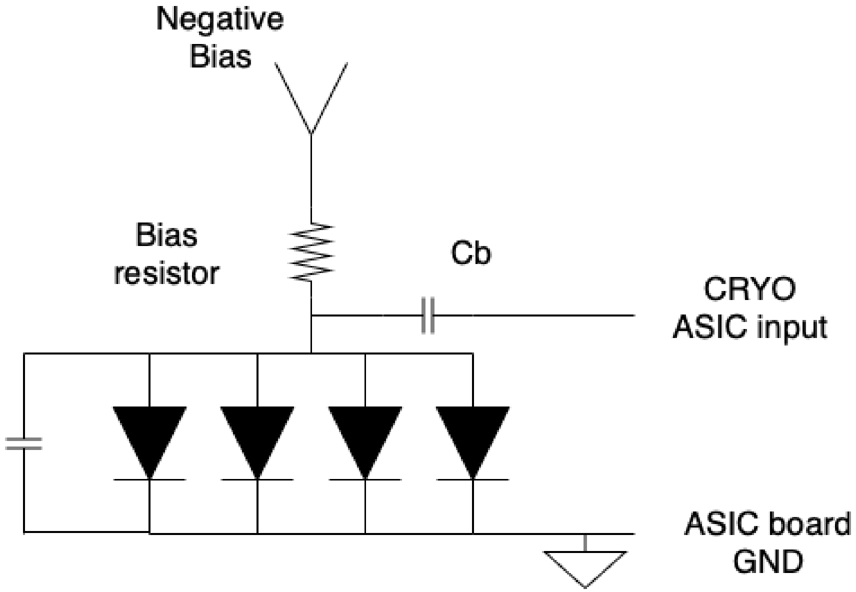


- System-On-Chip (SoC) ASIC minimizing interconnections - All functionalities in a single chip per tile with minimal number of I/O. Does not require active external components (low background)
- Signal pre-amplification, channel multiplexing and waveform digitization with two data output streams
- DUNE variant of the ASIC front end has a similar front-end specifications to LArASIC.

SiPM board for testing CRYO ASIC







- PCB board is designed to connect multiple Hamamatsu VUV4 2x2 SiPMs to the readout.
- Capacitance of the SiPM is ~ 1.3 nF, a 3.3 nF capacitor is connected in parallel to simulate total capacitance of 4.6 nF
- Weak coupling capacitor is chosen to be 0.2 nF

Connecting SiPM to CRYO ASIC FEMB board

ASIC board
Power cable

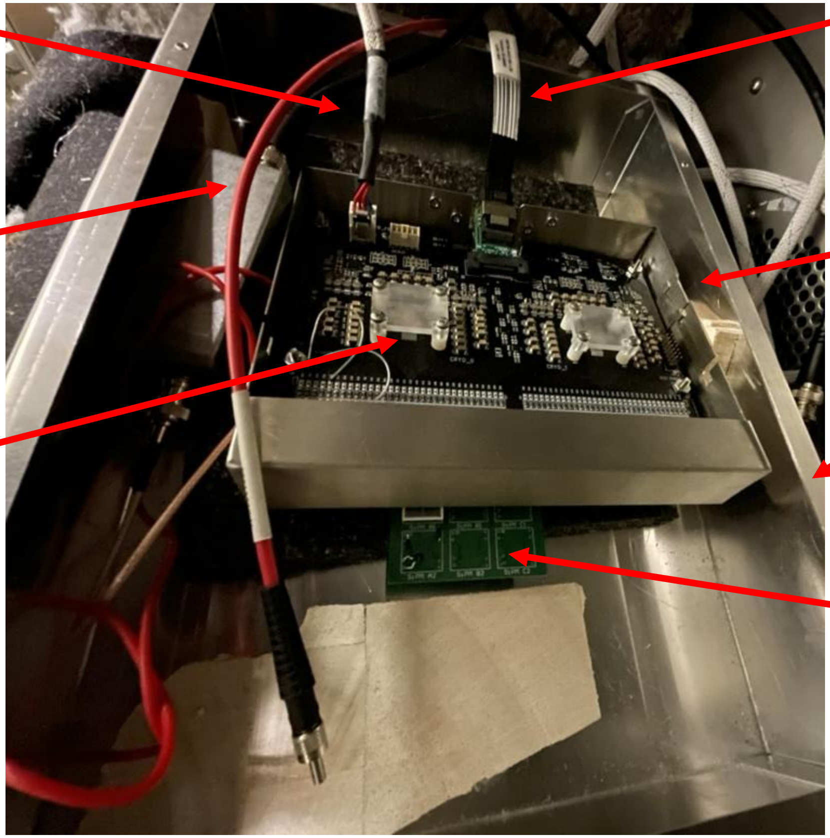
Data cable

LED fiber

Shielding boxes
(adding to reduce
noise)

FEMB ASIC board

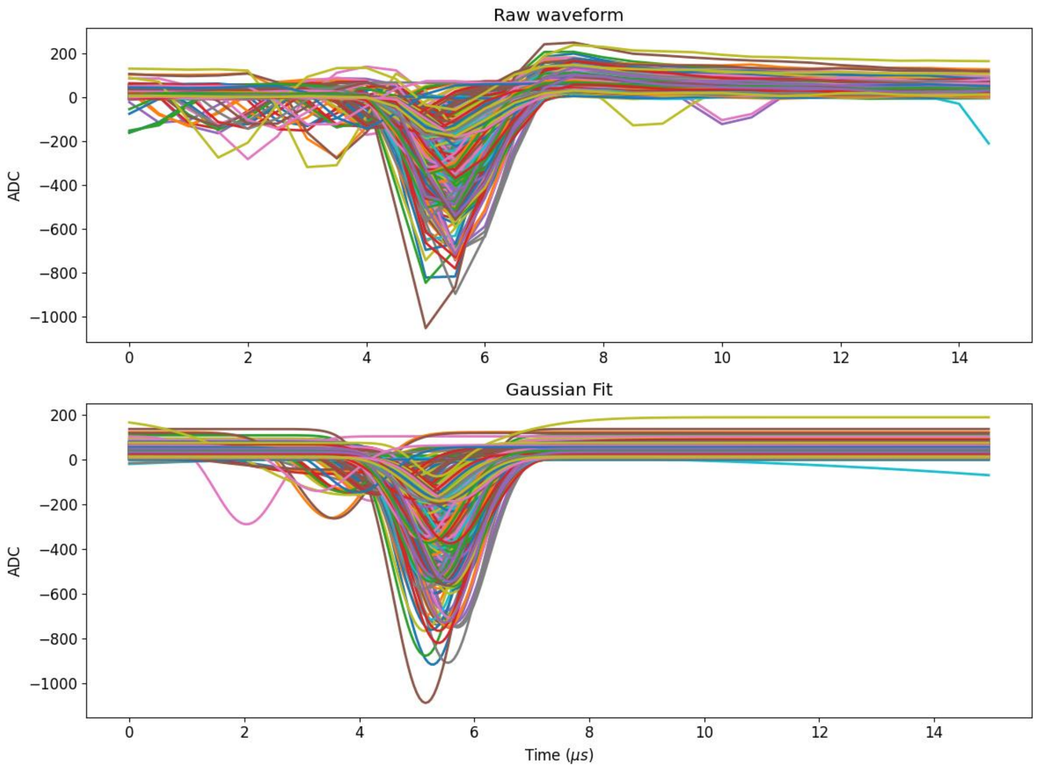
SiPM board



- CRYO ASIC FEMB board was used to read out the signal from the SiPM board
- The entire setup is installed in an environmental chamber, cooled down to LXe temperature of 160 K

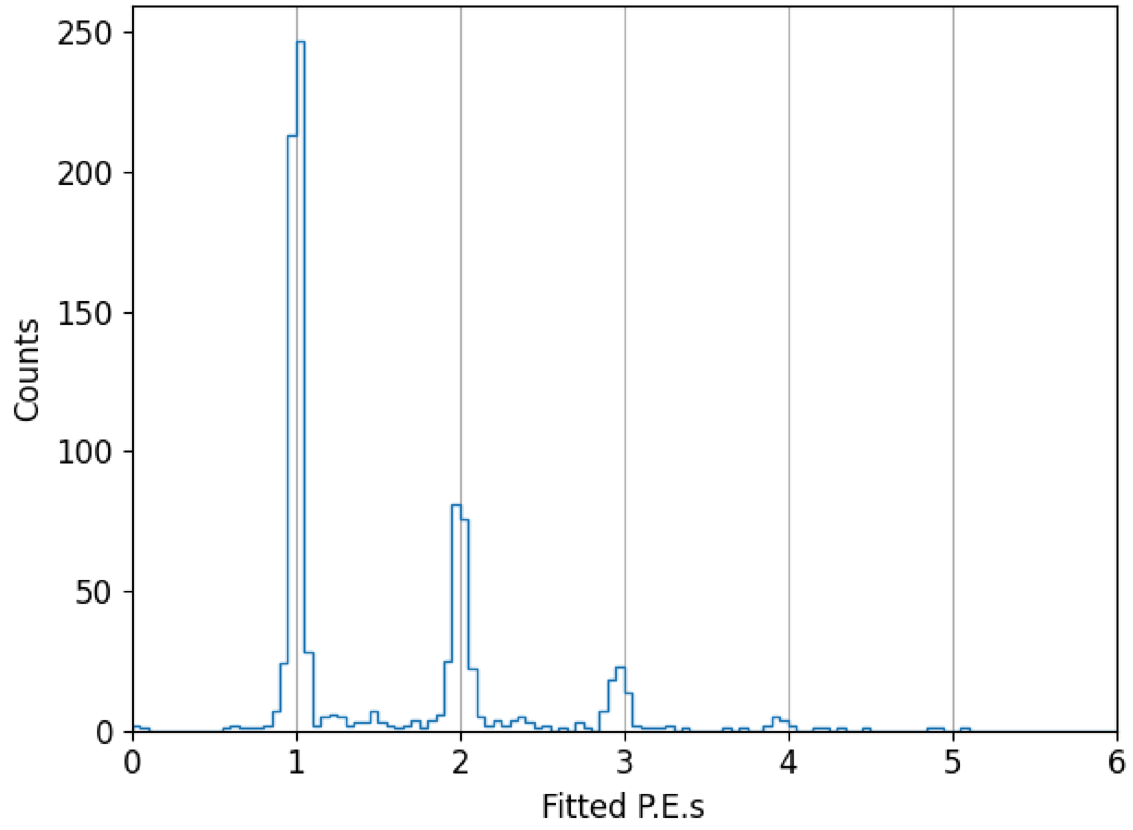
SiPM readout with CRYO ASIC at 160 K

- CRYO ASIC configured for 1.2 us peaking time, 4.8 mV/fC gain
- -50 V bias for SiPM, 0.2nF coupling capacitor,
- LED light injection, random trigger



- Light leakage leading to multiple peaks in a short time window in some events
- Gaussian fit used to reconstruct magnitude.

SiPM readout with CRYO ASIC at 160 K



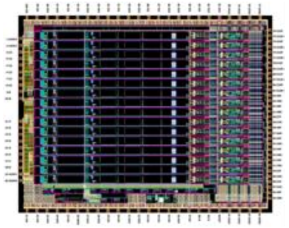
- Single p.e. magnitude ~200 ADC
- Noise level ~ 4 ADC (2100 e-)
- S/N ~ 50

Noticed ground connection affects the noise level. Further noise reduction may be possible with improved grounding schemes.

Summary

- Both LArASIC and CRYO ASIC can be used for SiPM readout using the weak coupling concept, achieving excellent S/N > 40 for ~ 6 cm^2 devices.
- LArASIC system has separate ADC chips and can be used optimized for a stave oriented waveform snippet design to minimize power consumption.
- CRYO ASIC system integrates the digitization and transmission in a single chip, more suited for a tile oriented design and where fully waveform streaming is preferred.

LArASIC



CRYO