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hls4ml - a tool for machine learning hardware-software co-design for HEP detector applications

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The tight integration of machine learning (ML) models into detector readout and trigger systems will allow future HEP detectors to move complex reconstruction tasks much closer to the detector compared to the current implementations. This will enable these detectors to cope with much higher data rates and perform more complex and better targeted event selection at trigger level. ML algorithms have to be designed from the beginning with the tight latency and computing resource constraints in mind, a process called co-design. This is often challenging and the integration of ML models into FPGAs or ASICs requires significant technical know-how. ML We present hls4ml, an open-source tool that translates ML models from standard tools like keras or pytorch into high level synthesis (HLS) code for integration into either FPGA or ASICs. hls4ml supports a large variety of common ML operations, recently adding support for transformer architectures. It generates HLS code targeting a variety of vendors, such as Xilinx/AMD, Intel/Altera, or Siemens EDA. Hardware-software co-design is enabled with native solutions, such as pruning techniques that specifically optimize the model for FPGA resource usage, or thanks to the tight integration of hls4ml into a wider eco-system of model pruning and quantization tools. These include established tools such as QKeras or QONNX, but also many advanced open-source tools that are developed by the HEP community. These include PQuant and HGQ2, support for which have recently been added to hsl4ml. hls4ml is already widely used in the HEP community to integrate ML models into existing trigger systems and its capabilities in accelerating ASIC design for detector readout has been demonstrated.

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