

# Novel High-Performance Single-Photon Detectors for Next Generation HEP Applications

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Assistant Professor

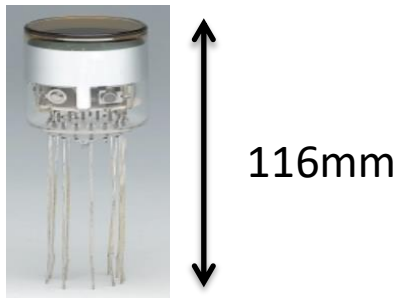
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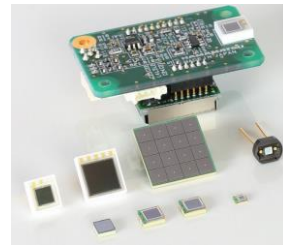


**CPAD 2025**

# Motivation: PMT vs SPAD & SiPM (Array of SPADs) <sup>2</sup>

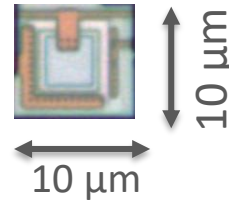


**Photomultiplier tube (PMT)**

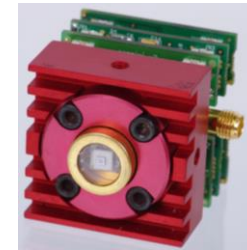


**Commercial**

**Single Photon Avalanche Diode (SPAD)**

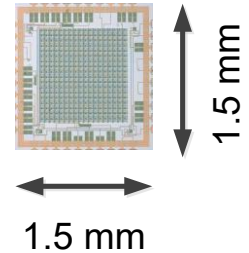


**CMOS**



**Commercial**

**Silicon Photomultiplier (SiPM)**

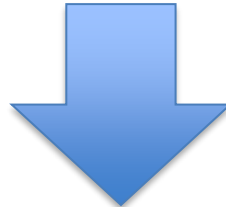


**CMOS**

|                             | <b>PMT</b> | <b>Commercial SPAD</b> | <b>CMOS SPAD</b> | <b>Commercial SiPM</b> | <b>CMOS SiPM</b> |
|-----------------------------|------------|------------------------|------------------|------------------------|------------------|
| Supply voltage              | 1250       | 58                     | 10-30            | 58                     | 10-30            |
| Sensitive to magnetic field | Yes        | No                     | No               | No                     | No               |
| Size                        | Bulky      | Less bulky             | Compact          | Less bulky             | Compact          |
| Gain                        | High       | Moderate               | Moderate         | Moderate               | Moderate         |
| Integrated Readout          | No         | -                      | -                | No                     | Yes              |
| Price (USD per pixel)       | 1500       | 100                    | 22-32            | 100                    | 22-32            |

# Motivation

- SiPMs tend to degrade in high irradiation environments rapidly
- Making them unsuitable for some collider experiments, particularly given the trend towards higher luminosities and therefore higher irradiation levels
- **One of the major challenges** of SiPM in such high-radiation environments is their **noise performance**
- CMOS detectors have been developed for precision position measurements in HEP due to their compactness and spatial granularity
- In recent years, developments have focused on sub-100 ps photon timing and direct particle detection



**Goal: Develop Ultra-Fast, Low Noise, Low Cost, and Scalable SiPMs for Next Generation HEP Applications**

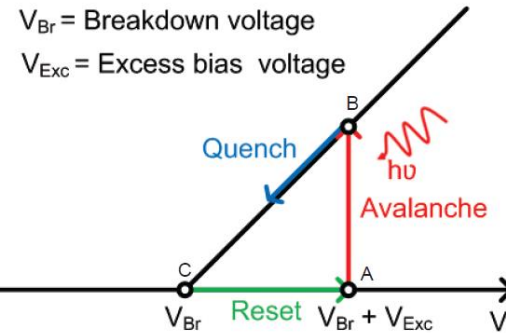
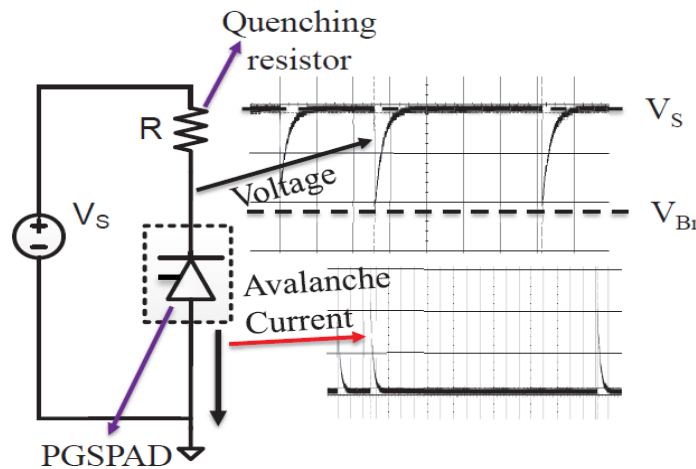
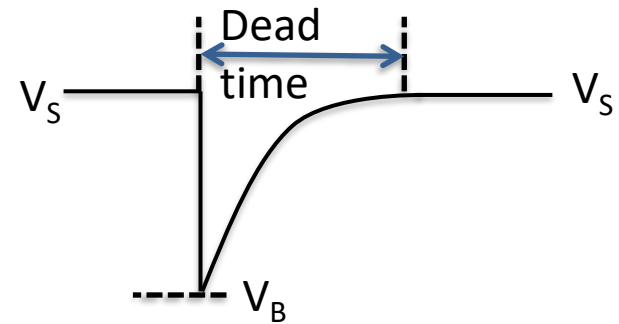
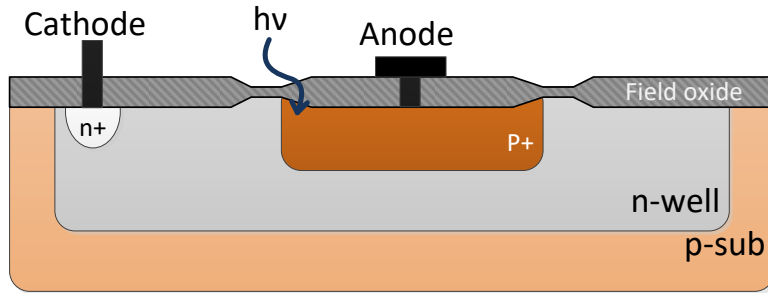
# Novel High Performance SPAD-based Single Photon Detectors for HEP

- New concepts at the Device and Circuit level design for improving the performance of SPAD detectors

## □ Technology:

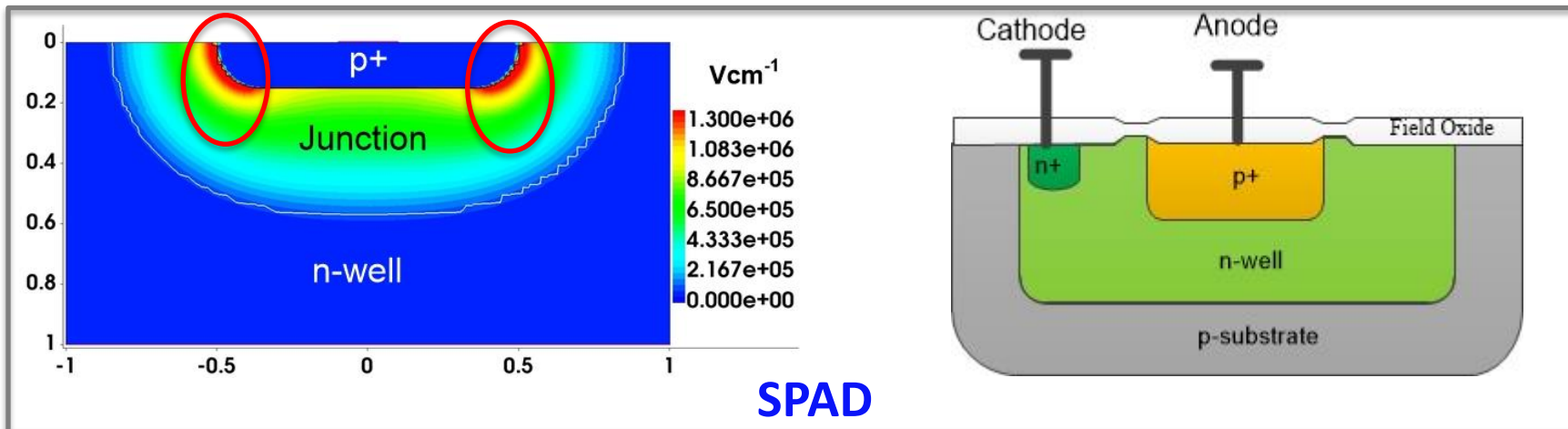
- **Device Level**: Incorporated surface field gates into SPAD devices within commercial CMOS processes to **improve noise**
- **Circuit Level**: New front-end readout circuits at pixel level, including mixed active and passive quenching and reset to **provide excellent timing resolution**

# Single Photon Avalanche Diode (SPAD)

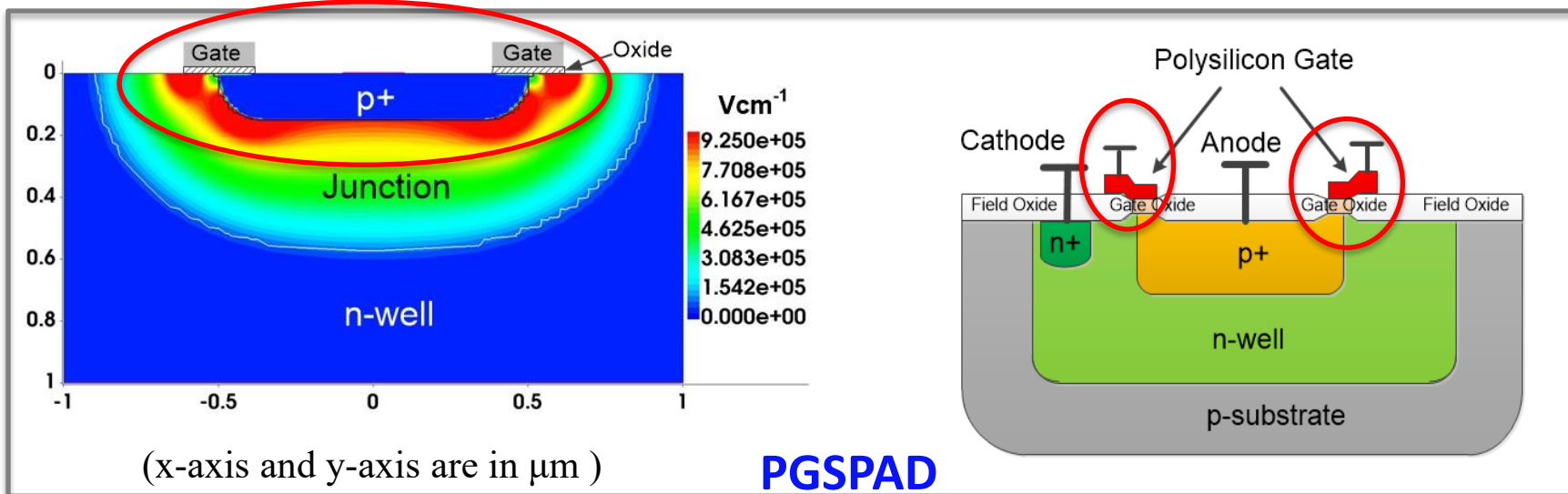


- SPAD is a p-n junction biased just above breakdown voltage
- Photon initiates impact ionization in depletion region
- After absorbing energy from the photon, free carrier drift with the electric field, causing ionization and triggering an avalanche
- Local current density increases rapidly until quenched
- Effective noise, DCR, -- Number of responses per unit time in complete darkness

# SPAD vs Perimeter Gated SPAD (PGSPAD)



**SPAD**



(x-axis and y-axis are in  $\mu\text{m}$ )

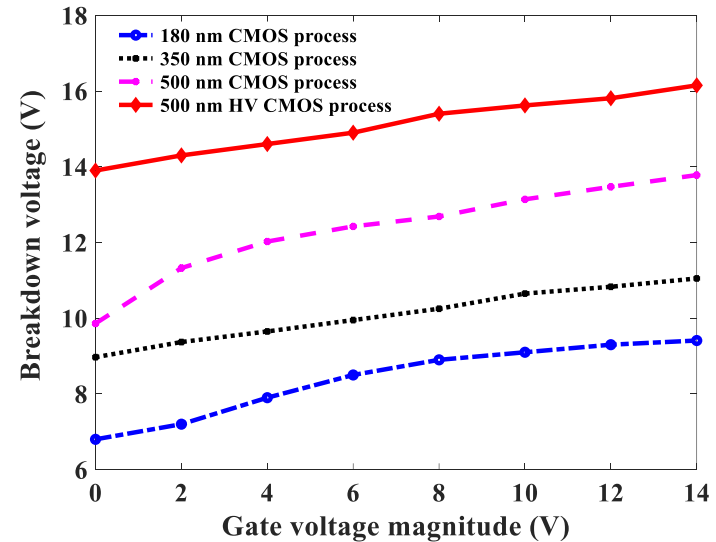
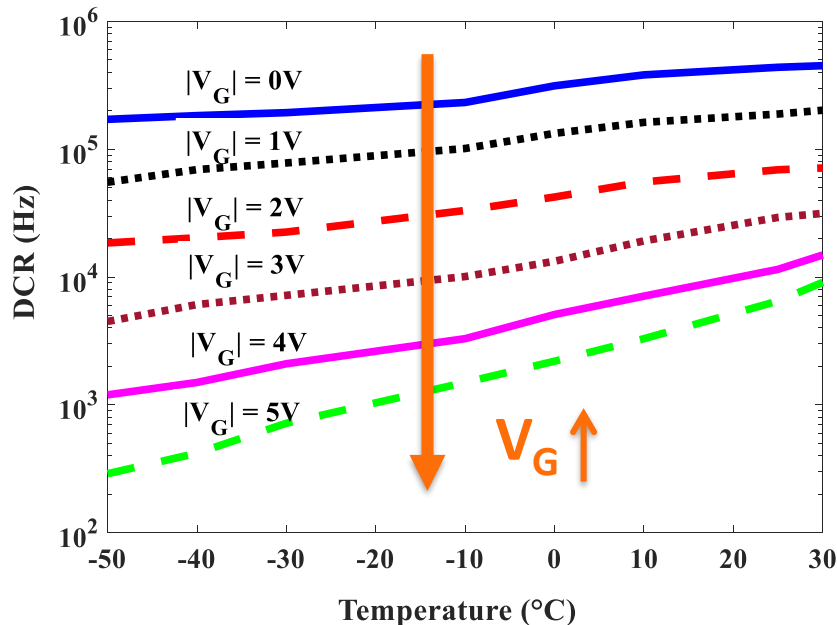
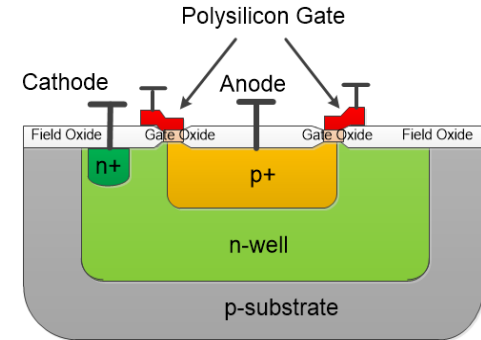
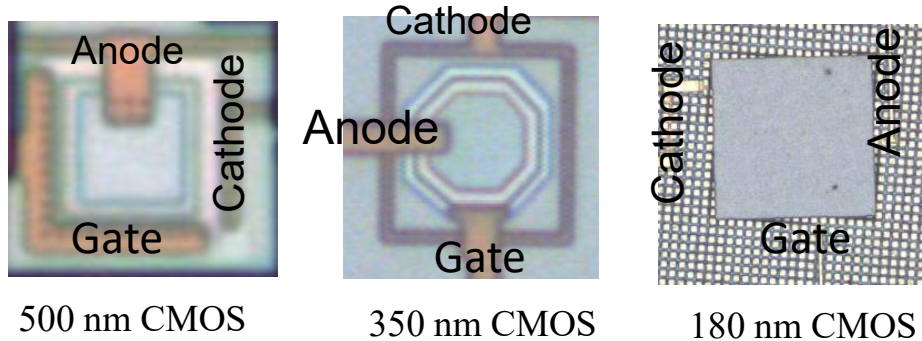
**PGSPAD**

- Electric field can be made uniform by applied gate bias of PGSPAD preventing Premature Edge Breakdown, a major problem of CMOS SPAD *Sajid et al., IEEE DCAS, 2024*
- Provide tunability of performance by applied gate bias *Shawkat et al., IEEE TCAS-I, 2020*

# Preliminary Works : Perimeter gated SPAD

## CMOS Perimeter Gated SPAD (PGSPAD)

- Design a Perimeter Gated SPAD
- First Noise Characterization through Experiment



- Applied gate voltage ( $V_G$ )  $\uparrow$   
Noise (Dark Count Rate, DCR)  $\downarrow$

Shawkat et al., IEEE Transactions on Circuits and Systems I (TCAS-I), 2018

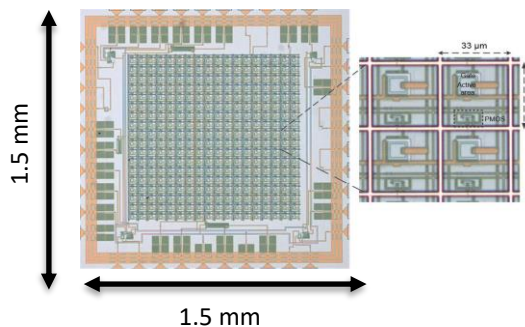
# Comparison

|                             | Custom SPAD<br>(Commercial<br>SPAD) | CMOS<br>SPAD | CMOS<br>Perimeter<br>Gated SPAD |
|-----------------------------|-------------------------------------|--------------|---------------------------------|
| Cost                        | \$\$\$                              | \$           | \$                              |
| Monolithic integration      | ✘                                   | ✓            | ✓                               |
| Noise (DCR)                 | Best                                | Worst        | Better                          |
| Breakdown variation control | ✘                                   | ✘            | ✓                               |
| Speed                       | Slow                                | Fast         | Fast                            |
| Dead space in array         | Higher                              | Lower        | Lower                           |

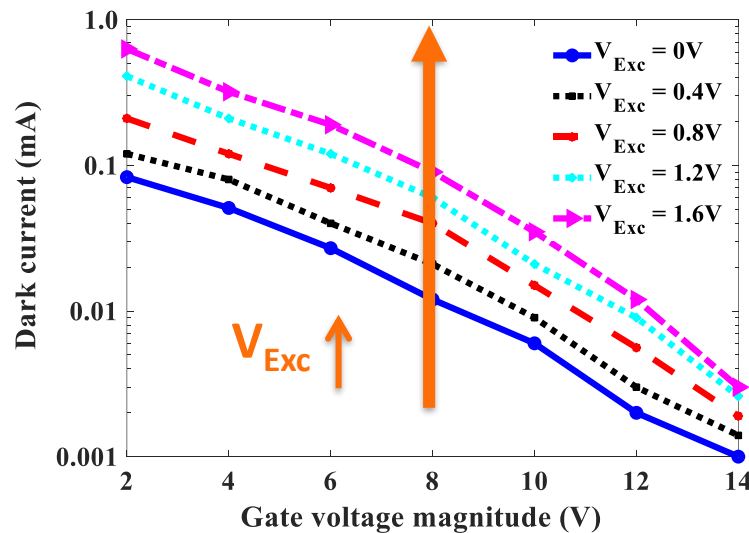
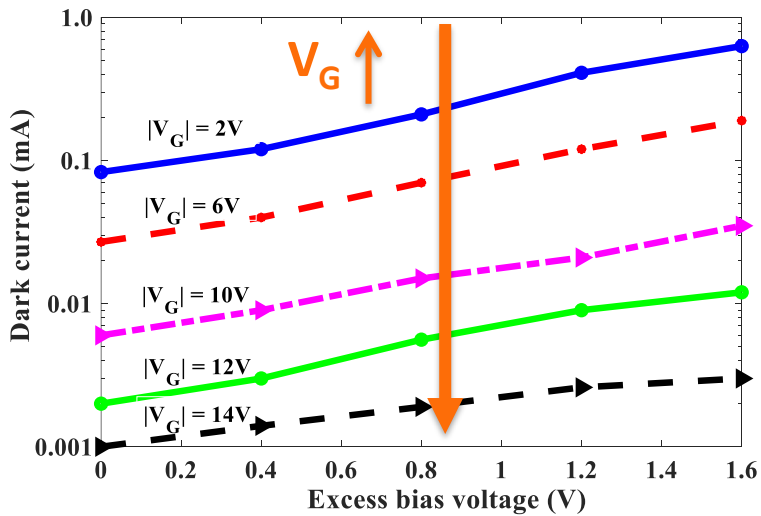
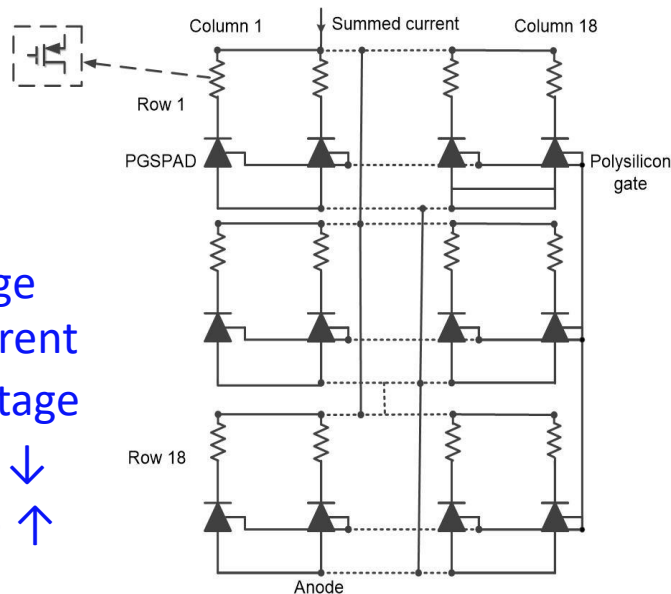
# Preliminary Works : Analog SiPM

## CMOS Analog SiPM using PGSPAD

- Design a New Compact CMOS Analog SiPM
- First Fully Characterized through Experiment (Electrical, Optical and Thermal)



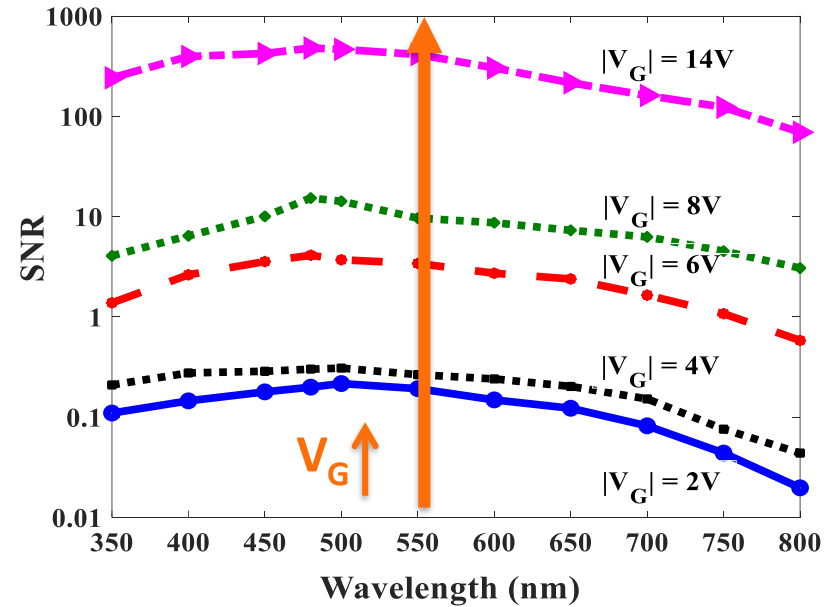
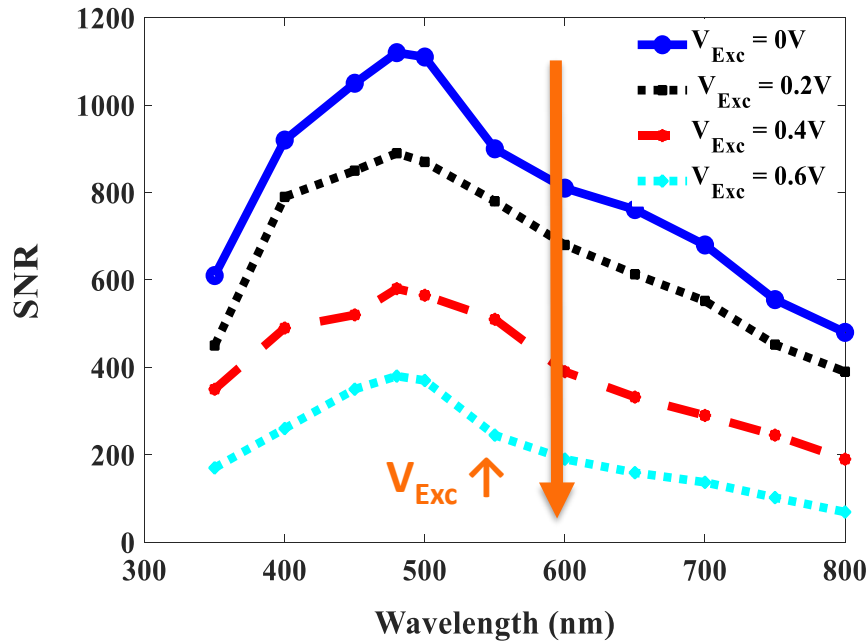
- $V_G$  - Gate voltage
- Noise - Dark current
- $V_{Exc}$  - Excess bias voltage
- $V_G \uparrow$  Noise  $\downarrow$
- $V_{Exc} \uparrow$  Noise  $\uparrow$



## Experimental Noise (Dark Current) Characterization

Shawkat et al., IEEE Transactions on Circuits and Systems I (TCAS-I), 2018

# Measured Optical Response



•  $V_{Exc} \uparrow$  Noise  $\uparrow$  SNR  $\downarrow$

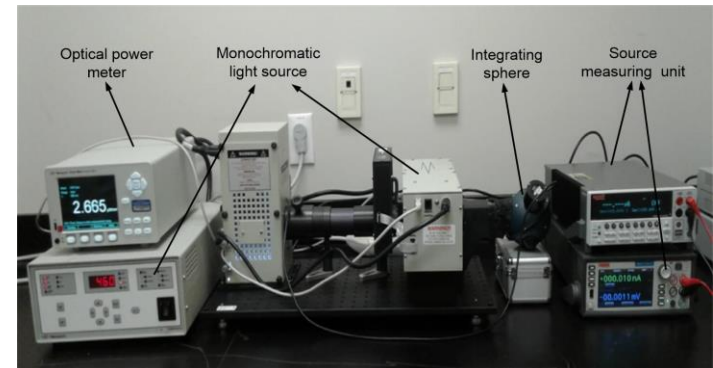
•  $V_G \uparrow$  Noise  $\downarrow$  SNR  $\uparrow$

$$SNR = \frac{\text{Measured current} - \text{Dark current}}{\text{Dark current}}$$

SNR – Signal-to-noise ratio

$V_{Exc}$  – Excess bias voltage

$V_G$  – Gate voltage

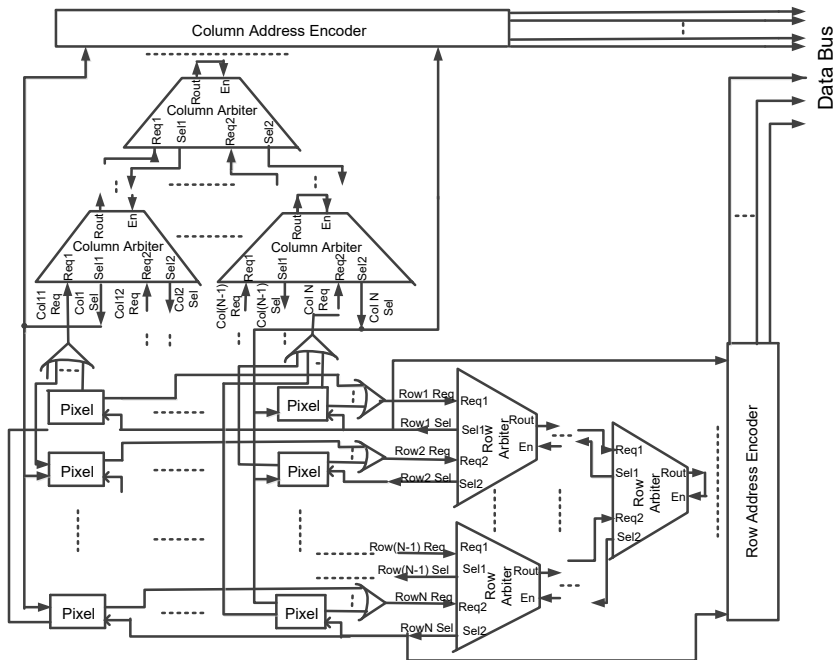


## ❑ CMOS Digital SiPM using PGSPAD

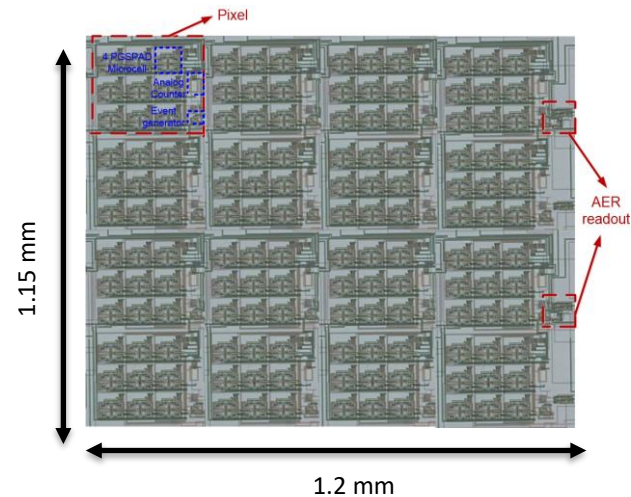
➤ Design a New Digital SiPM based on PGSPAD

➤ First Asynchronous Address Event Representation (AER) Readout for Digital SiPM

➤ Experimental Characterization (Electrical and Optical)



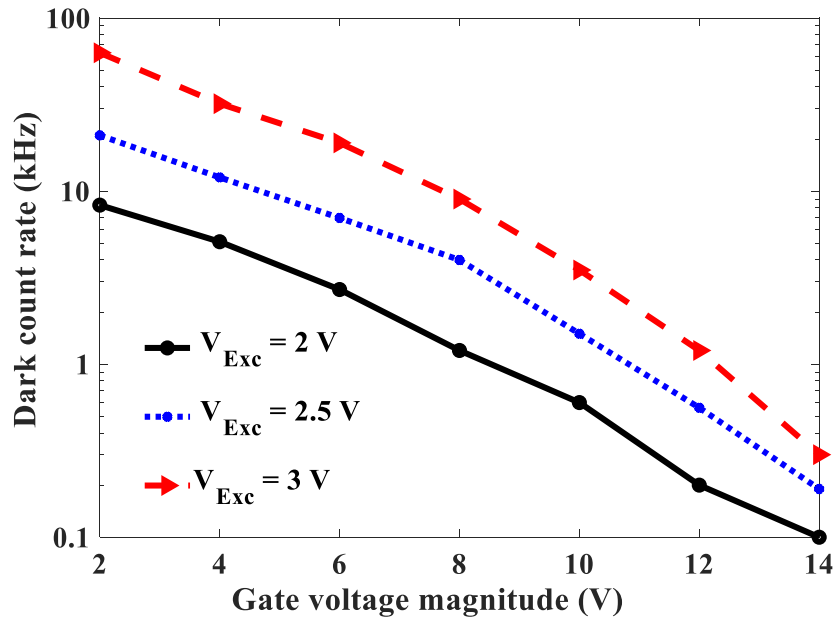
Digital SiPM with AER Readout



Photomicrograph of Fabricated Digital SiPM

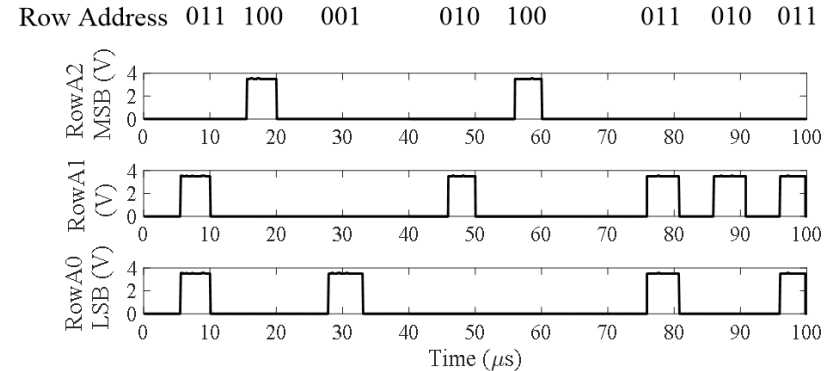
# Experiment Results

## Noise (Dark Count Rate) Characterization of Pixel of Digital SiPM

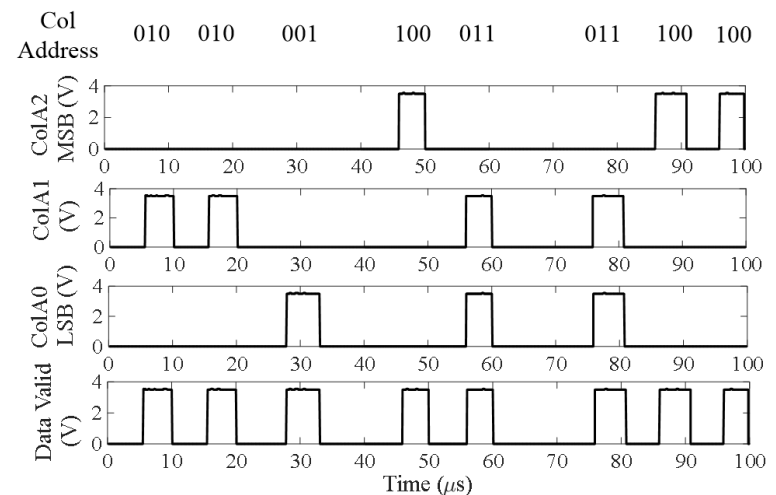


- Gate voltage ( $V_G$ )  $\uparrow$  Noise  $\downarrow$
- Excess Bias Voltage ( $V_{Exc}$ )  $\uparrow$  Noise  $\uparrow$

## Measured Response of $4 \times 4$ Digital SiPM with optical power of $100\text{ nWcm}^{-2}$



### Output Row Address

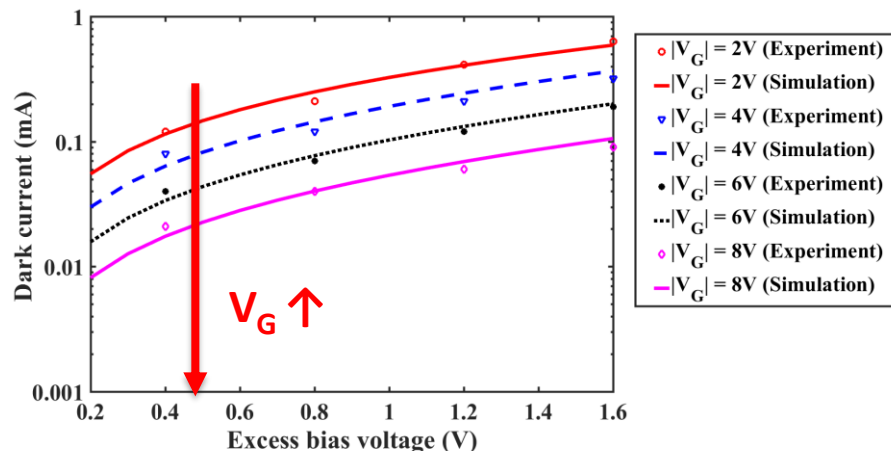
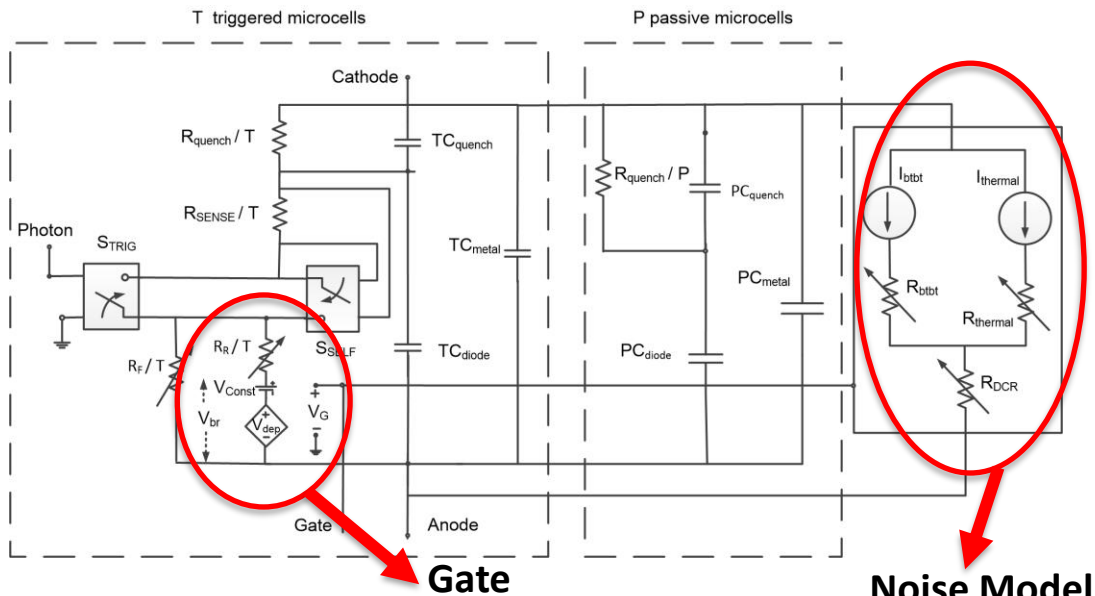
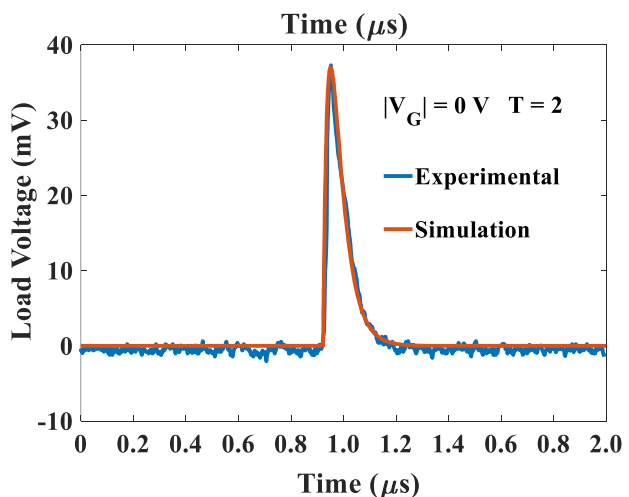
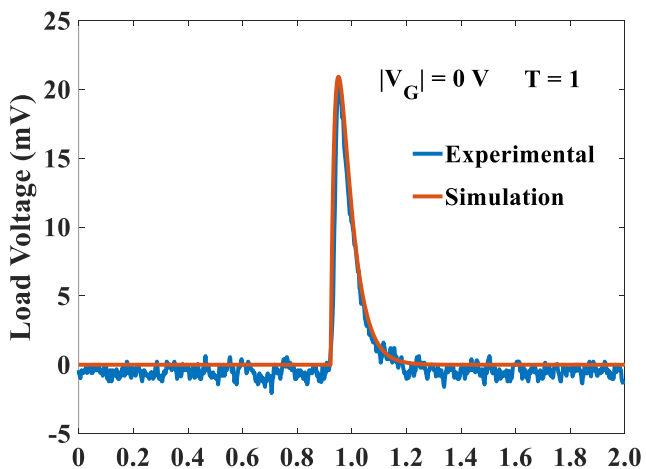


### Output Column Address

# Preliminary Works : SiPM Model

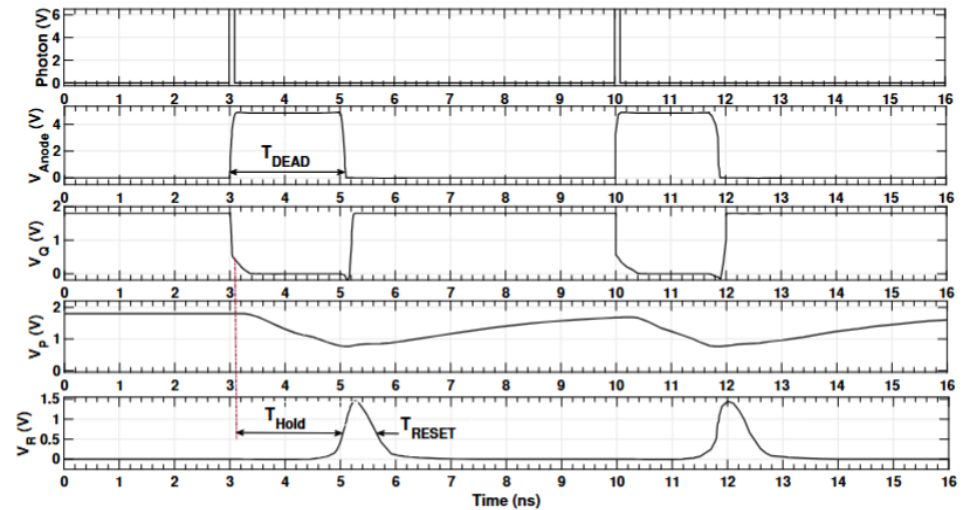
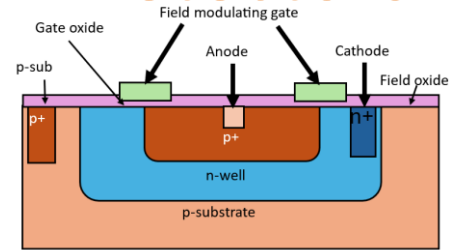
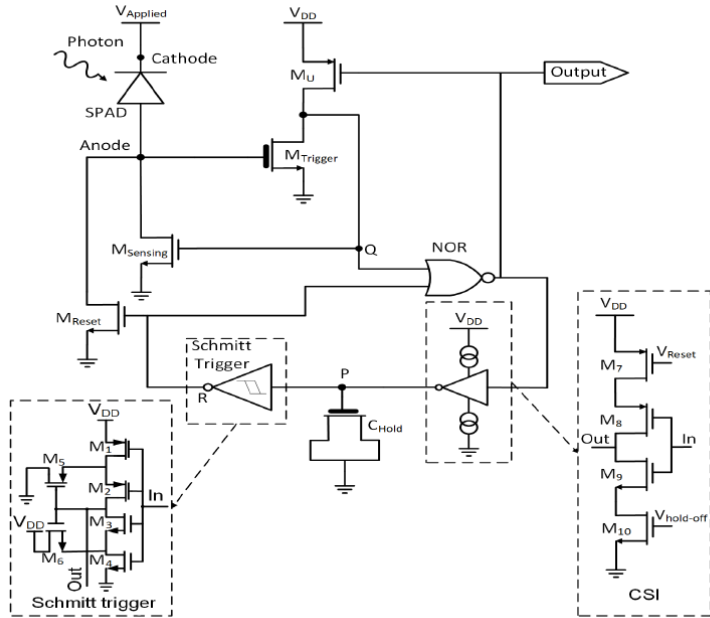
## Modeling of PGSPAD based SiPM

- Developed a Novel Comprehensive Model for SiPM based on PGSPAD
- First SiPM Noise model
- Validates with Experiments



Shawkat et al., IEEE Transactions on Nuclear Science (TNS), Feb. 2021

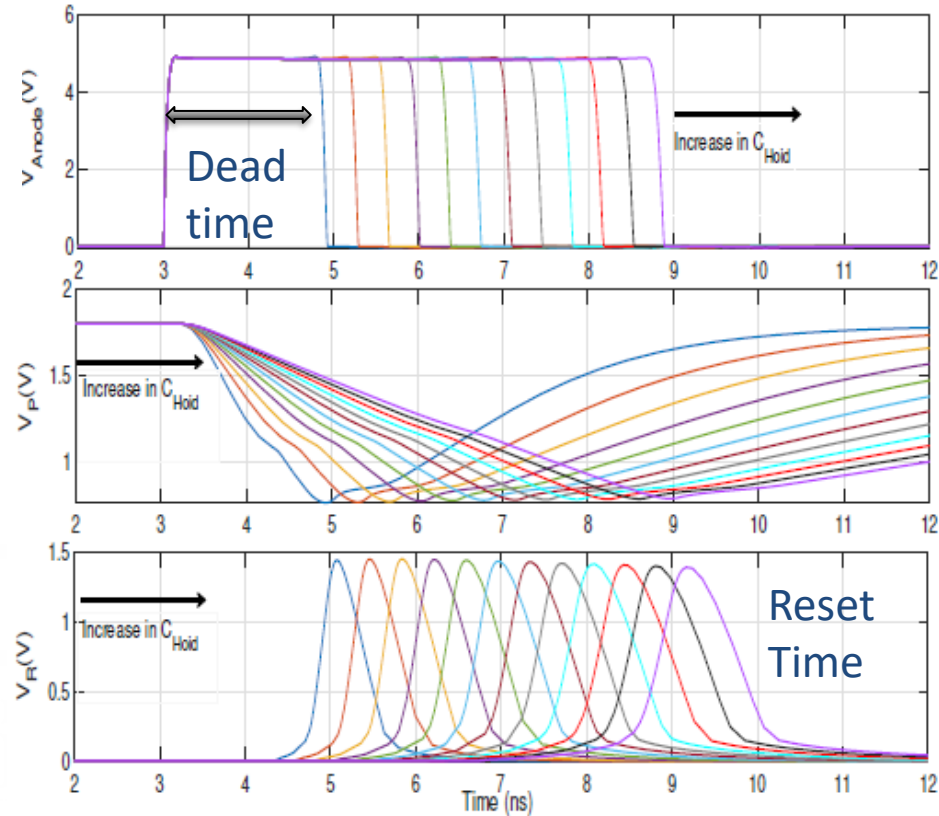
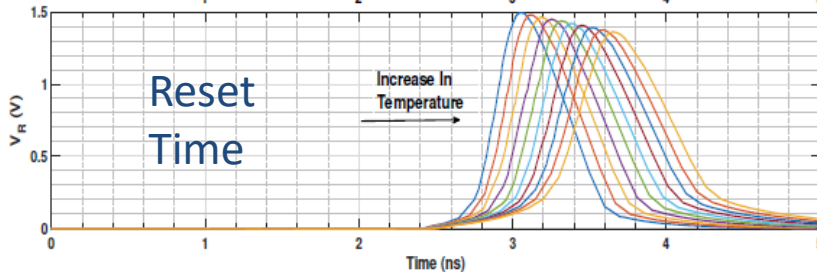
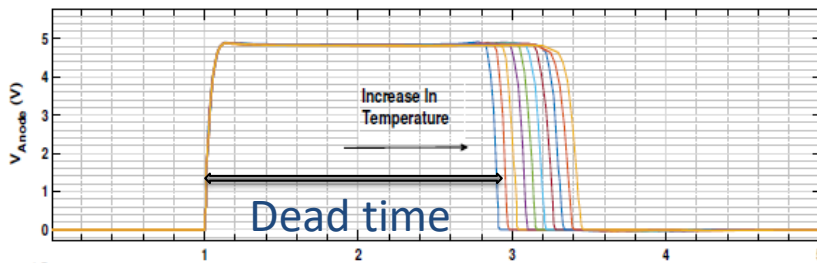
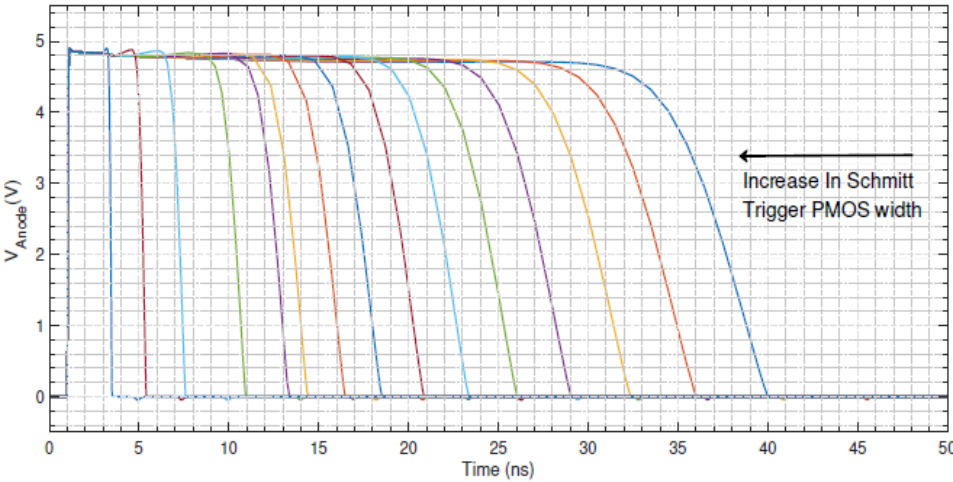
# Preliminary Works: Ultra-Fast, Low Noise SPAD-based Single Photon Detectors



- Improve noise performance and timing resolution of CMOS SPADs
- Incorporate surface field gate terminal into SPADs within commercial CMOS processes to reduce noise
- **New front-end readout circuits to quickly detect detector ignition and quench avalanche current, improving timing resolution**

N Irfan, K Daiyan, S Hasan, S. Hicks and **Shamim Ara Shawkat**. "A Tunable Dead Time, Low Noise, and Robust Front-End Circuit for CMOS SPADs" IEEE MWSCAS 2025

# Tuning Parameters to Improve Timing Resolution



Transistor Size (width)  $\uparrow$   $C_{Hold}$   $\downarrow$  Dead time  $\downarrow$  Timing Resolution  $\uparrow$

# Performance Comparison



| Ref.      | Process Tech (nm) | Dead time (ns) | Max Count Rate (Mcps) | Excess Voltage (V) |
|-----------|-------------------|----------------|-----------------------|--------------------|
| [18]      | 180               | 4              | 200                   | 3.5                |
| [19]      | 150               | 5              | 90                    | 10                 |
| [20]      | 65                | 3.35           | 300                   | 3.35               |
| [21]      | 350               | 7.86           | 127                   | 9.9                |
| [22]      | 180               | 3              | 300                   | 6                  |
| [23]      | 350               | 7.5            | 133                   | 16.5               |
| [24]      | 28                | 8              | 125                   | 0.5                |
| This Work | 180               | 2.12           | 526                   | 5                  |

Dead Time ↓

Timing Resolution ↑

Max Count Rate ↑

- Achieved a nominal deadtime of approximately 2.12 ns, resulting in a max count rate of 526 Mcps
- Provide dead time tuning capability over a wide range between 1.9 ns and 40ns
- Reduced dead time results in timing resolution improvement (30 pS)
- Potential for various applications, including HEP, which benefits from scalable single photon detectors with improved timing resolution and sensitivity

# Conclusions and Future Works

- A new class of SiPM detectors to provide an order-of-magnitude improvement in noise and timing resolution
- Introduce new concepts at the Device, Circuit levels to provide noise and timing resolutions far beyond what is currently available
- *At device level:* Incorporated surface field gates into SPAD devices within commercial CMOS processes to improve noise
- *At Circuit Level:* New front-end readout circuits at pixel level, including mixed active and passive quenching and reset to provide excellent timing resolution
- Suitable not only for next-generation HEP detectors but also in other applications such as long-term space missions

# Acknowledgment, Team Members, Sponsors and Collaborators

❑ **Acknowledgment:** This research is sponsored by the U.S. DoE, Office of Science, Office of HEP, Award Number DE-SC0024670

❑ **Team members:**

- Four Graduate (Ph.D.) Students
- Three Undergraduate Students

❑ **Collaborators:** UM, UC DAVIS



Brookhaven National Lab, EPFL, UF

UTK, Oak Ridge Lab, Stanford, UConn

❑ **Sponsors:**



Thank You

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