



Innovative **Back-Side Illuminated SiPMs**: first results from the **IBIS** project



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for IBIS project

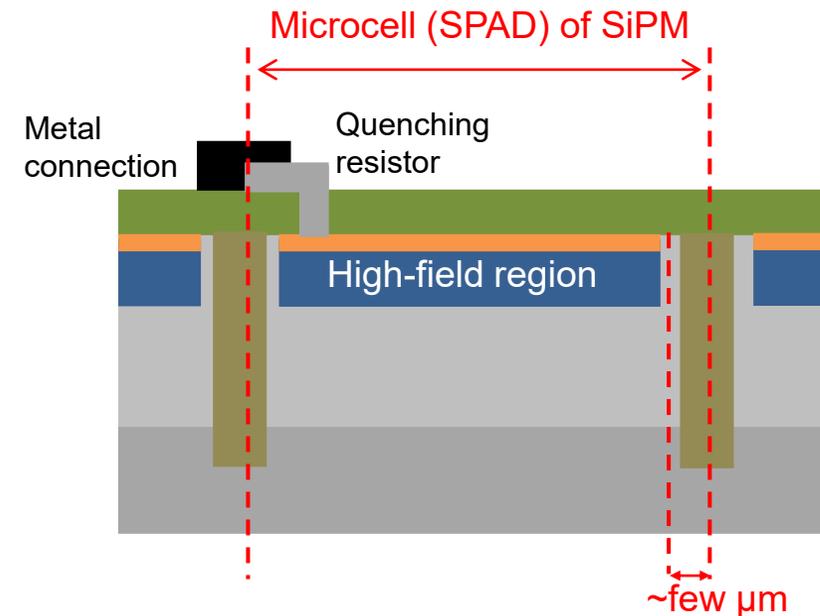
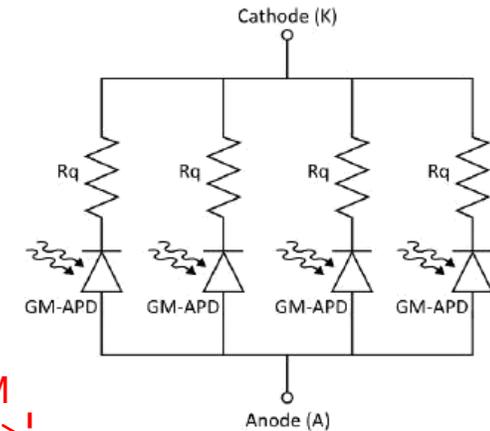
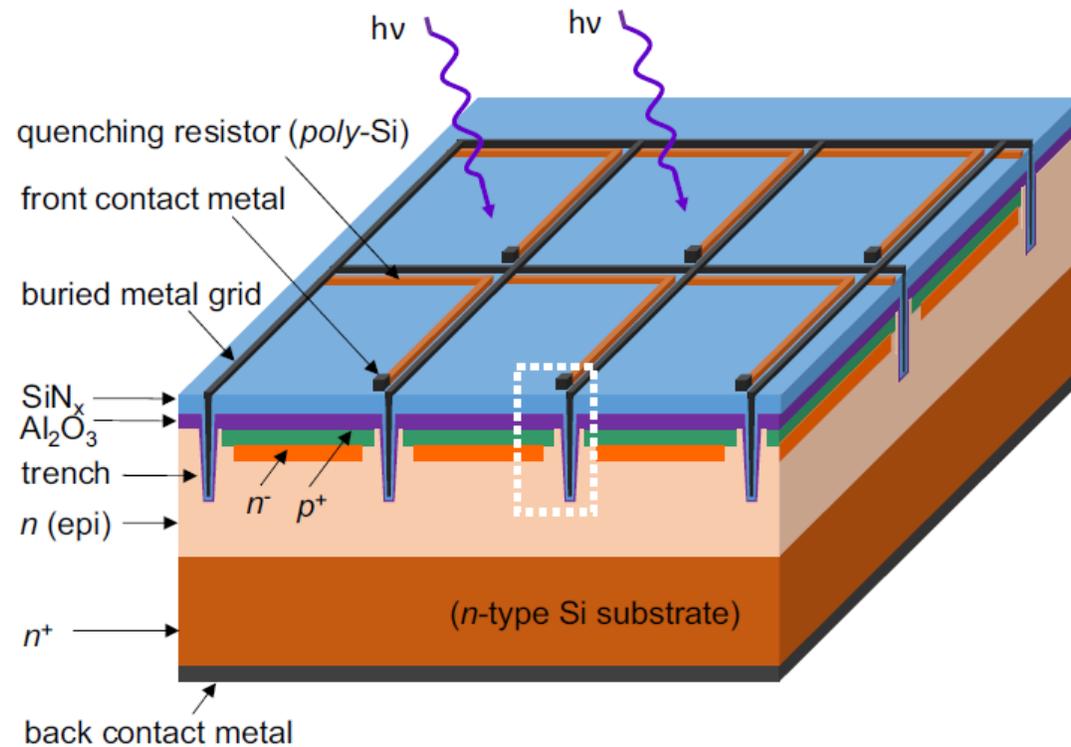
Coordinating Panel on Advanced Detectors

7 – 10 October 2025

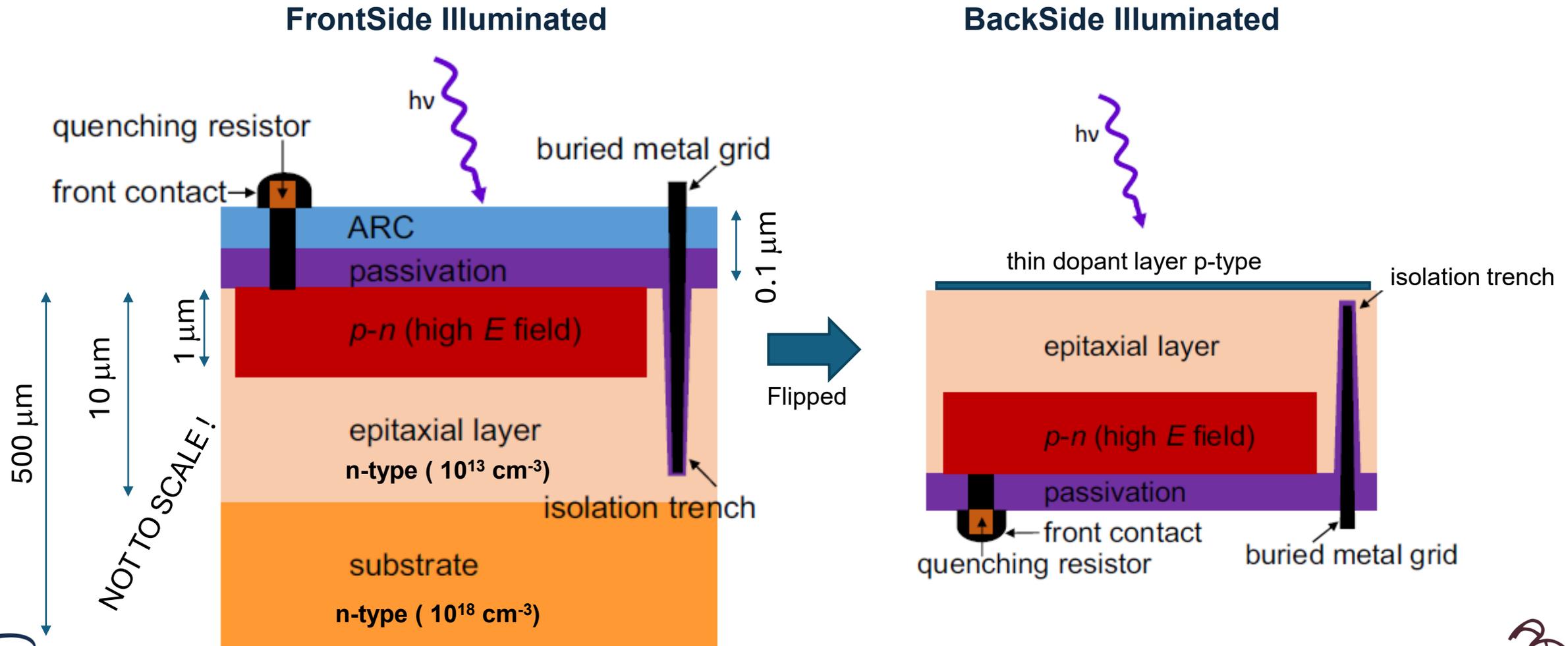
The standard SiPM

Array of Geiger-mode avalanche photodiodes (SPAD) connected in parallel on a common Silicon substrate:

→ analog signal «linearly» proportional to number of impinging photons



What is a Backside Illuminated SiPM?



BSI SiPMs

Advantages:

- Entrance window free of metal grid, quenching resistance, Through Silicon Vias
→ **Enhanced Fill Factor** (up to 100%)
Enables more advanced surface treatments to improve optical properties
- No need for Vias allows smaller SPAD size:
→ **High Dynamic range**
- Direct coupling of individual pixels (or small group of pixels) to readout chip by bump bonding
→ **Extremely high performance cameras**

Possible disadvantages:

- More difficult to control CrossTalk and AfterPulse



State of the art



Development of Back Illuminated SiPM at the MPI Semiconductor Laboratory

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Advanced Back-Illuminated Silicon Photomultipliers With Surrounding P+ Trench

Haifan Hu, Ying Wang^{ORCID}, Senior Member, IEEE, Penghao Liu, Xiubo Qin, Junpeng Fang, Hongming Zhao, Zhe Ma, and Jiatong Wei

31 January 2020

64x48 pixel backside illuminated SPAD detector array for LiDAR applications

Jennifer Ruskowski, Charles Thattil, Jan H. Drewes, Werner Brockherde

[Author Affiliations +](#)

www.nature.com/scientificreports

Journal of Microelectronics and Photonics XVII; 1128805 (2020)

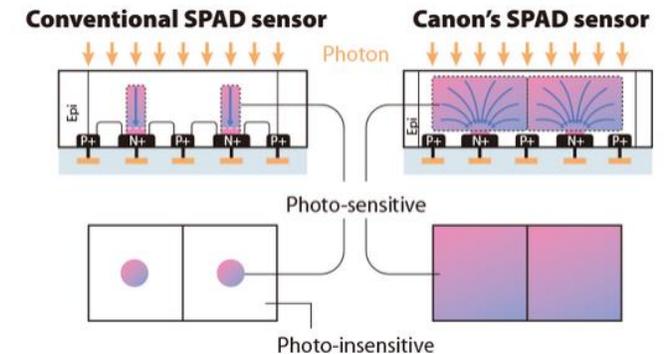
United States

scientific reports

OPEN Advanced antireflection for back-illuminated silicon photomultipliers to detect faint light

Yuguo Tao^{ORCID}, Arith Rajapakse & Anna Erickson

Nuclear and Radiological Engineering, Georgia Institute of Technology, Atlanta, GA, USA. [✉]email: yuguo.tao@gatech.edu



IBIS project

Backside Illumination

- Now a standard process in CMOS imaging, but still not used in SiPM

→ Main goal of the **I**nnovative **B**ackside **I**lluminated **S**ingle photon detector (**IBIS**) project is the production of **different devices** tailored **for several applications**

IBIS project (2020-today)

- Funded by Istituto Nazionale di Fisica Nucleare (**INFN**) and Fondazione Bruno Kessler (**FBK**)
- Originally (2019) main interest was on VUV sensitivity imaging of tracks in Liquid Argon detectors (DUNE Near Detector)
- Since also other experiments (**EIC**, **LHCb**, **ALICE3**) were interested in BSI, new runs has been funded by **INFN** with the purpose of **consolidate the base technology** and **optimize the efforts** to customize the technology for the various application (radiation hardness, VUV sensitivity, timing).



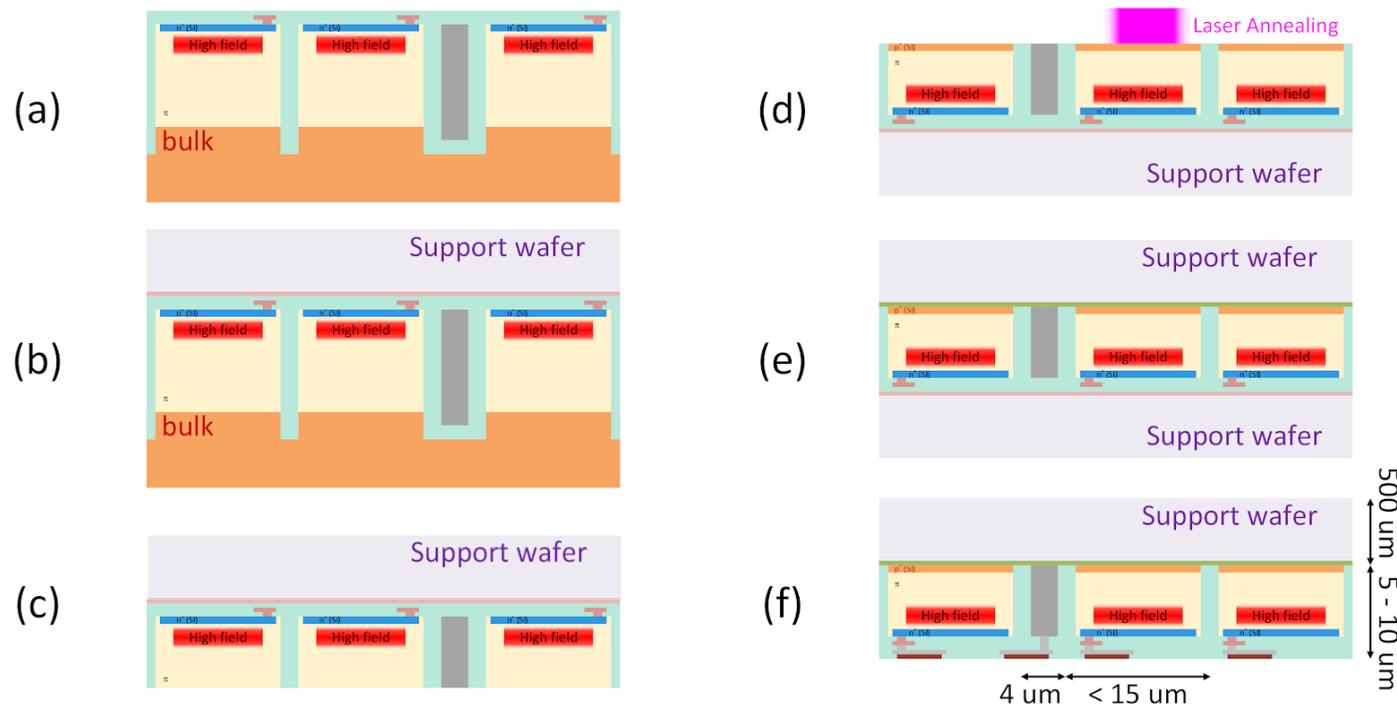
IBIS project

Goals:

- **Characterization** of the first prototypes samples of BSI SiPMs
- Test **Radiation tolerance**
- Test MIPs detection capability and **timing**
- Study Cherenkov application
- Study application to novel **imaging** technique to Liquid Argon detectors
 - Surface treatment to improve VUV sensitivity
- Design of a vertically integrated readout electronics (Read Out Chip bump bonded)
 - **INFN Torino** already has in hand an **ASIC** for SiPM readout with a matrix of 32 channels **ready for bump bonding**: mini-SiPMs backside illuminated with matched size (440 um) can be coupled with the existing ASIC with bump bonding...first step towards vertical integration



BSI Sensor Development at FBK



- a) **Build new cell**
- b) Attach Support Wafer on Front side
- c) **Remove completely Silicon bulk + Plasma doping on backside**
- d) **Laser annealing** on backside thin dopant
- e) Attach Support Wafer on Back side
- f) Remove Support wafer from Back side, from contacts



Features

Significant advantage of the BSI innovative cell design by FBK is the **clear separation between charge collection and multiplication regions** → **charge focusing**

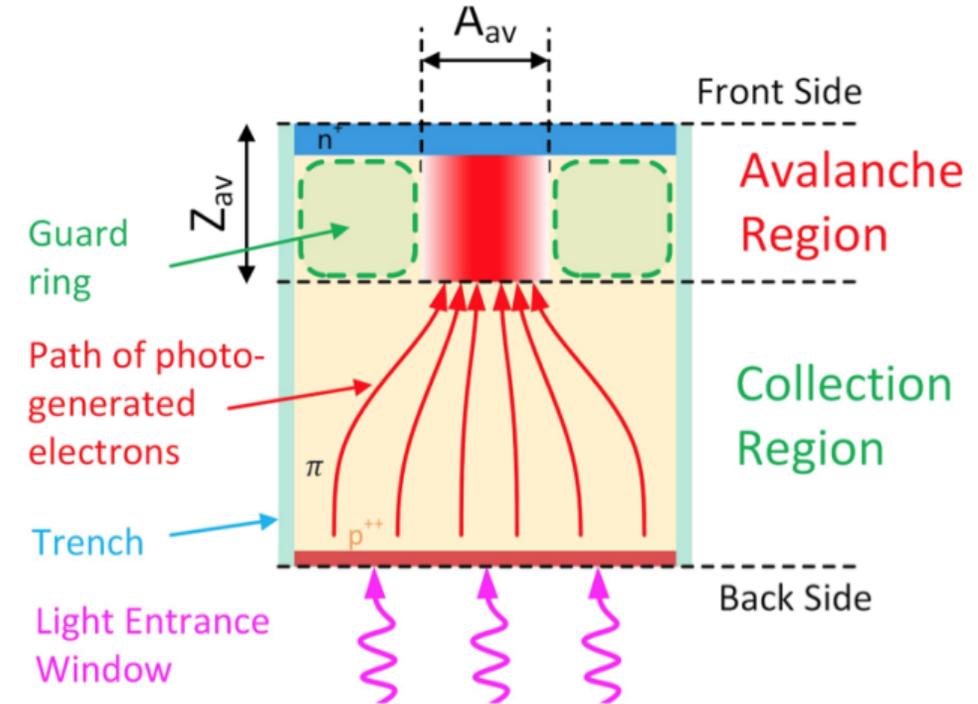
Better Radiation Tolerance:

Under the assumption that the main source of DCR is field-enhanced generation or tunnelling, radiation induced DCR is lower because the high field region is smaller
→ area sensitive to radiation damage is smaller than the light sensitive area

Possible drawbacks:

Timing performance may be degraded from difference in charge collection path length.

Lower gain leading to worse Single Photon Time Resolution (SPTR)



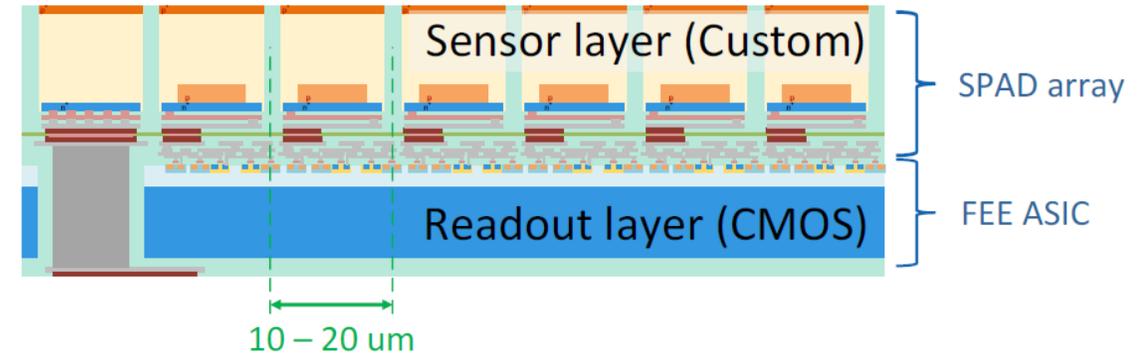
[S. Enoch et al 2021 JINST 16 P02019](#)



Features

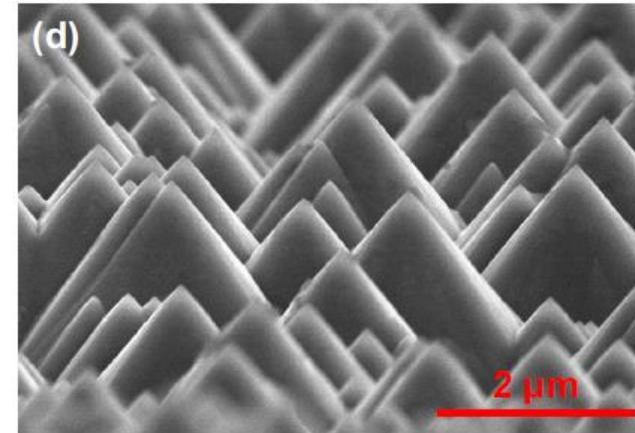
Direct Read Out Chip bonding:

- Enabling up to single SPAD access without TSV
→ Path towards imaging SiPM
- Local electronics → ultra fast and possibly low-power



Enhanced Sensitivity:

- No structures on the entrance window
→ maximal fill factor ($\sim 100\%$) even with small cells
→ Easier application of surface treatments for enhanced sensitivity in VUV



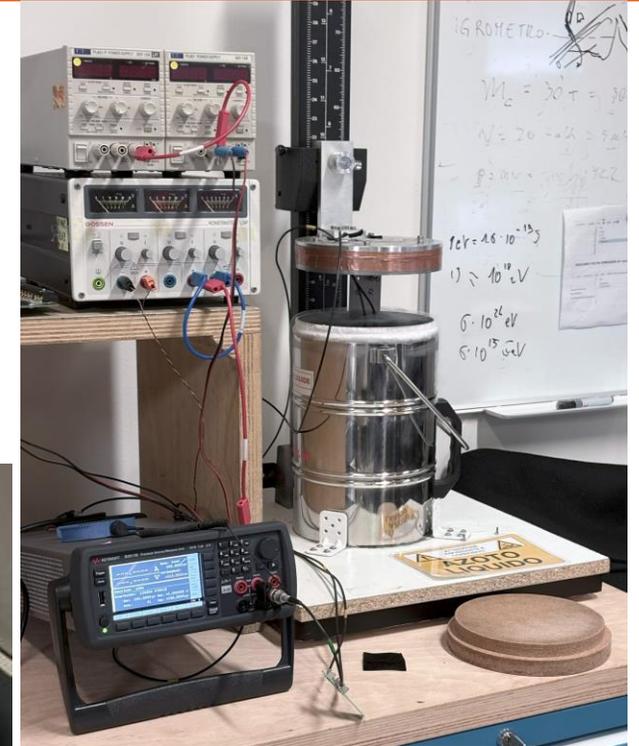
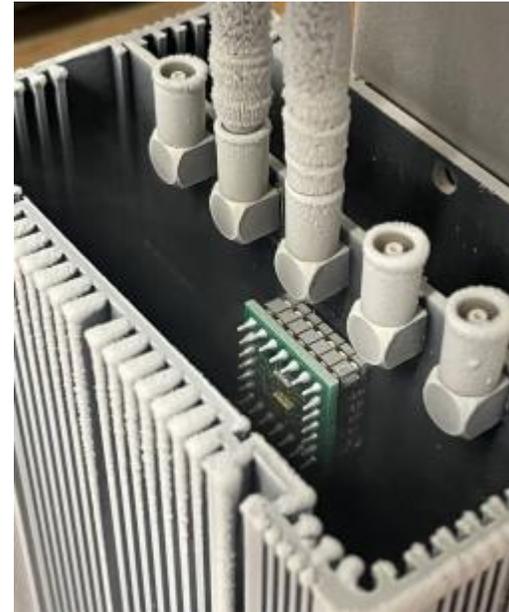
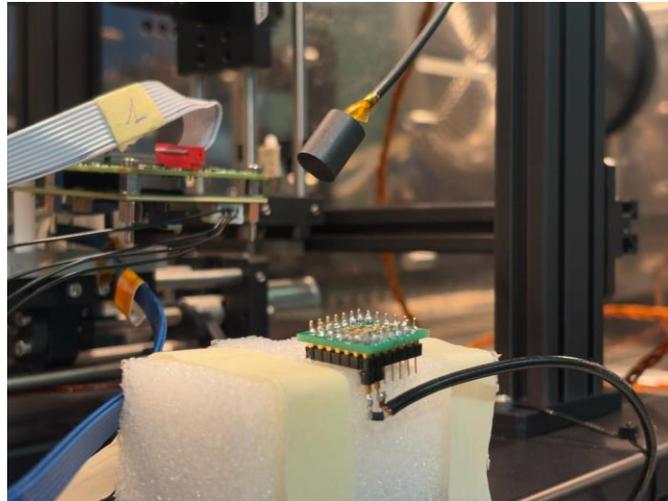
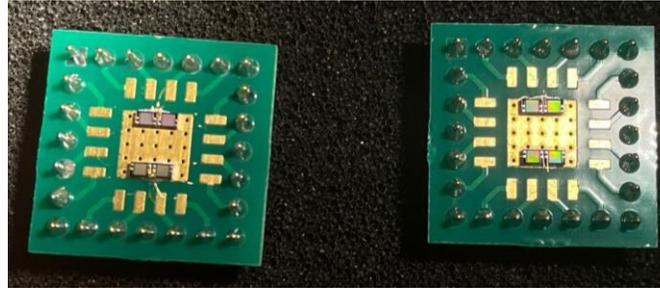
Tao, Y. Et al. *Sci Rep* **12**, 13906 (2022)



Test setups for I-V characteristics

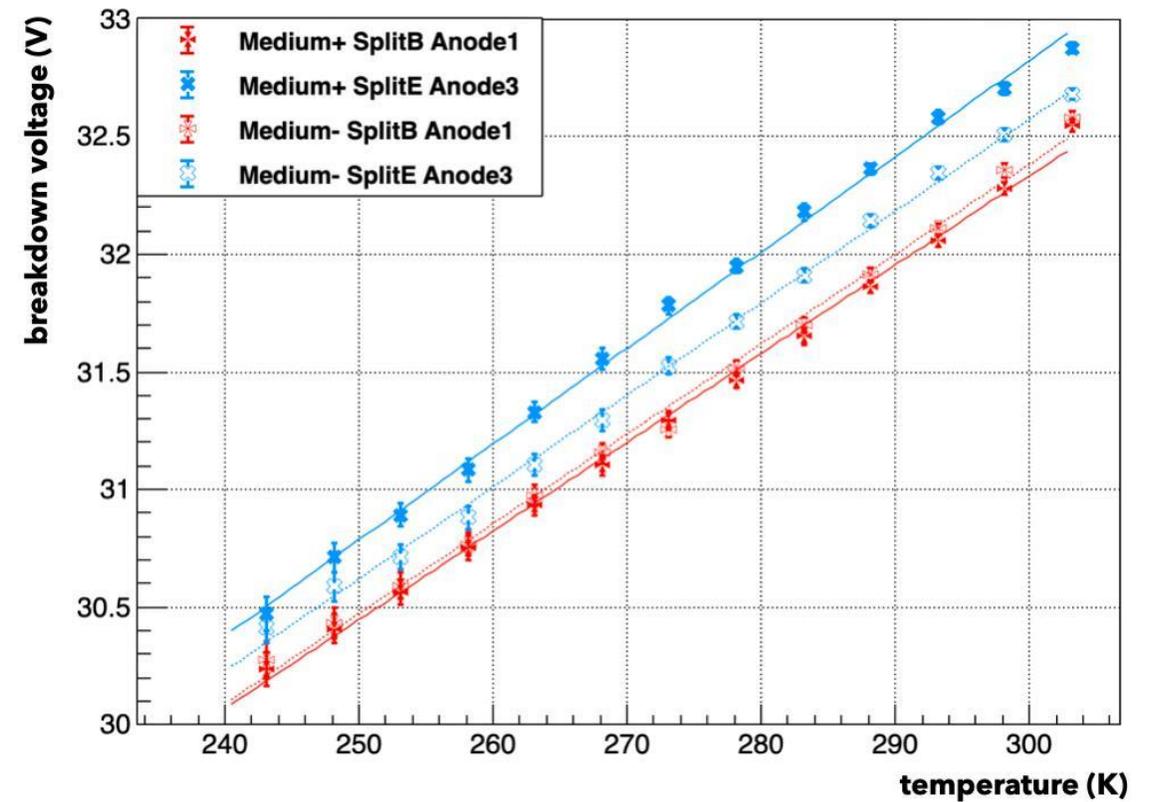
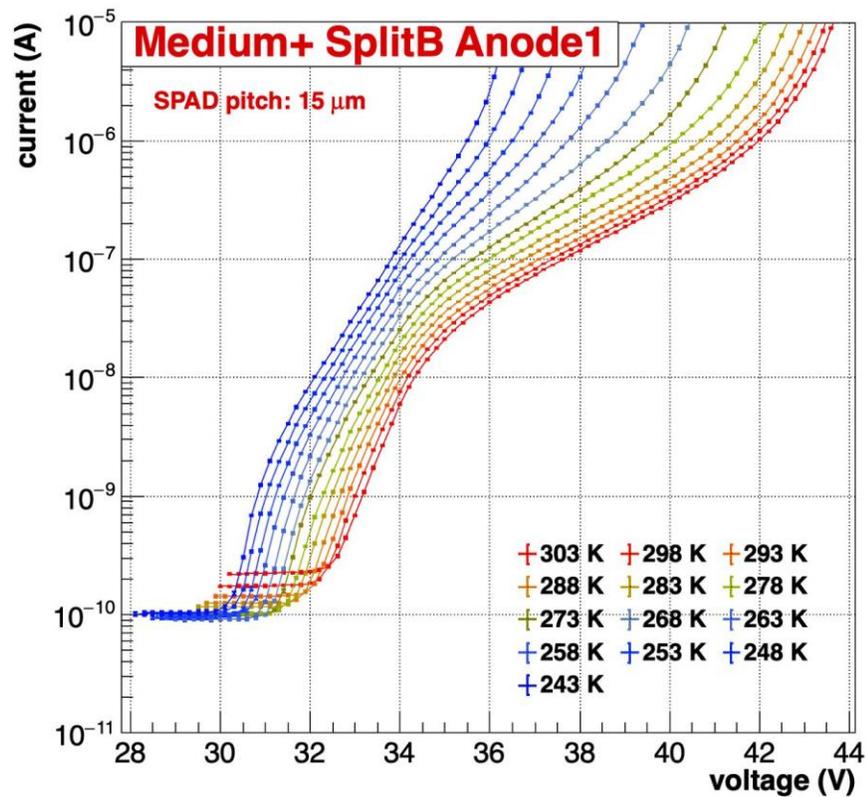
Setup used for the I-V measurements:

- **Source Measure Unit** to bias the SiPM
- **Black box** for light shielding
- **Climatic chamber**
- 6 lt dewar for **Liquid Nitrogen** (77 K) measurements



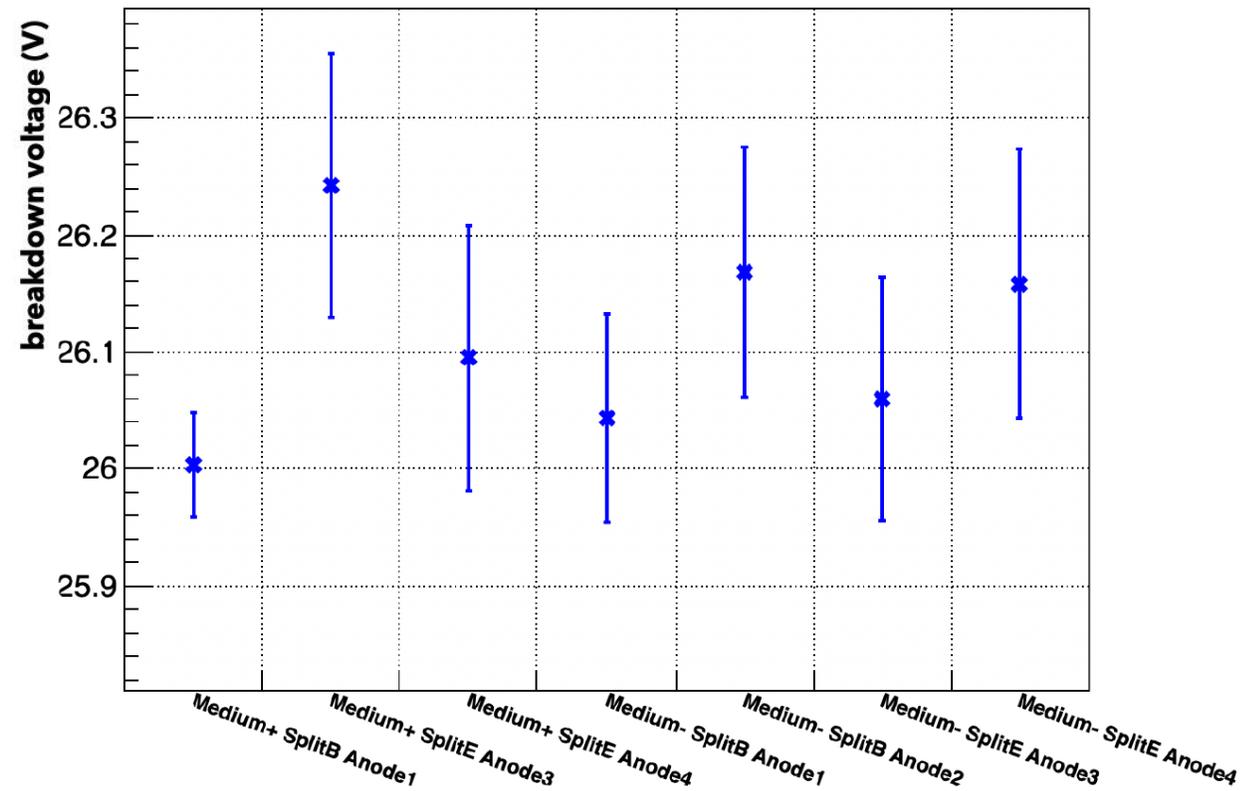
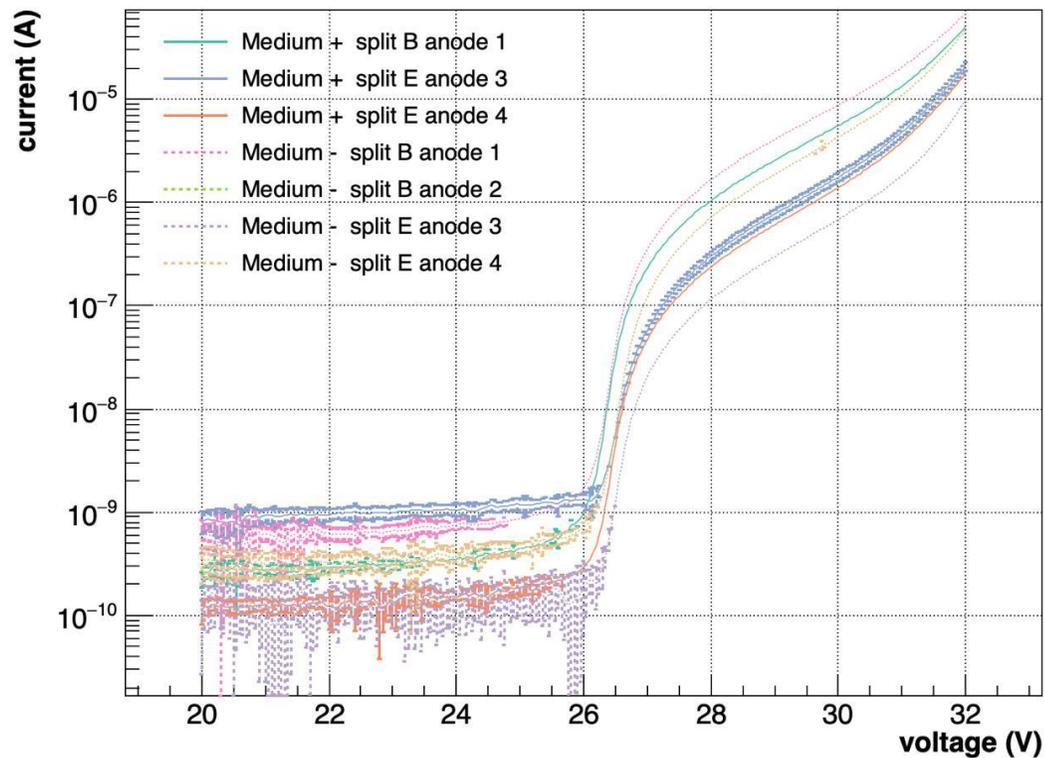
I-V curves

- Measurements in climatic chamber → Determine breakdown voltage (V_{bd}) for different temperature



I-V curves

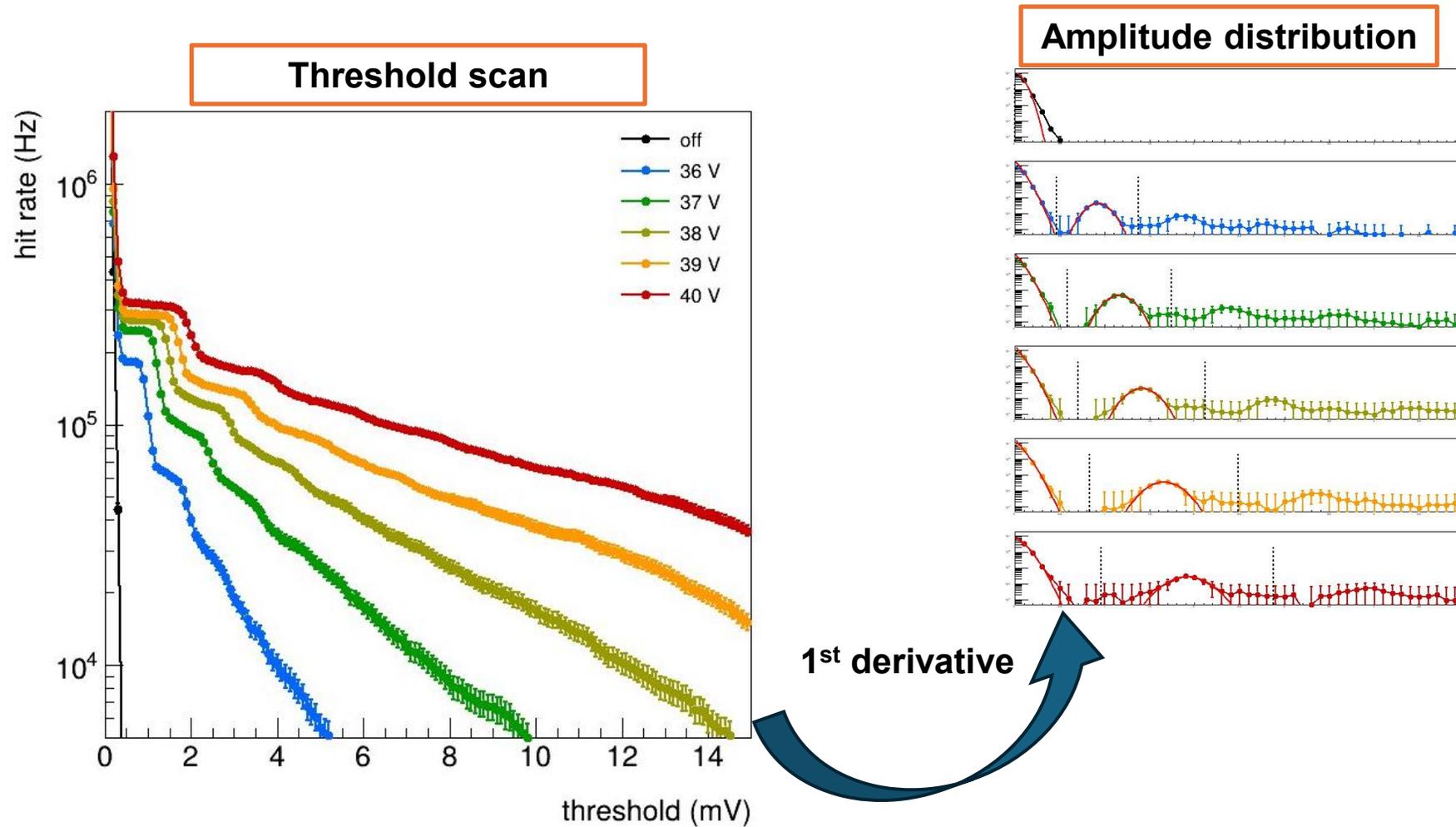
- Measurements in Liquid Nitrogen: Determine breakdown voltage (V_{bd}) at cryogenic temperature (77 K)



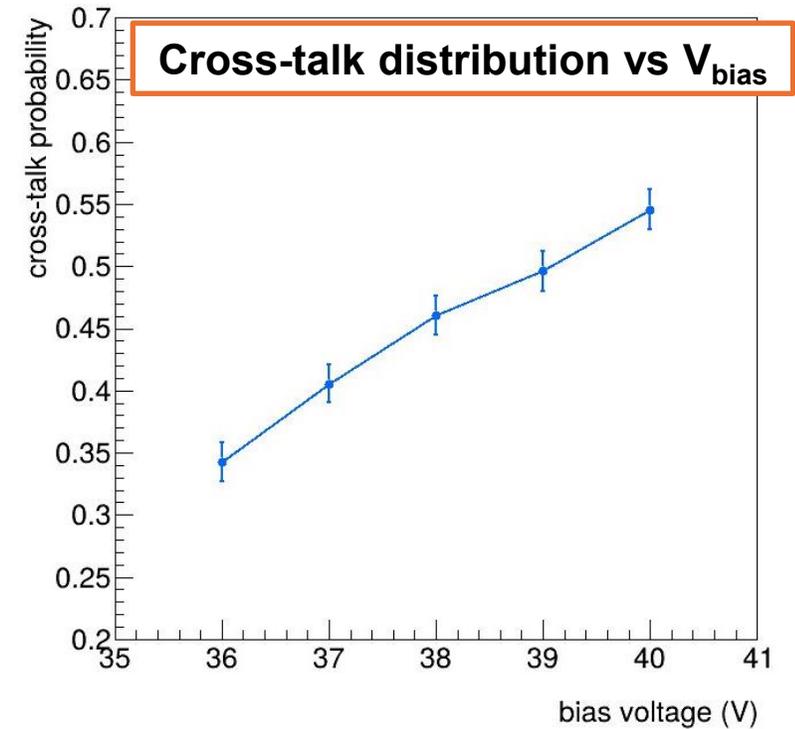
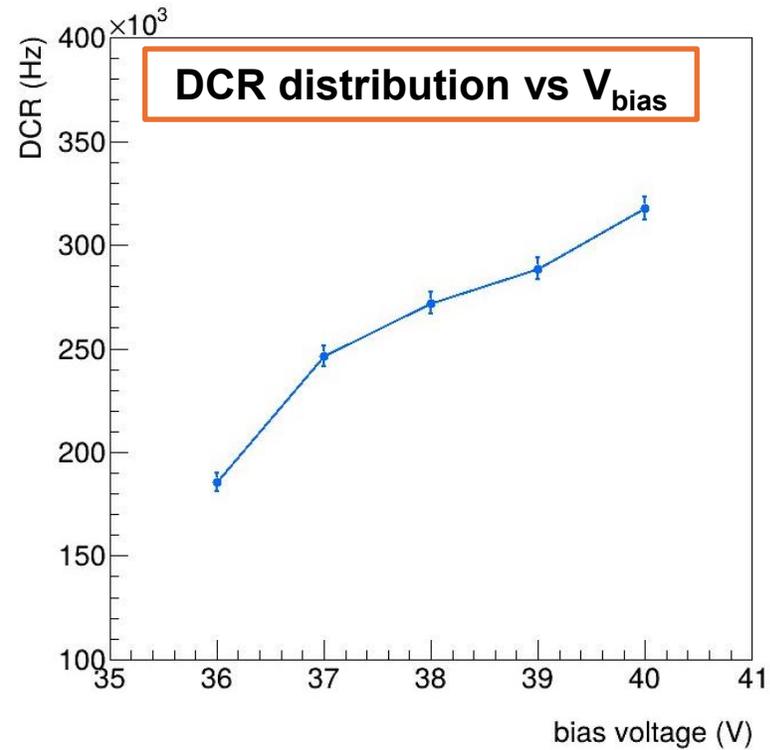
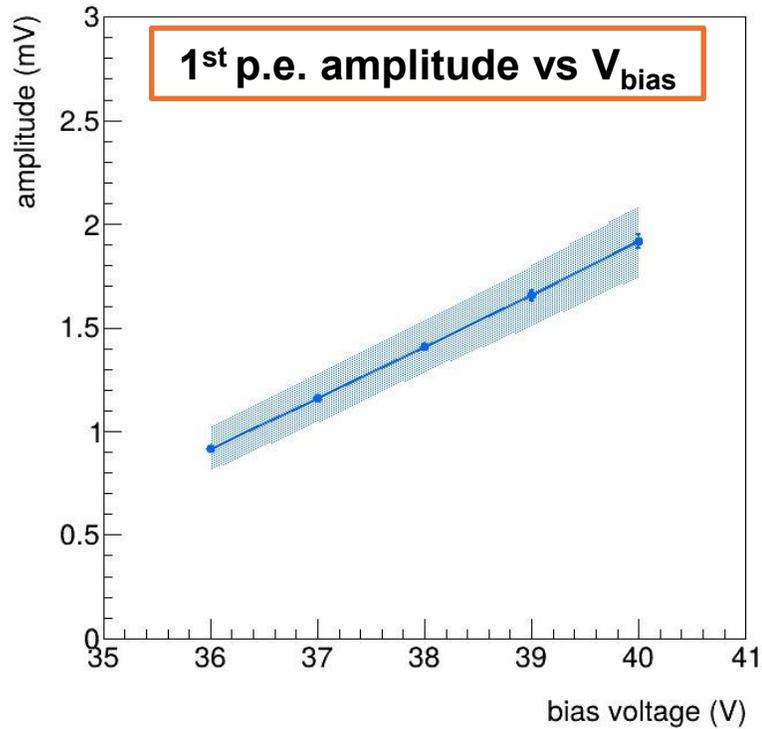
First setup for DCR measurements in Bologna



Results from DCR measurements



Results from DCR measurements



Conclusions and outlook

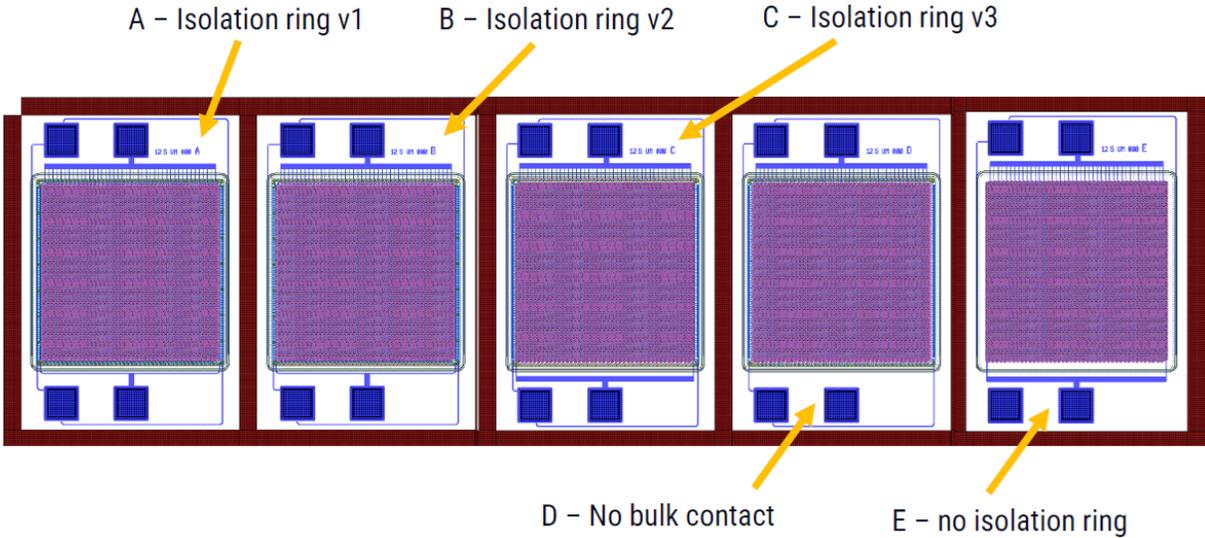
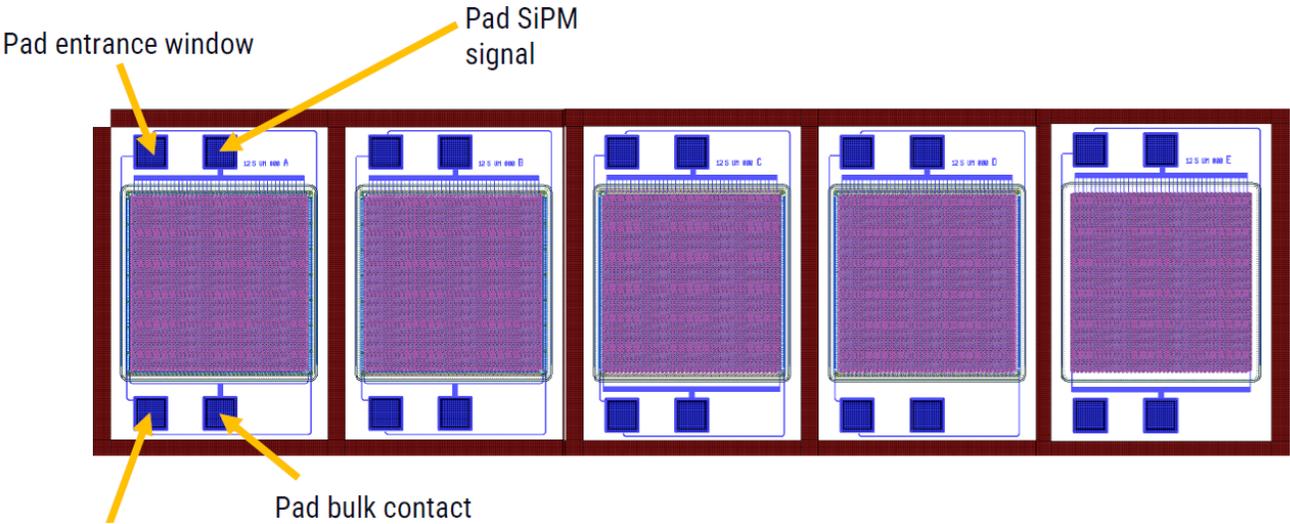
- Comprehensive set of measurements done on partially processed BSI
 - new cell is **working**
 - in future runs some strategy to reduce **CT** will be investigated
- First samples **fully processed BSI ready to be diced** after wafer level measurements will be soon available to Bologna for detailed characterization
- A **new run** is co-founded by IBIS project and scheduled for end 2025/begin 2026 It will profit from experience gained since today
- So far interest from **DUNE** for VUV, **EIC**, **LHCb** and **ALICE3** for radiation hardness and timing



Back up



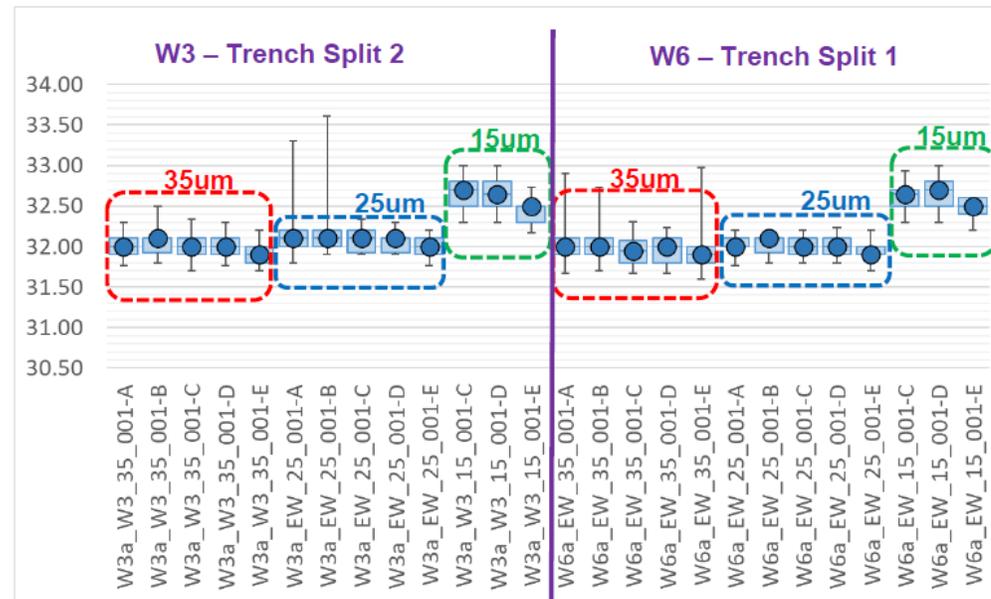
Sample testing



SiPM parameters statistics on IBIS1

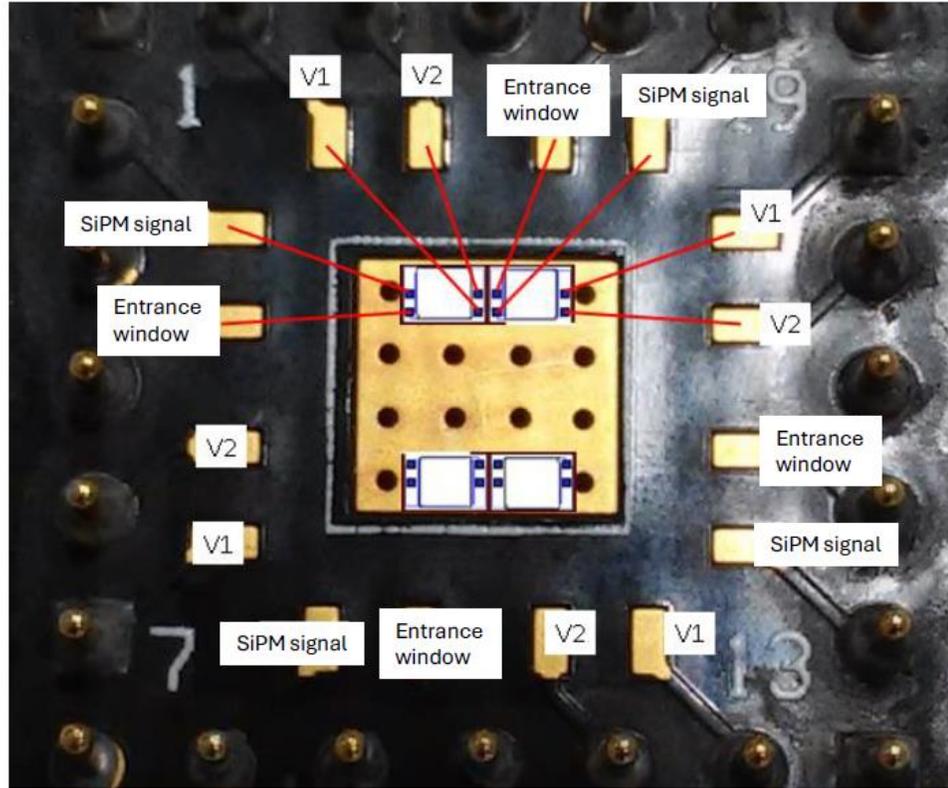
Breakdown Voltage

W3 – Trench Split 2 (Trench depth medium-)
 W6 – Trench Split 1 (Trench depth medium+)



Quite uniform breakdown voltage between same splits and different wafers





SiPM structure

Superficial implant (SI):

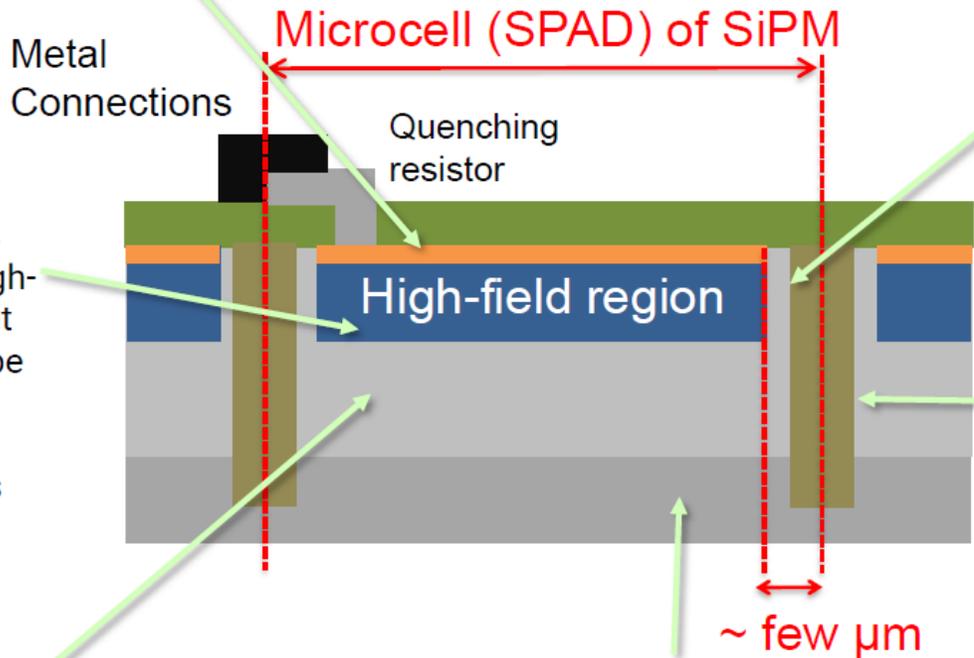
Very thin, constitutes the entrance window for the light into the SPAD. High-dose, opposite dopant polarity compared to the epitaxial layer, partially undepleted. Constitutes one half of the diode.

Virtual Guard Ring:

Dead border around the high-field region, necessary to prevent edge breakdown.

High-field region:

is defined with a high-energy deep implant (DI) of the same type as the epi layer. Avalanche multiplication takes place here.



Deep trench Isolation:

are used to isolate adjacent microcells electrically. Optical isolation depends on filling material.

Epitaxial layer:

The high-resistivity region in which the SiPM cells are built. Few μm thick. Almost fully depleted at breakdown. Close to the interface with the bulk, part of it is undepleted. Constitutes one half of the diode.

Bulk:

(Very) highly doped region upon which the epitaxial layer is built. Never depleted.

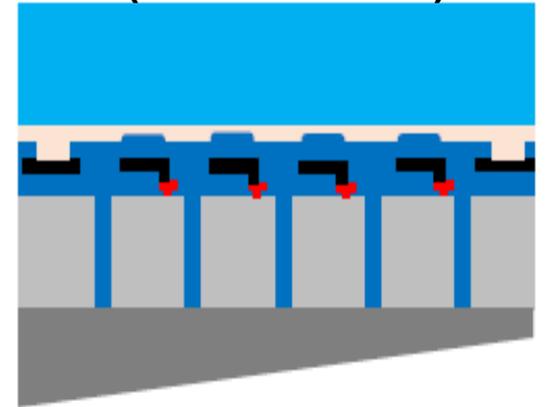


FBK dedicated a first learning cycle on mechanical tests and improvement of the process flow (wafer thinning - bulk removal, grinding)

One important challenge in developing the NUV-BSI process flow is **achieving small total thickness variation (TTV)** after wafer thinning

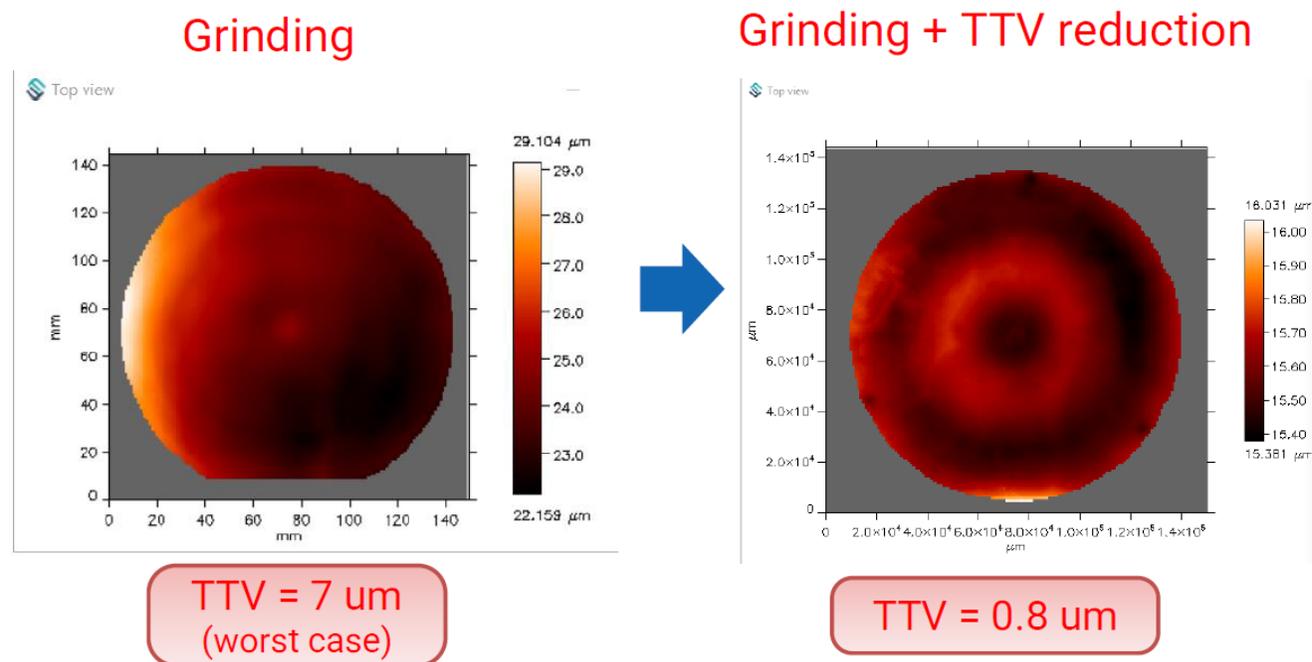
→ in order to ensure **consistent SPAD performance across the wafer**

**Wafer thinning
(bulk removal)**

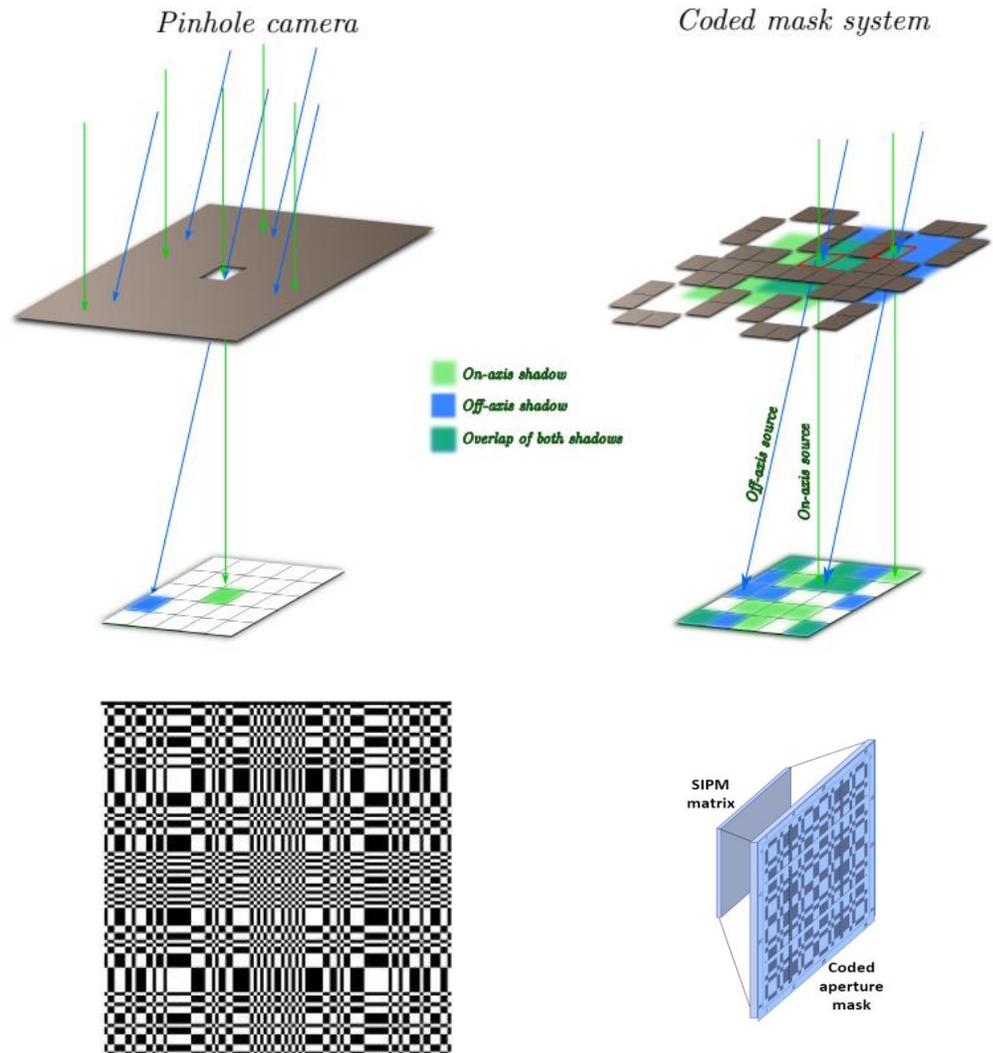


Too high Total Thickness Variation (TTV) evaluated after chemical mechanical polishing
→ **study of additional TTV reduction process**

Results obtained after optimization of recipes and procedures :
→ a **TTV of less than 1 μm** achieved with additional etching step



Optics development



- **Coded Aperture** mask techniques were developed as the evolution of a single pinhole camera

- matrix of multiple pinholes to improve light collection and reduce exposure time

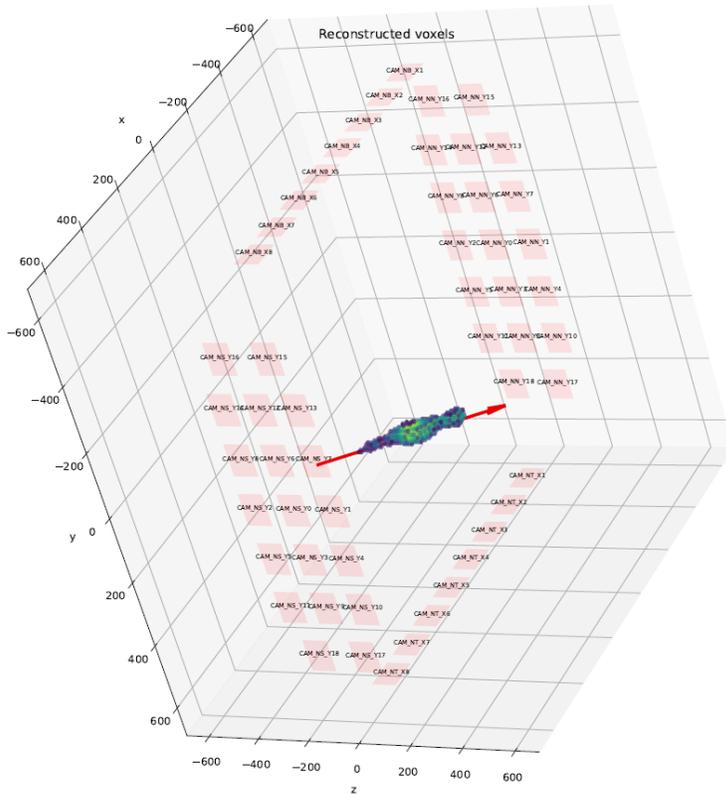
- **Image** formed on sensor is the superimposition of multiple pinhole images.

- **Advantages**
 - Good light transmission (50%)
 - Good depth of field
 - Small required volume

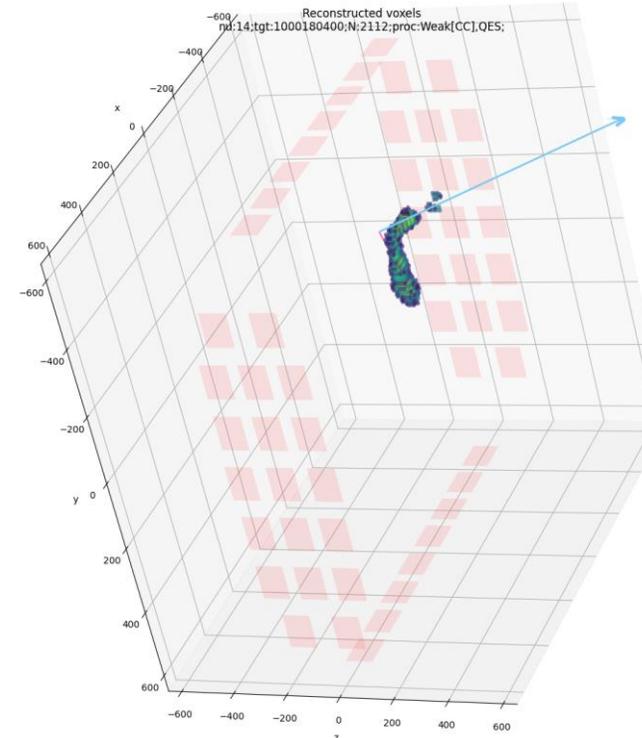


Examples

- Simulations of Coded Aperture masks with 3D reconstruction algorithm in LAr:



Cosmic Muon



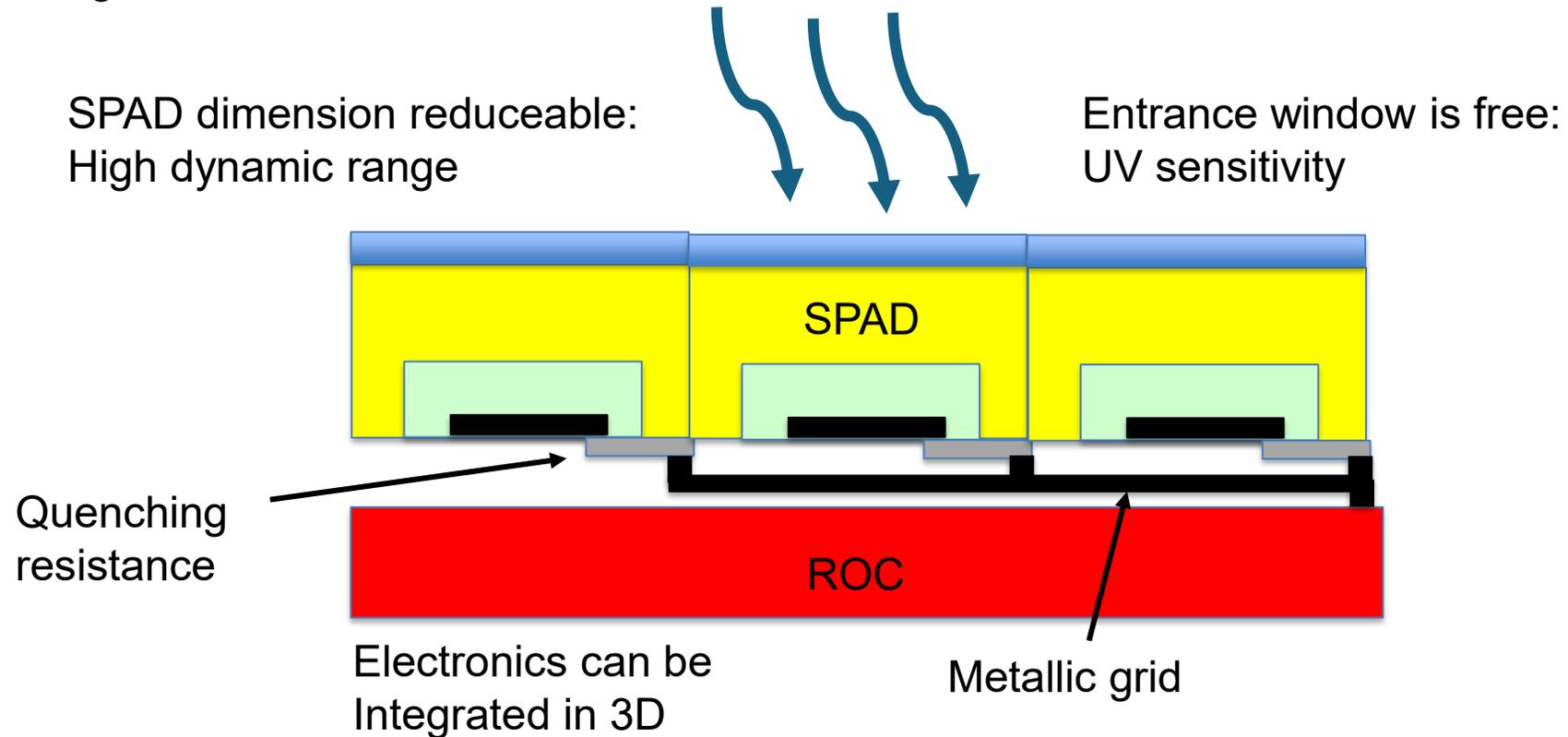
(a)

Neutrino Interaction (proton + muon)

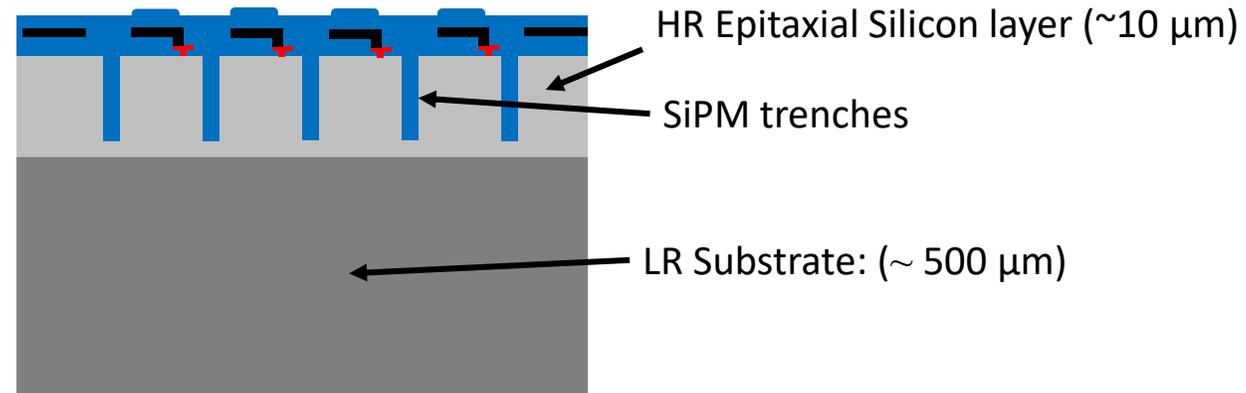


Electronics

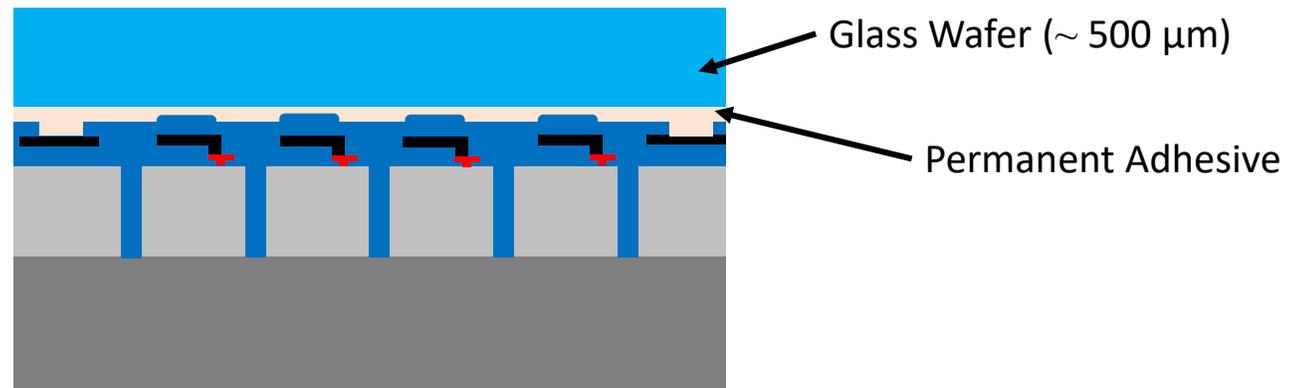
- ❑ As a first step of 3D integration, the design of INFN-Torino foresees a ReadOut Chip (ROC) based on the “Alcor” ASIC:
 - one channel in $440 \times 440 \text{ } \mu\text{m}^2$
 - mini-SiPM by grouping SPADS so that the size corresponds to one channel
 - chip bonding



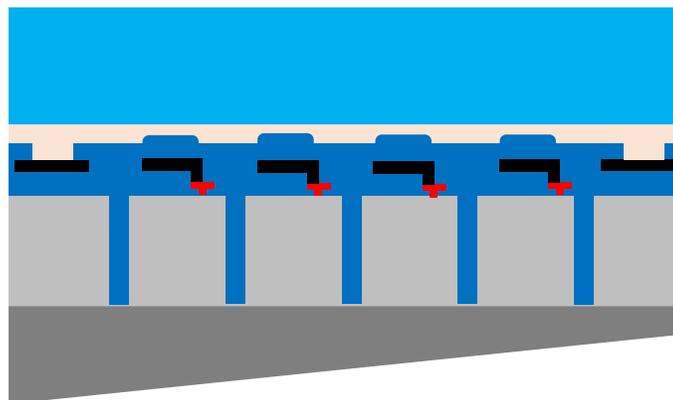
1. Starting Wafer (6")



2. Adhesive Permanent Bonding to Glass Wafer



3. Wafer thinning (Substrate Removal)

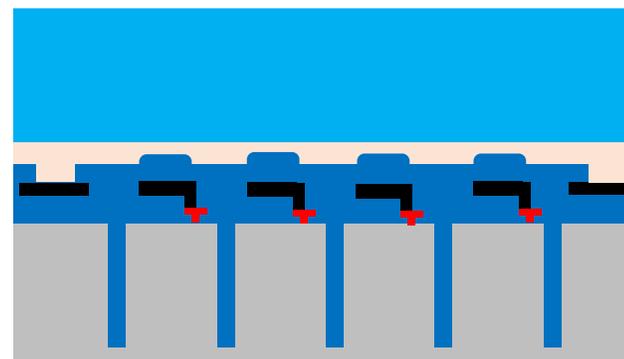


Remaining Substrate buffer after grinding: $\sim 10 \mu\text{m}$

Expected total thickness variation (TTV): 2-4 μm

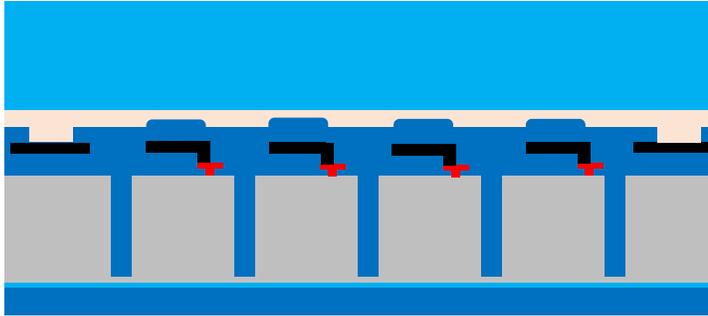
$\updownarrow 10 - 20 \mu\text{m}$

4. Etching of highly doped Silicon substrate using doping selective etching



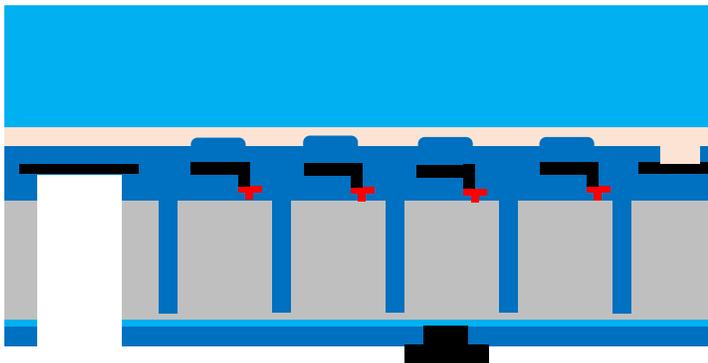
Doping Selective WET etching is used to complete the substrate removal and to reach the epi/sub interface by reducing the final TTV

5. Back junction Formation



- Final Polishing (tbd)
- Plasma Ion Implantation and laser annealing
- ARC deposition

7. Contact formation



Anode and cathode contacts form the backside