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Development of a 28 nm Cryogenic PDK for Next-Generation HEP Detectors

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Advances in high-energy physics (HEP) increasingly rely on ASICs operating at cryogenic temperatures. While modern 28 nm CMOS offers superior speed, power efficiency, and integration density, its behavior under deep cryogenic conditions deviates significantly from nominal operation. Threshold voltage shifts, mobility enhancement, mismatch, noise, and reliability mechanisms all change substantially, making standard room-temperature models inadequate. A dedicated cryogenic process design kit (cryo-PDK) in 28 nm is therefore essential for accurate modeling, simulation, and design. Such a PDK, validated down to 4 K, reduces design risk, enables first-pass silicon success, and establishes a framework for ASIC development in extreme environments.

This work describes the ongoing collaboration between LBNL and SLAC in four R&D directions: (1) the design of a 28 nm mini-ASIC with test structures covering all device flavors; (2) the development of a cryogenic test setup for characterization at 165 K, 77 K, and 4 K; (3) a model extraction and data-fitting platform for cryo-PDK development; and (4) radiation-hardness analysis. By capturing cryogenic device physics and closing the loop between measurement, modeling, and design, the cryo-PDK will enable next-generation low-noise, low-power, and radiation-tolerant readout systems for HEP detectors, quantum technologies, and space instrumentation.

Authors: ZARKOS, Panagiotis; PENA-PEREZ, Aldo; HEIM, Timon; LENARDO, Brian

Co-authors: PAPADOPOULOU, Aikaterini; ROTA, Lorenzo; GRACE, Carl; ZARCO, Valeria; GARCIA-SCIVERES, Maurice; BOATENG, Kevin K.; KWE, Bryan; PARKER, Chase R.; TURBINER, Victor; JOHNSON, Will; ATENCIO, Ariella; HSU, Marissa (SLAC National Laboratory); LU, Michael (SLAC National Laboratory)

Presenter: LENARDO, Brian

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