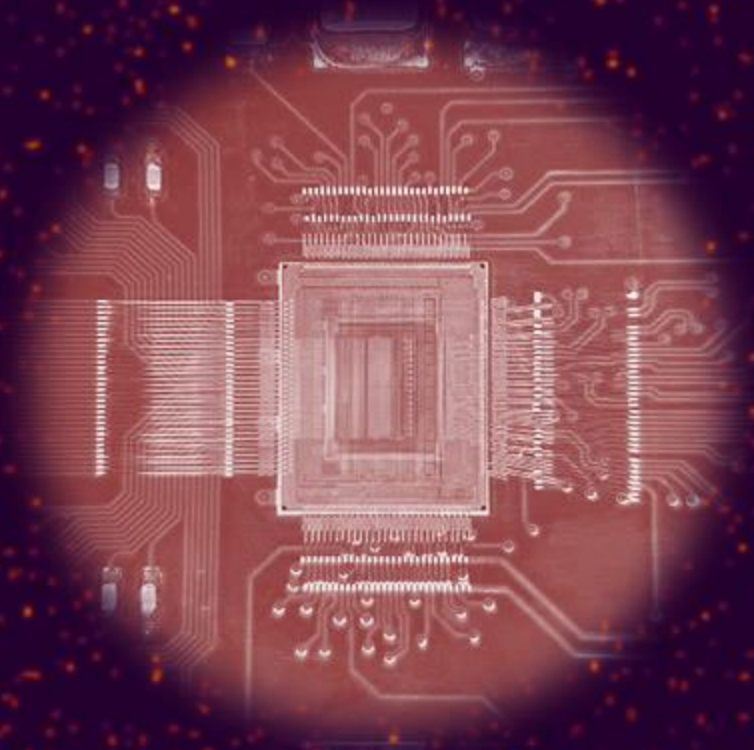


Coordinating Panel on Advance Detectors – CPAD 2025  
Inn at Penn, University of Pennsylvania

RDC4 Readout and ASICs

# Development of a 28 nm Cryogenic PDK for Next-Generation HEP Detectors



Brian Lenardo  
on behalf of LBL and SLAC

Oct. 9<sup>th</sup>, 2025



# LBL-SLAC: 28nm CMOS Cryogenic Models

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## How the collaboration started?

- Clear interest in our community in having cryogenic models for TSMC 28nm HPC+ (core devices)
- LBL designed an array of test structures for characterization at cryogenic temperatures, as part of an internal LBL LDRD (PI: Timon Heim)
  - Designer: Panagiotis Zarkos
- SLAC was also planning to develop cryo-models for TSMC 28nm HPC+ (KA25 PI: Aldo Pena Perez)
  - Designers: SLAC IC team
- LBL shared their design to enable collaboration
- **Joint submission of a 2nd prototype of test structures chip** with minor improvements based on LBL feedback from 1st prototype

# LBL-SLAC: 28nm CMOS Cryogenic Models

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## Primary goal:

Cryogenic characterization of 28 nm CMOS for the development of custom cryogenic models

## Key R&D directions

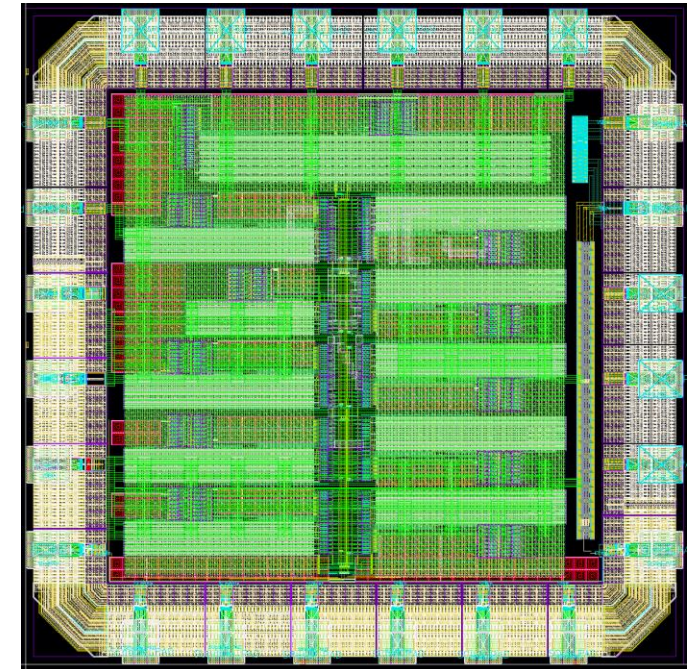
- The design of a 28 nm mini-ASIC with test structures covering core device flavors
- Development of a cryogenic test setup for characterization at 165 K, 77 K, and 4 K
- A model extraction and data-fitting platform for custom cryo-model development
- Radiation-hardness analysis

# 28 nm CMOS Chip with Test Structure

- Modifications to LBL design done by graduate students (**ex-HEPIC**):
  - Victor Turbiner
  - Will Johnson
  - Marissa Hsu
  - Kevin Boateng
- Area reduced to fit in 1x1 mm<sup>2</sup> area
- Test structures include a variety of device flavors
- Great opportunity for new designers to do a tape-out on advanced node
- Chip submitted in Jan 24<sup>th</sup>, 2025

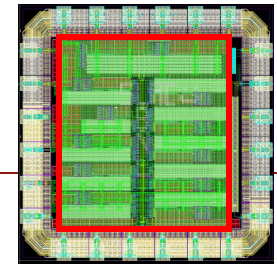
## Goals for 2025:

- Joint characterization campaign between LBL and SLAC
- Targeting different temperatures: LAr/LXe and deep cryo (4 K)
- Complementary expertise and instrumentation
- **Seek ways to continue collaboration (possible RDC4 working group)**

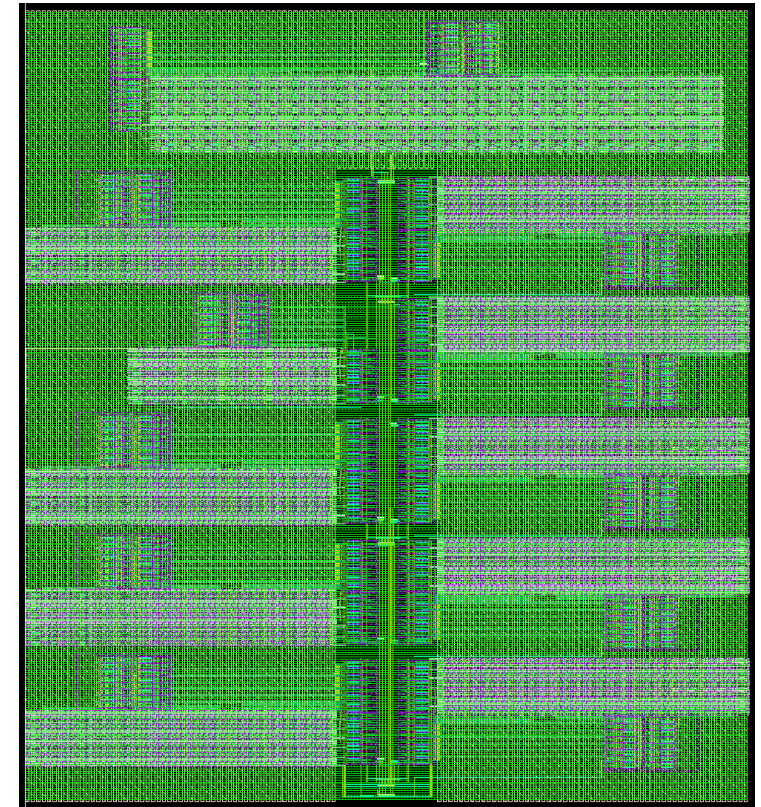
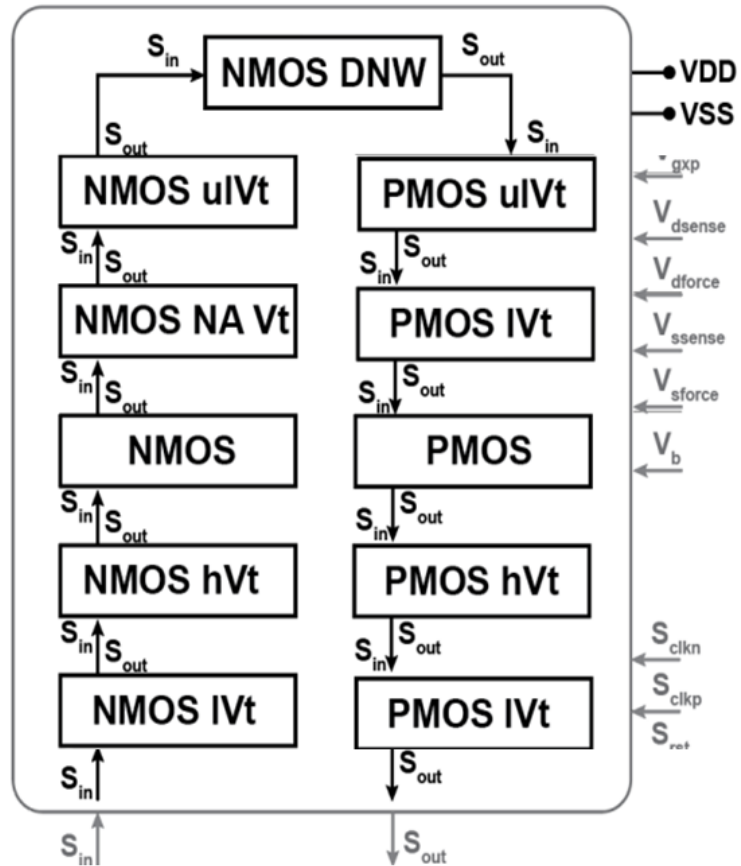


LBL-SLAC R&D Prototype  
(28 nm CMOS)

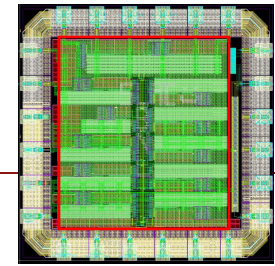
# 28 nm CMOS Chip with Test Structure



## Brief Overview of the Core

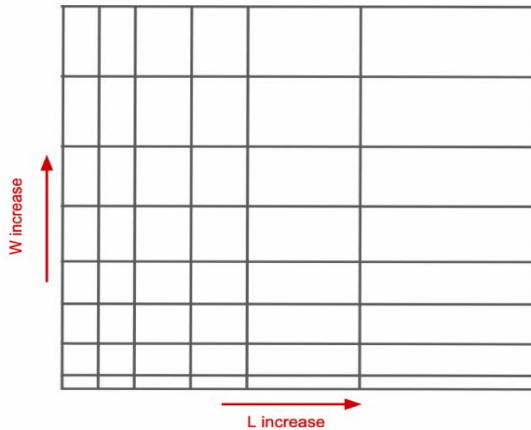


# 28 nm CMOS Chip with Test Structure



## Brief Overview of the Core

### Matrix array per device



#### Single finger devices

L (nm) = 30, 40, 60, 90, 200, 500, 1000

W (um) = 0.1, 0.2, 0.4, 0.8, 1.6, 3

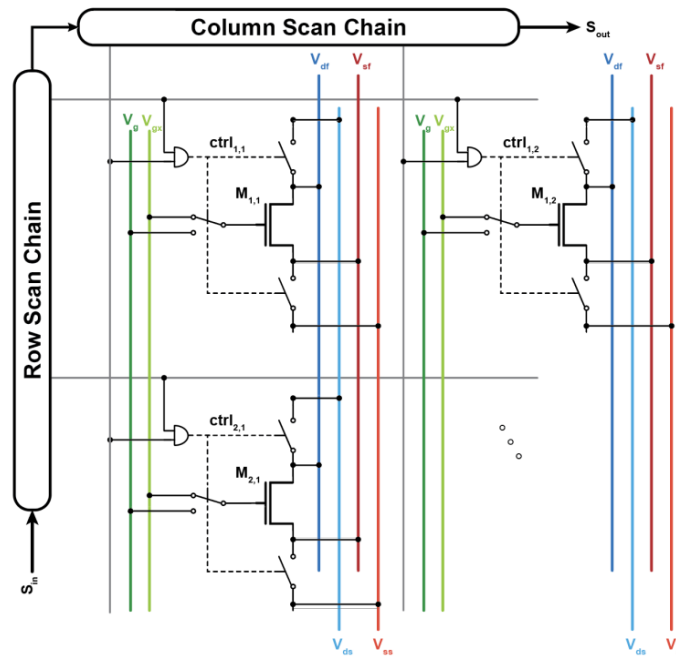
#### Multi-finger devices

L (nm) = 30, 40, 60, 90, 200, 500, 1000

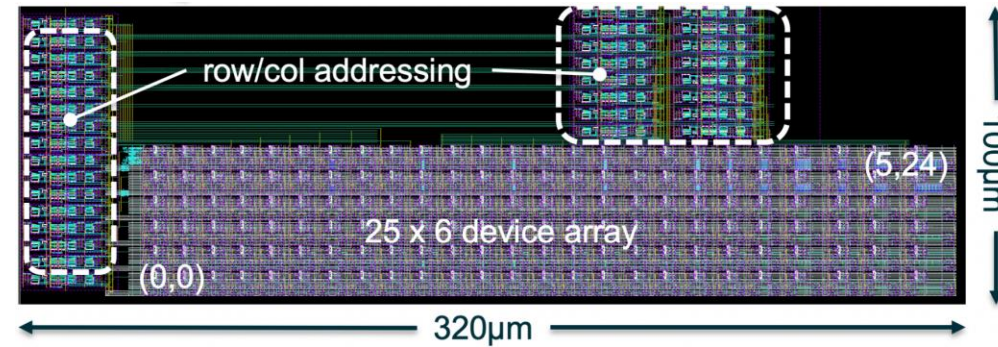
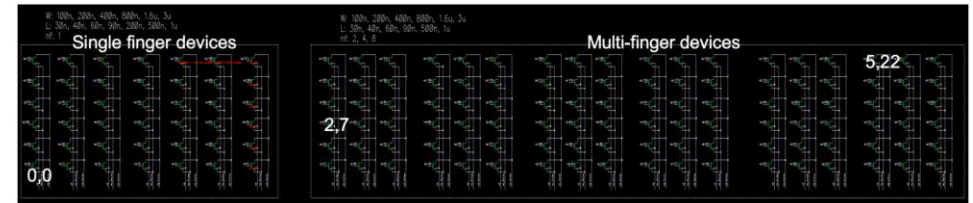
W (um) = 0.1, 0.2, 0.4, 0.8, 1.6, 3

nf = 2, 4, 8

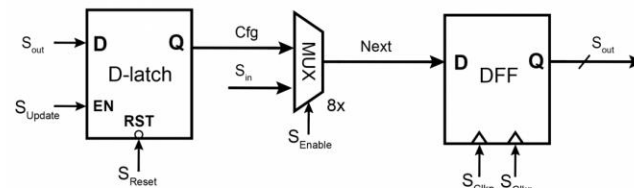
### Row/Column selection



### Example of NMOS devices



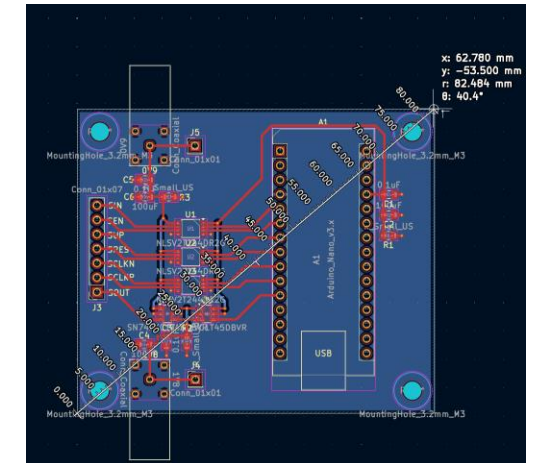
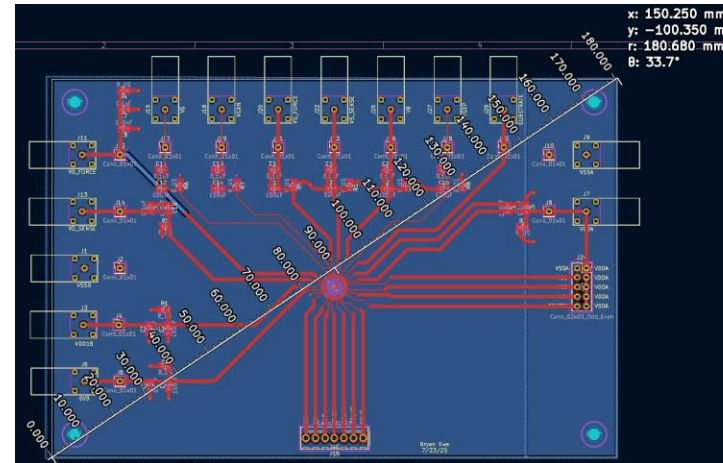
### Some logic for device selection



# PCB Design Status

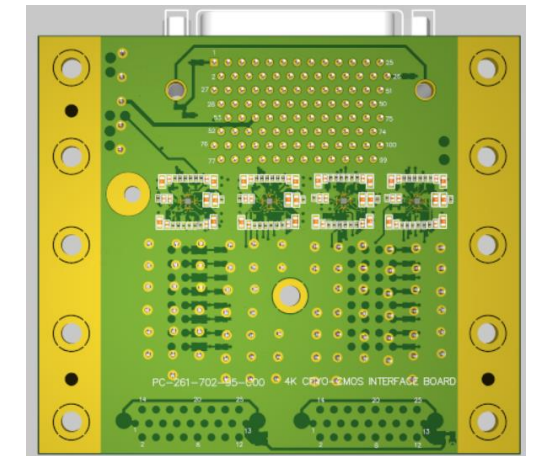
## Initial testing

- LBL student ([Bryan Kwe](#)) designed a single-chip carrier board for functionality assessment
- Arduino-based DAQ system implemented
- Initial tests confirmed device communication

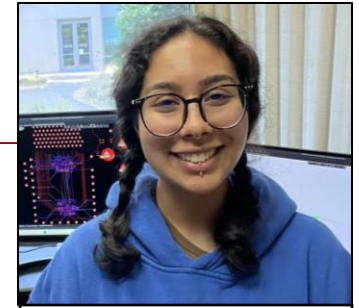


## Cold board

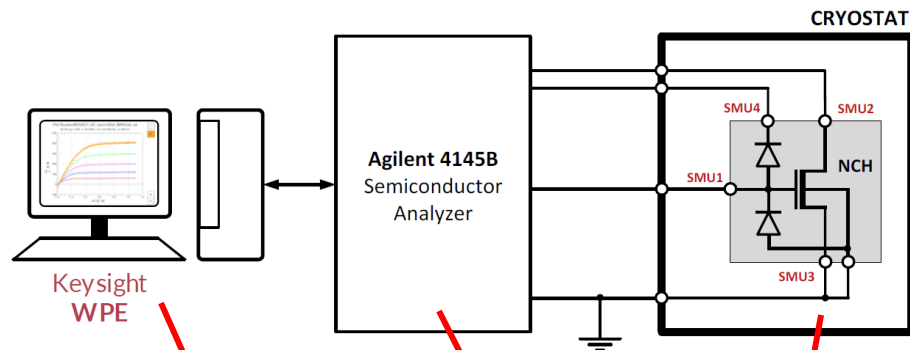
- SLAC in collaboration with LBL, is developing a dual-chip carrier board
- Targeted for cryogenic characterization at 165 K, 87 K, and 4 K
- Arduino-based DAQ system could be adapted for this board



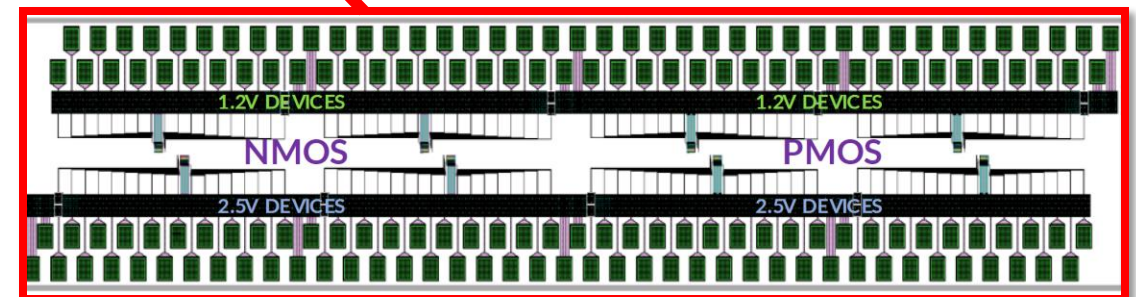
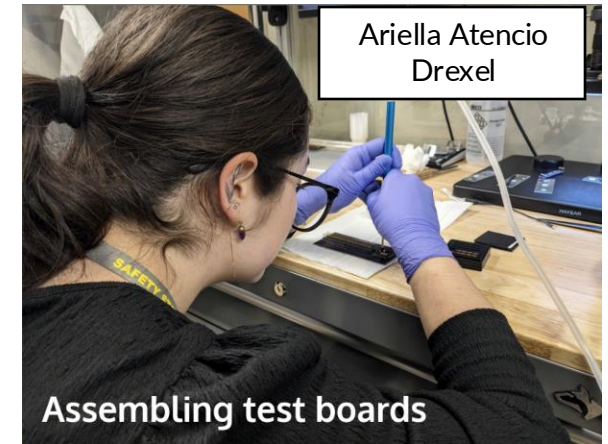
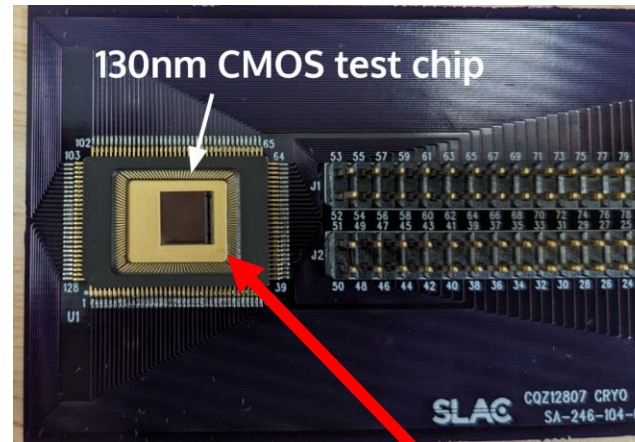
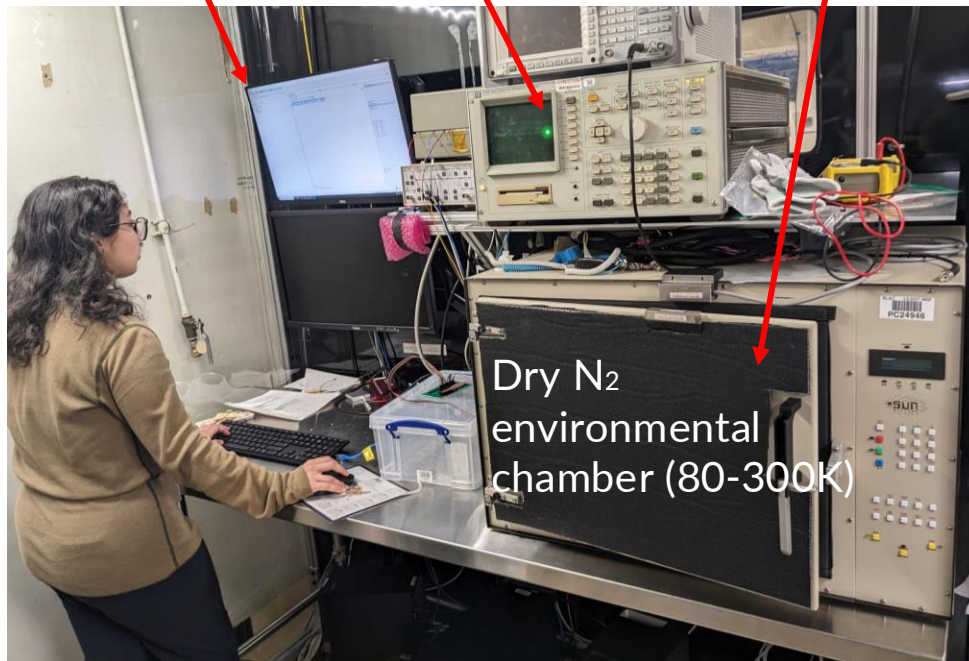
# Device Characterization Setup at SLAC



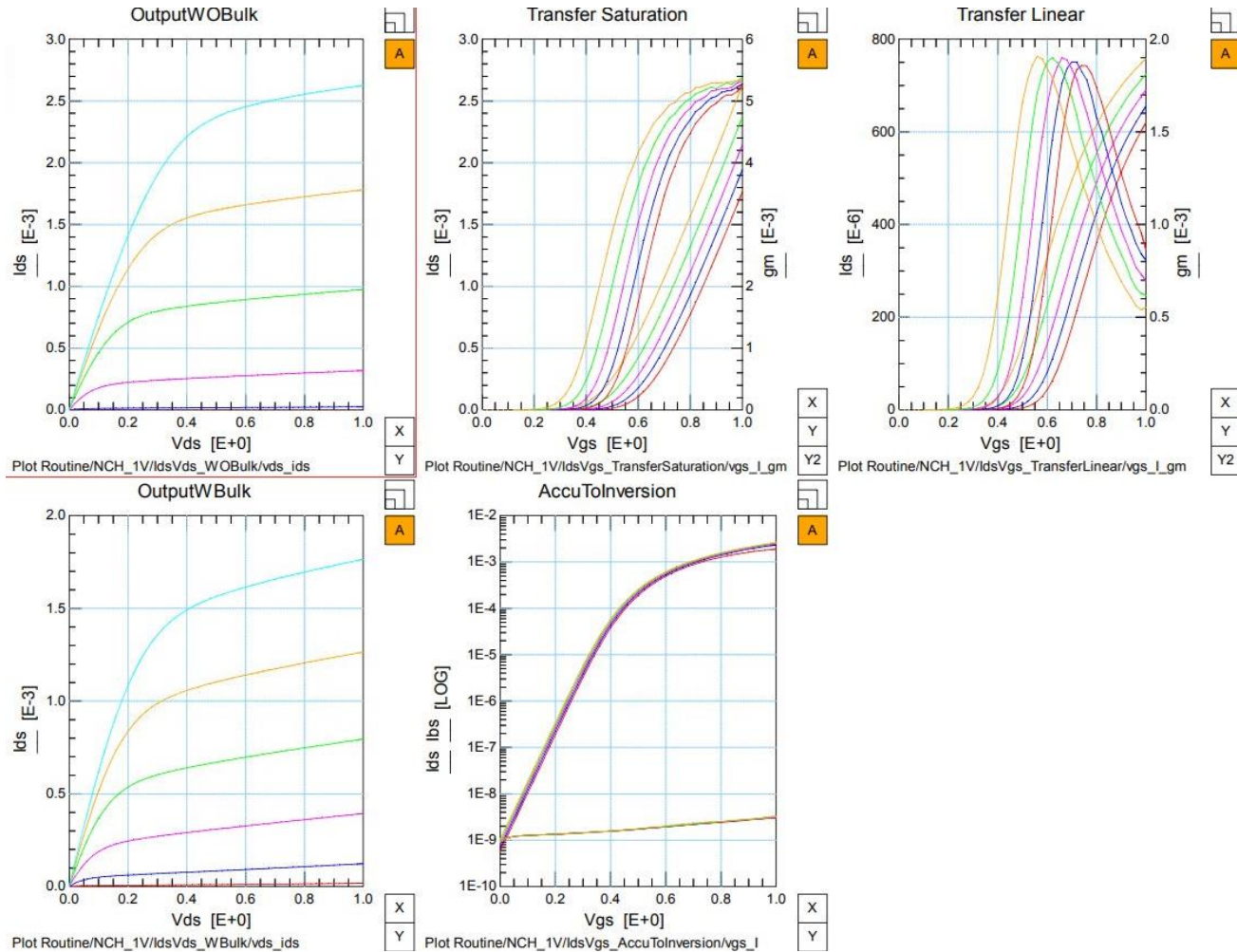
Valeria Zarco  
Skyline College ->  
UC Davis



- Set up summer 2025 for new measurements of TSMC 130nm

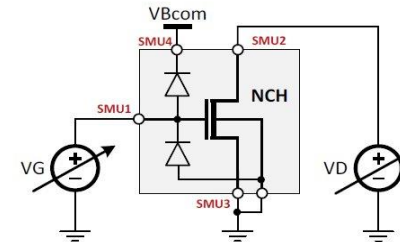


# DC Measurement Routines

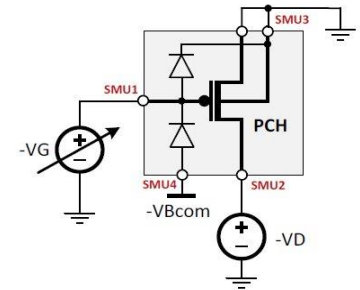
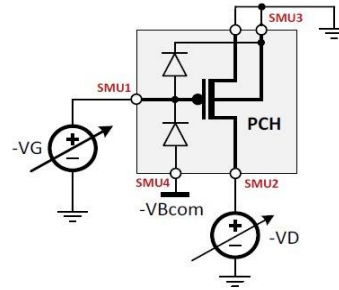
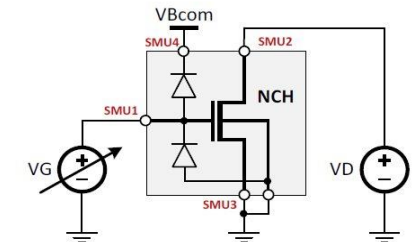


- Five different automated measurement routines for each device flavor for comprehensive I-V characterization

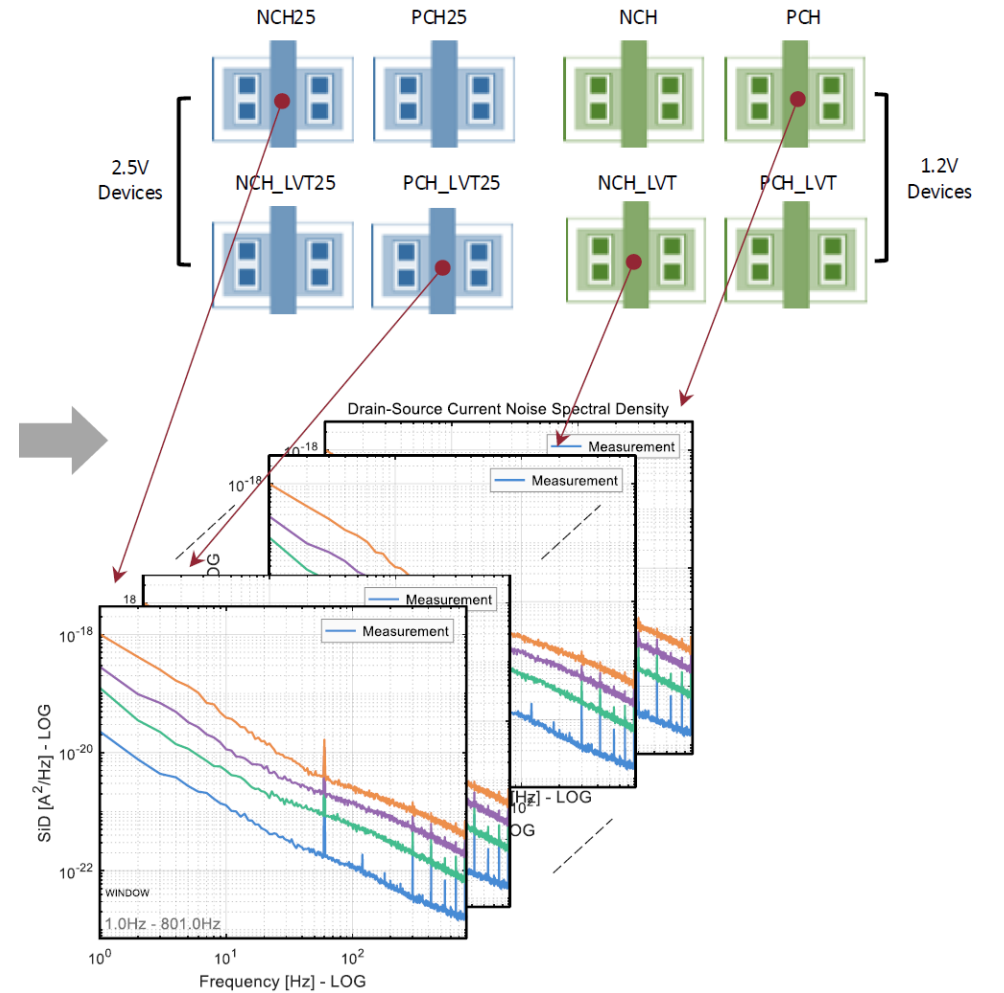
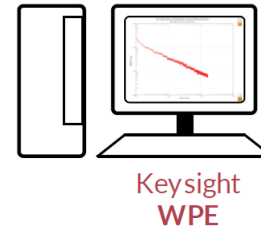
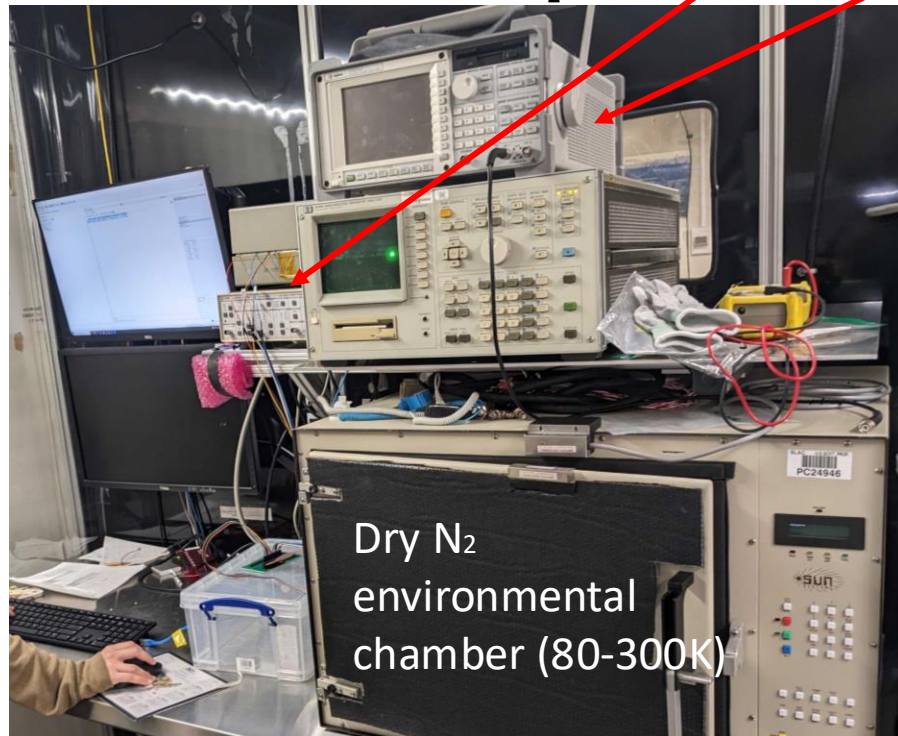
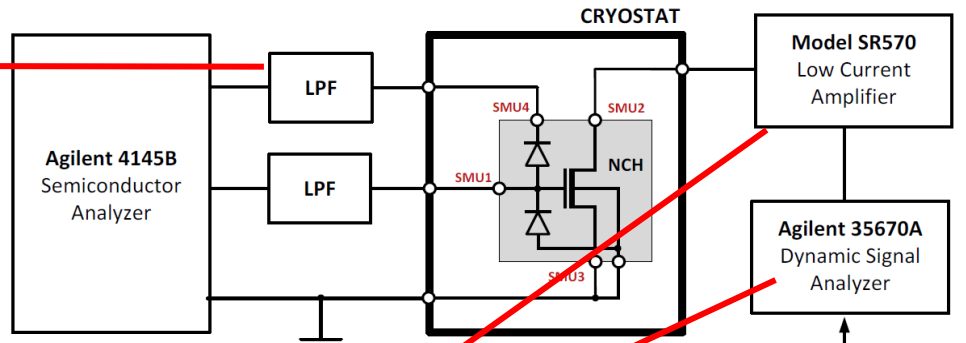
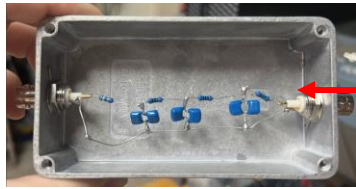
$I_{ds}$  vs  $V_{ds}$  Curve @ Different  $V_{gs}$



$I_{ds}$  vs  $V_{gs}$  Curve @ Fixed  $V_{ds}$



# Noise Measurements





# Summary & Next Steps

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## Developed 28nm CMOS chip with test structures for cryogenic characterization

- LBL design, SLAC/LBL collaboration for version 2
- Carrier PCB design nearly completed

## Testing routines and flow established, based on experience with 130nm CMOS

- SLAC lab prepared for testing at LXe (170K) and LAr (80K) temperatures
- Deep cryo (4K) testing planned at LBL

## Next steps:

- Fabricate PCBs and reconfigure testing routines for 28nm technology
- First measurements anticipated in coming months

# Acknowledgments

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## ▪ LBL

- Timon Heim
- Panagiotis Zarkos
- Bryan Kwe
- Aikaterini Papadopoulou
- Carl Grace
- Maurice Garcia-Sciveres

## ▪ SLAC

- Brian Lenardo
- Victor Turbiner
- Will Johnson
- Marissa Hsu
- Kevin Boateng
- Chase Parker
- Valeria Zarco
- Ariella Atencio
- Michael Lu
- Lorenzo Rota
- Aldo Pena-Perez



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# Thanks!

## Q/A

### Contact info:

- Brian Lenardo ([blenardo@slac.stanford.edu](mailto:blenardo@slac.stanford.edu))
- Timon Heim ([theim@lbl.gov](mailto:theim@lbl.gov))
- Panagiotis Zarkos ([panzark@lbl.gov](mailto:panzark@lbl.gov))
- Aldo Pena Perez ([aldopp@slac.stanford.edu](mailto:aldopp@slac.stanford.edu))