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# Possible new iterations of the VMM chip for MPGD readout

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The JLab SoLID experiment is assessing the VMM ASIC family for GEM tracker readout in high-rate environments. The current VMM3a falls short of requirements. We propose a VMM3b revision with optimized gain and shaping time for high-rate GEM and uRWell operation. Additionally, we are considering a VMM4 version, migrating to TSMC 65nm, with redesigned ADCs, digital core, and new features to serve broader MPGD community applications.

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