DG CIRCUITS
ASICs for Radiation Detectors

Jefferson Lab

SoLID
SOLENOIDAL LARGE INTENSITY DEVICE

Possible New Iterations of the VMM Chip for MPGD Readout

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Outline

VMM3a ASIC

Architecture and Functionality

VMM3S ASIC for SoLID

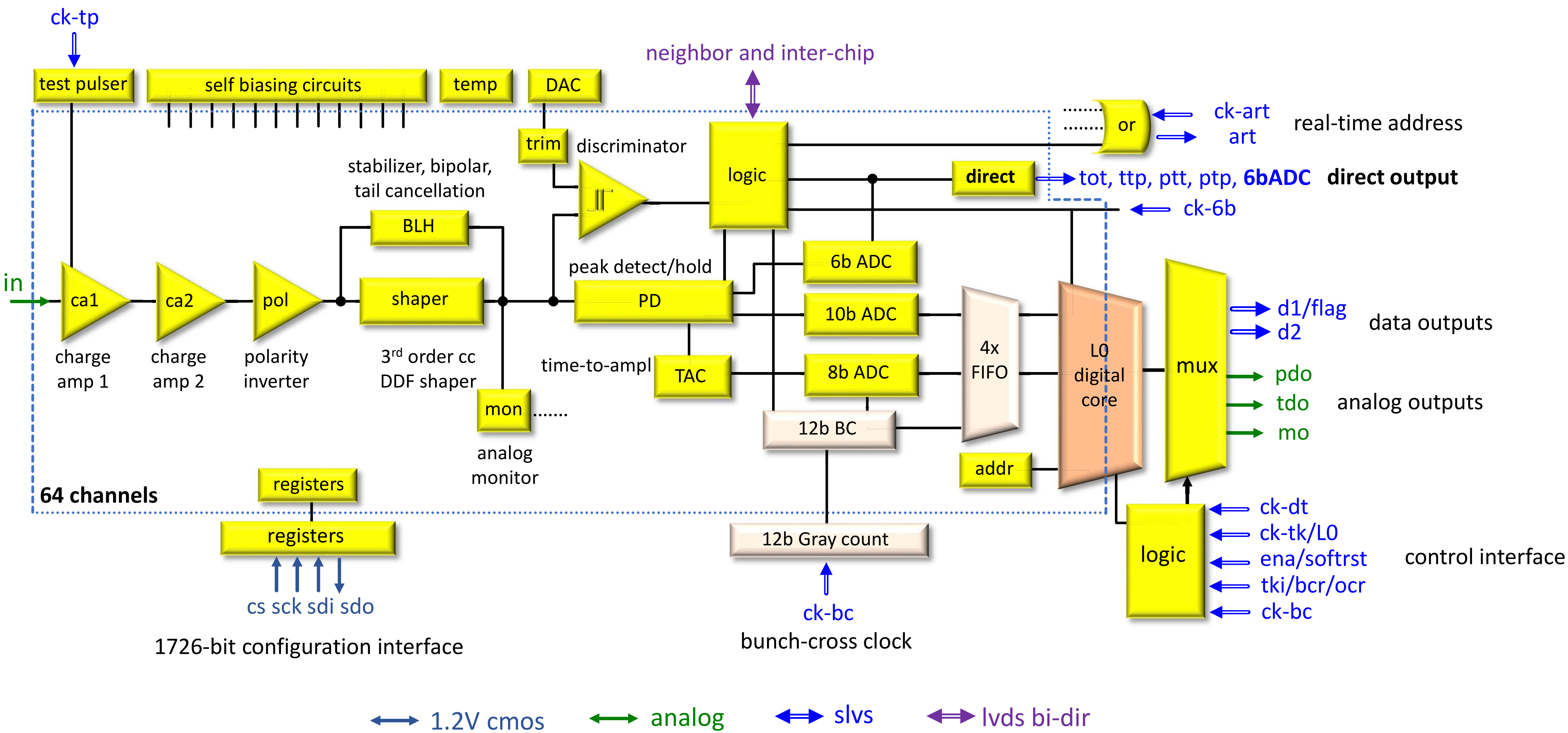
Motivation

Planned Modifications

Forthcoming ASIC Designs

VMM3a Architecture

Designed in 2018 for the ATLAS Muon Spectrometer Upgrade



VMM3a Functionality and Programmability

Front-End
- optimized for 200pF, programmable stabilization for 2pF to 2nF
- adjustable polarity, adaptive mirror for high-rate DC and AC operation
- fast recovery from high charge events (up to 12pC)

Shaping
- adjustable conversion gain: 0.5mV/fC (2pC), ... , 16mV/fC (64fC)
- adjustable peaking time: 25, 50, 100, 200 ns
- programmable ion tail cancellation

Timing
- at leading edge or peak (low time-walk)
- programmable time-to-amplitude conversion (TAC)

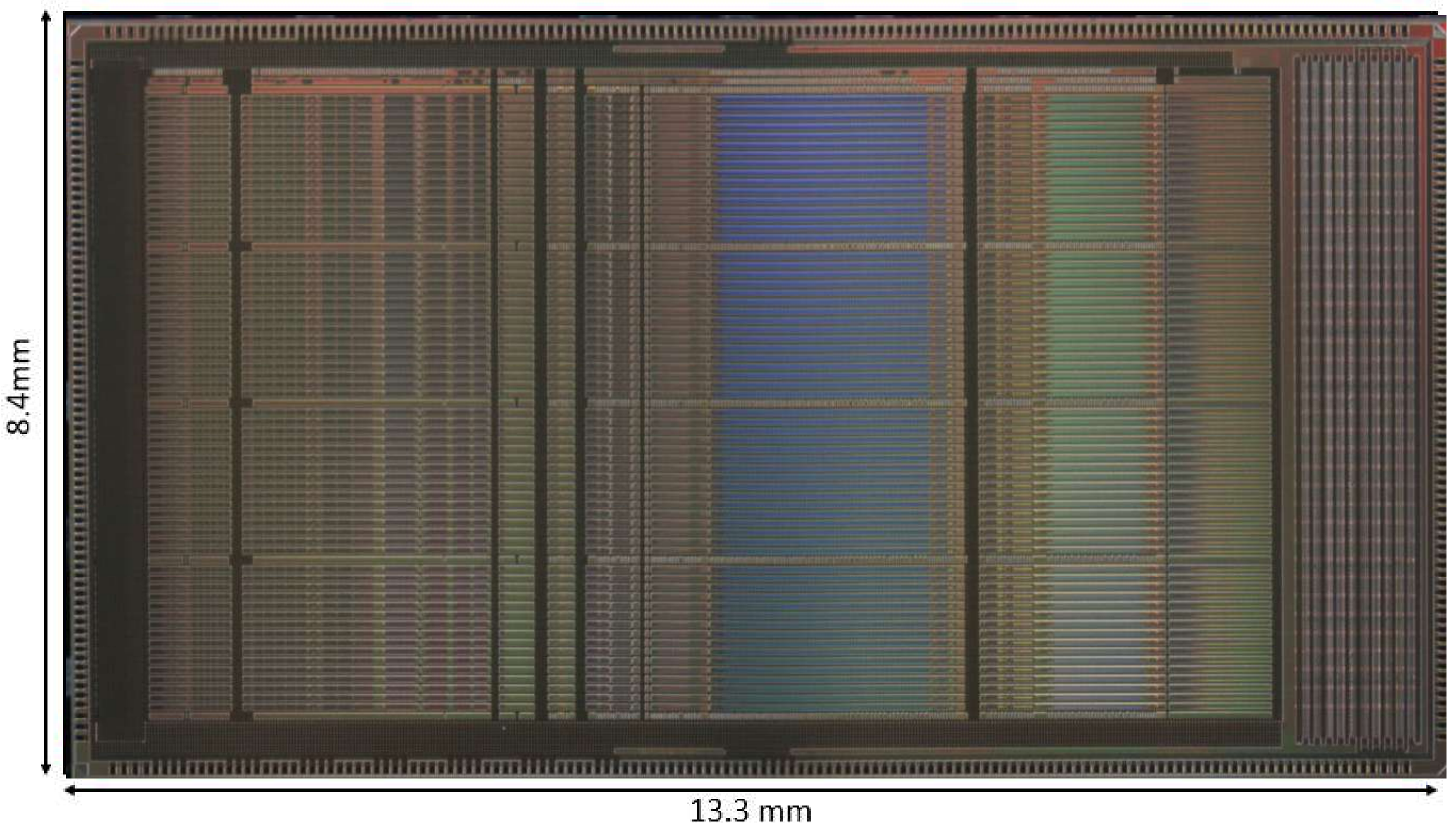
Discrimination
- sub-hysteresis, neighbor processing with inter-chip communication
- external acceptance with auto-reset, fast-reset

Readout
- continuous or two-phase (acquisition/readout)
- full digital or mixed-signal (external ADCs)

Service
- programmable test pulse generator and injection capacitor
- analog monitor: BGR, DACs, pulser, BGR, temperature, analog signals

regarded as "the working horse for RD51 frontends"

VMM3a Layout and Packaging



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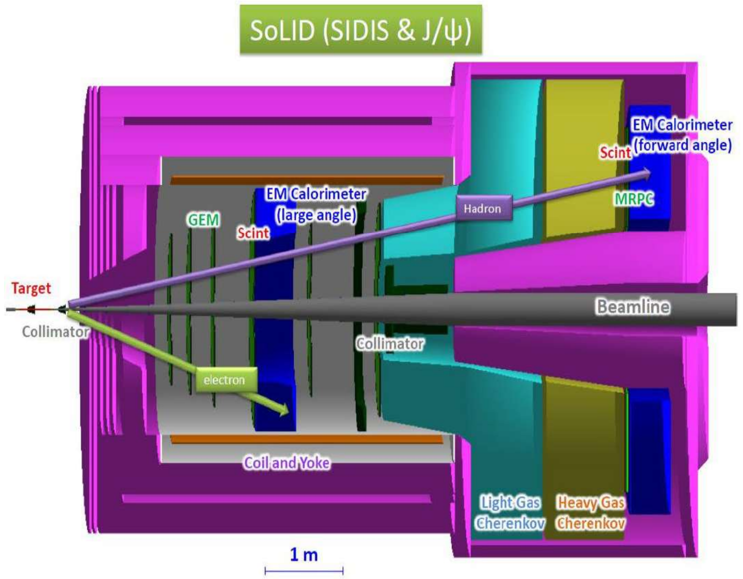
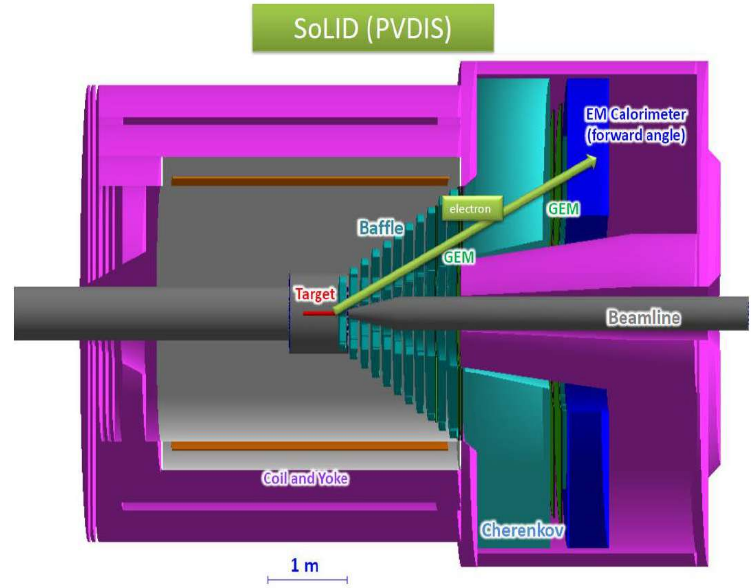
B	vddp	vddp	vddp	Vss	Vss	Vss	Vss	pdo	Vdd	Vdd	Vdd	Vssd	+ CKBC -		+ CKTP -		SDI	SDO	CS	SCK
C	i0	i1	i2	i3	Vss	Vss	Vss	mo	Vdd	Vdd	Vdd	Vssd	+ TKI -		+ TKO -		+ ENA -		+ CK6B -	
D	i4	i5	i6	i7	Vss	Vss	Vss	Vdd	Vdd	Vdd	Vdd	Vssd	+ CKTK -		+ DT0 -		+ DT1 -		+CKART-	
E	i8	i9	i10	i11	Vss	Vss	Vss	Vdd	Vdd	Vdd	Vdd	Vssd	+ ART -		+ CKDT -		+ t0 -		+ t1 -	
F	i12	i13	i14	i15	Vss	Vss	Vss	Vdd	Vdd	Vdd	Vdd	Vssd	+ t2 -		+ t3 -		+ t4 -		+ t5 -	
G	i16	i17	i18	i19	Vss	Vss	Vss	Vdd	Vdd	Vssd	Vssd	Vssd	+ t6 -		+ t7 -		+ t8 -		+ t9 -	
H	i20	i21	i22	i23	Vss	Vss	Vss	Vdd	Vdd	Vssd	+ t10 -		+ t11 -		+ t12 -		+ t13 -		+ t14 -	
J	i24	i25	i26	i27	Vss	Vss	Vss	Vdd	Vdd	Vssd	+ t15 -		+ t16 -		+ t17 -		+ t18 -		+ t19 -	
K	i28	i29	i30	i31	Vss	Vss	Vss	Vdd	Vdd	Vssd	+ t20 -		+ t21 -		+ t22 -		+ t23 -		+ t24 -	
L	i32	i33	i34	i35	Vss	Vss	Vss	Vdd	Vdd	Vddd	+ t25 -		+ t26 -		+ t27 -		+ t28 -		+ t29 -	
M	i36	i37	i38	i39	Vss	Vss	Vss	Vdd	Vdd	Vddd	+ t30 -		+ t31 -		+ t32 -		+ t33 -		+ t34 -	
N	i40	i41	i42	i43	Vss	Vss	Vss	Vdd	Vdd	Vddd	+ t35 -		+ t36 -		+ t37 -		+ t38 -		+ t39 -	
P	i44	i45	i46	i47	Vss	Vss	Vss	Vdd	Vdd	Vddd	Vddd	Vddd	+ t40 -		+ t41 -		+ t42 -		+ t43 -	
R	i48	i49	i50	i51	Vss	Vss	Vss	Vdd	Vdd	Vdd	Vdd	Vddd	+ t44 -		+ t45 -		+ t46 -		+ t47 -	
T	i52	i53	i54	i55	Vss	Vss	Vss	Vdd	Vdd	Vdd	Vdd	Vddd	+ t48 -		+ t49 -		+ t50 -		+ t51 -	
U	i56	i57	i58	i59	Vss	Vss	Vss	Vdd	Vdd	Vdd	Vdd	Vddd	+ t52 -		+ t53 -		+ t54 -		+ t55 -	
V	i60	i61	i62	i63	Vss	Vss	Vss	Vdd	Vdd	Vdd	Vdd	Vddd	+ t56 -		+ t57 -		+ t58 -		+ t59 -	
W	vddp	vddp	vddp	Vss	Vss	Vss	Vss	Vdd	Vdd	Vdd	Vdd	Vddd	+ t60 -		+ t61 -		+ t62 -		+ t63 -	
Y	vddp	vddp	vddp	Vss	Vss	Vss	Vss	Vdd	Vdd	Vdd	V ssad	V ssad	V ssad	V ssad	V ddad	V ddad	V ddad	V ddad	+ SETB -	

- Vddp: preamp +1.2V
- Vdd: analog +1.2V
- Vss: analog 0V
- V ddad: ADC +1.2V
- V ssad: ADC 0V
- Vddd: digital +1.2V
- Vssd: digital 0V
- analog in
- analog out
- digital SE IO
- + xxx -: SLVS IO

- CMOS 130nm, single 1.2V supply, 6-10 mW/channel
- available as die or BGR 400 package

Solenoidal Large Intensity Device (SoLID) at Jefferson Lab





https://solid.jlab.org/

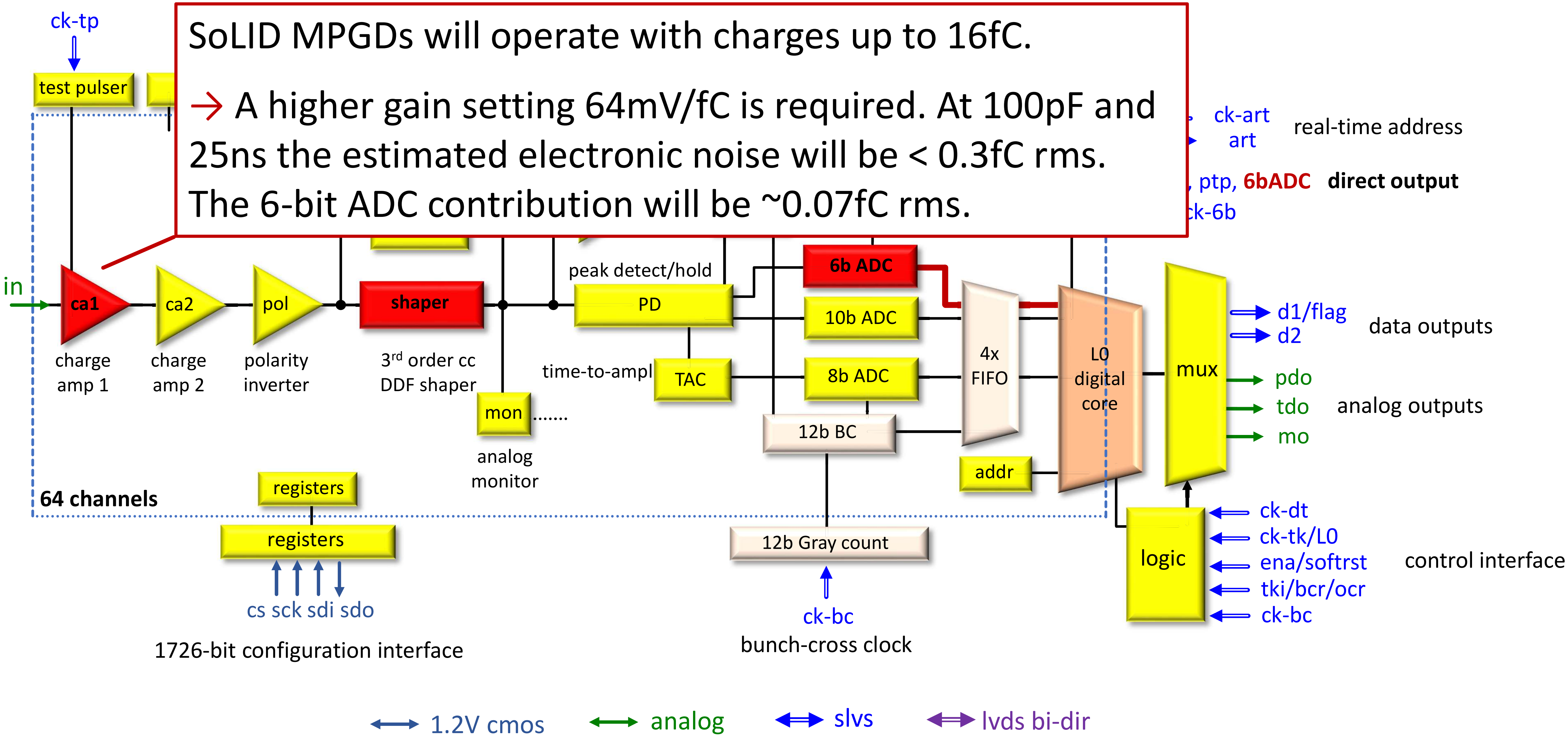
- Large use of Micro-Pattern Gas Detectors (MPGDs) like Gas Electron Multipliers (GEMs) and micro-Resistive WELLs (µRWELLs) operating at very high luminosity: high-bandwidth events (~100MHz) occurring for few hundred ns (~400ns) at relatively high frame rates (>100kHz)
- For initial deployment, JLAB is evaluating a modified version of VMM (VMM3S) operating in 6-bit direct output mode. In the longer term JLAB will use waveform sampling.

Planned Modifications in VMM3S

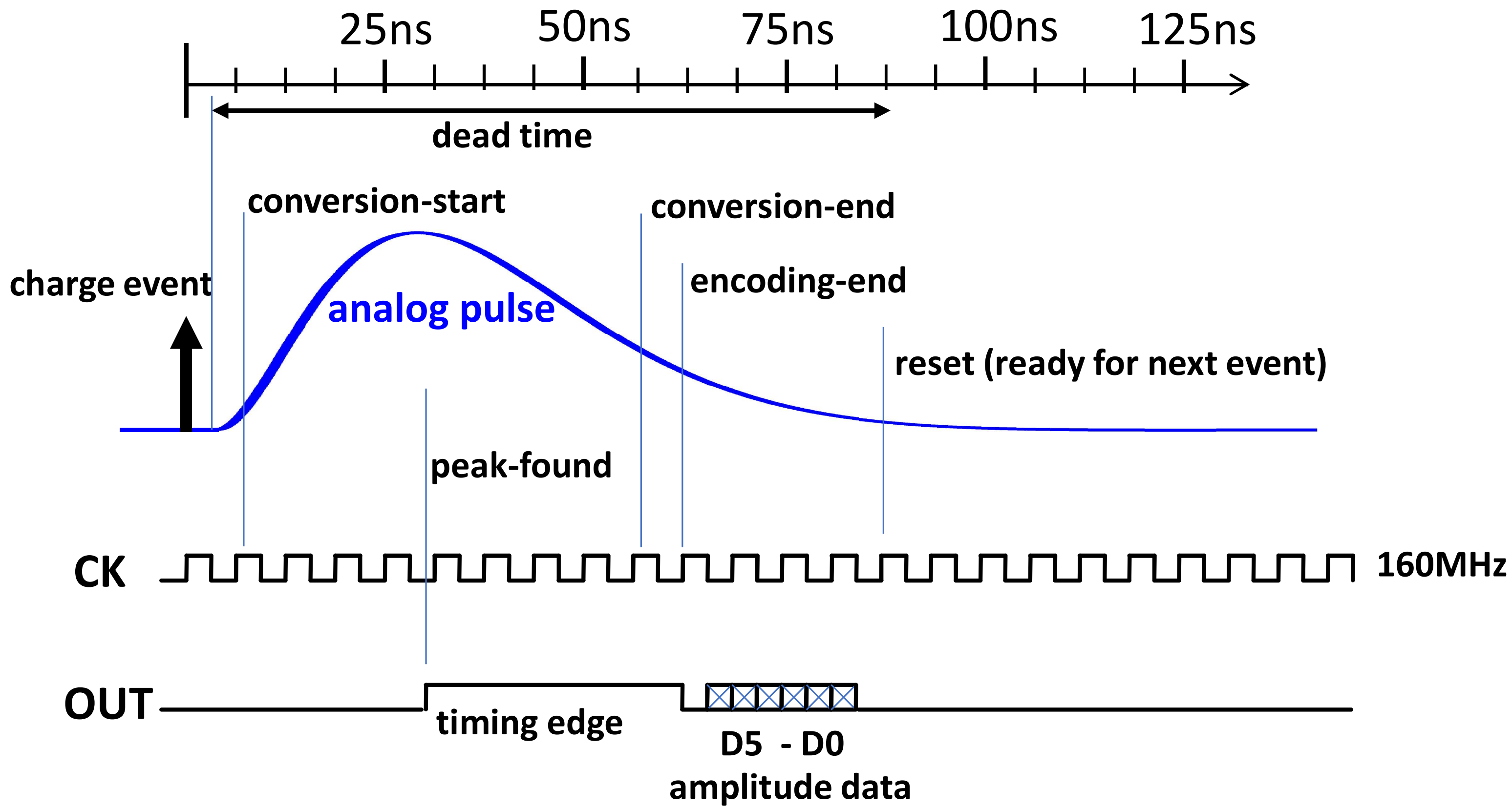
blocks to be revised are in red

SoLID MPGDs will operate with charges up to 16fC.

→ A higher gain setting 64mV/fC is required. At 100pF and 25ns the estimated electronic noise will be < 0.3fC rms. The 6-bit ADC contribution will be ~0.07fC rms.

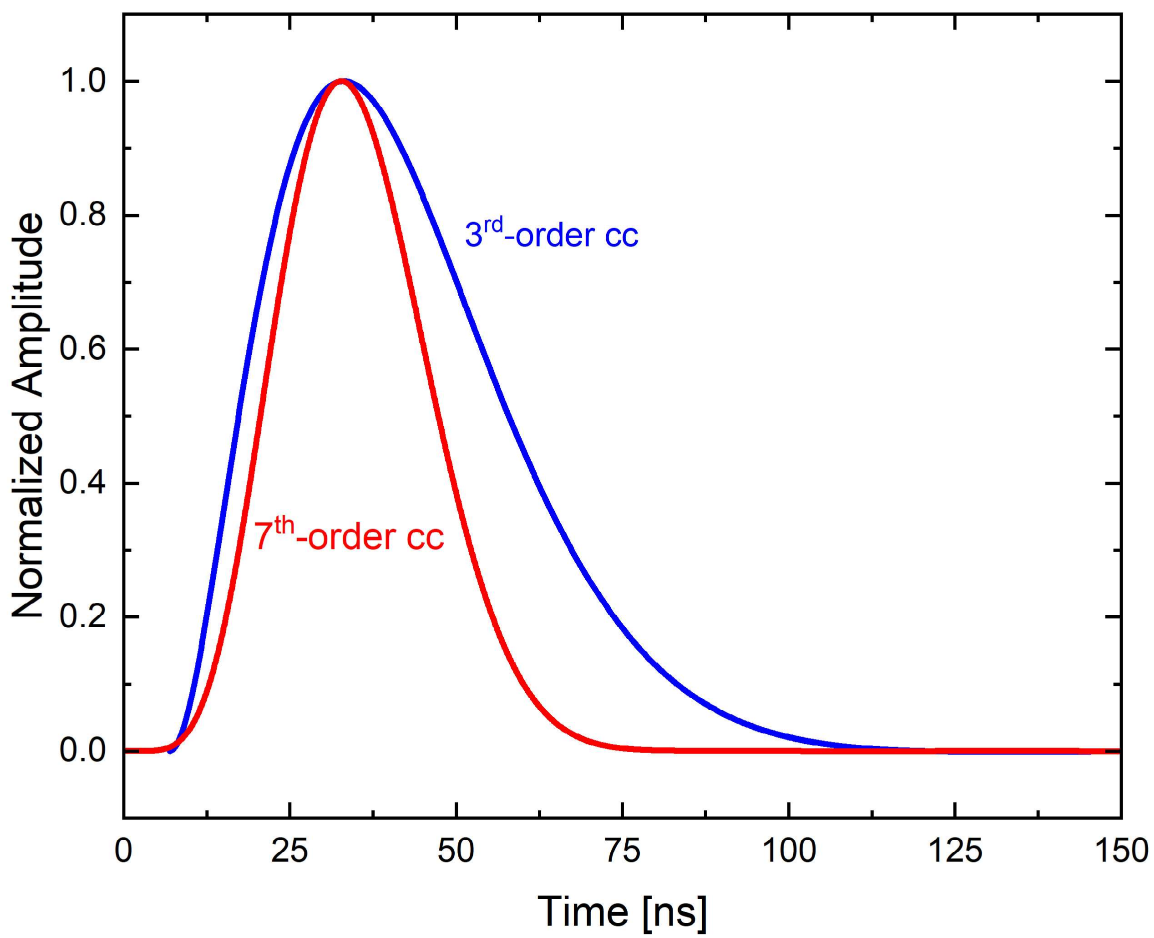


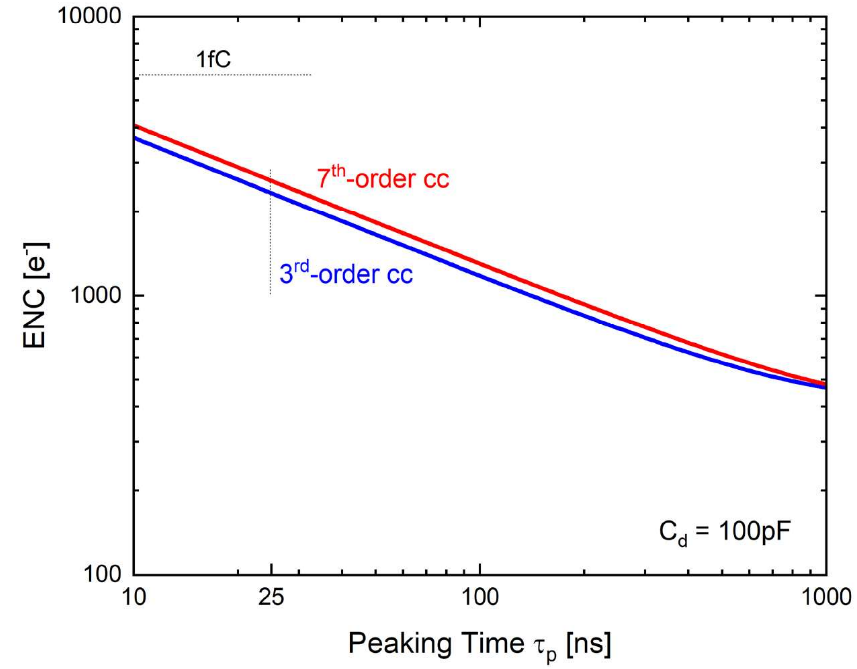
6-Bit Direct Output in VMM3a

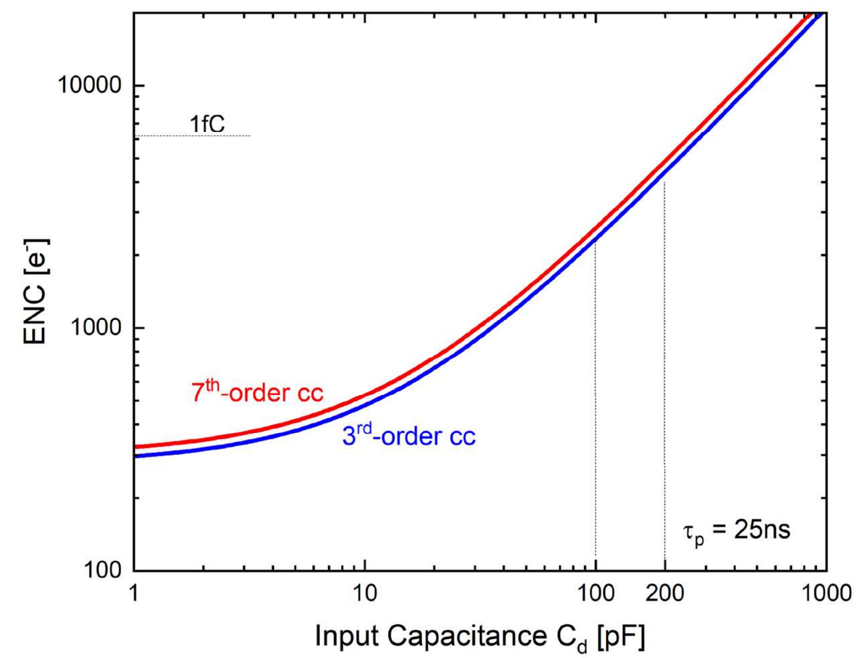


- ADC conversion time < 50ns
- Dead time < 90ns
- D5-D0 shifted at 160MHz DDR in SLVS

Shape Optimization

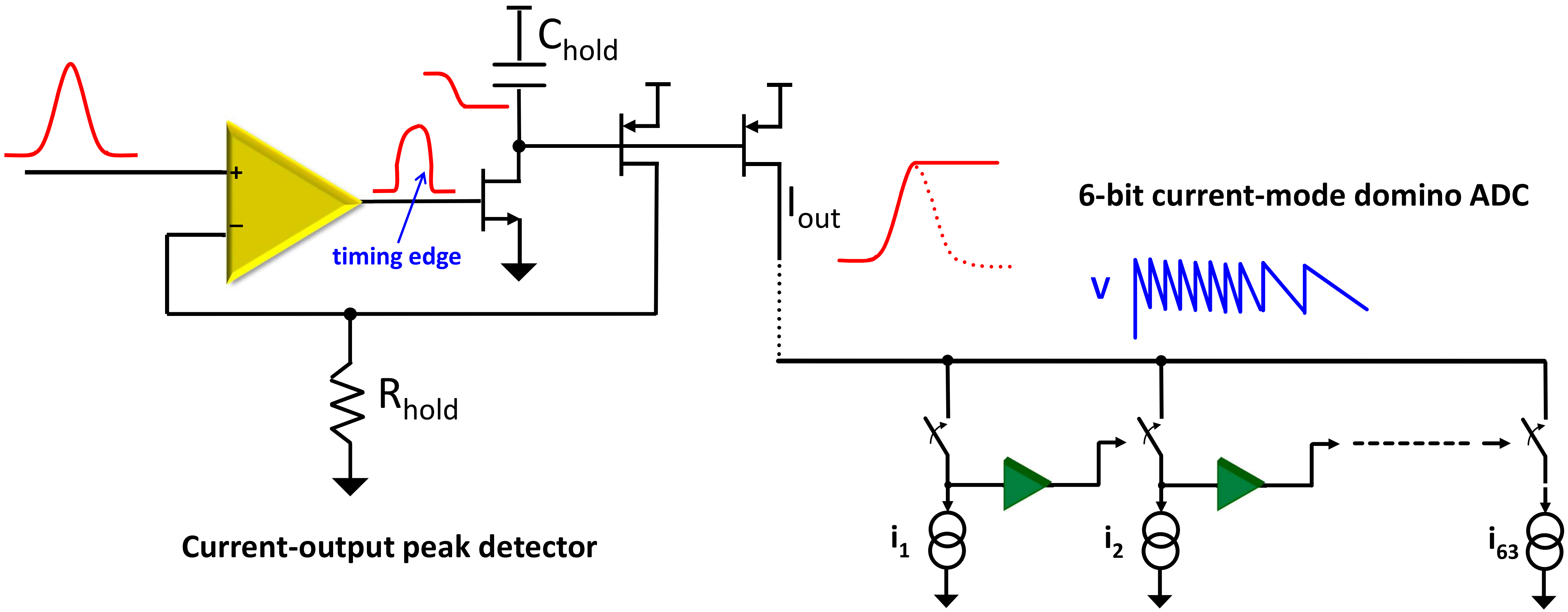






- Very high order low-noise (DDF) shaper → fast return to baseline
- Marginal impact on charge resolution (ENC)
- Improved timing resolution (peak curvature)
- Relevant impact on rate (reduces dead time per charge event)

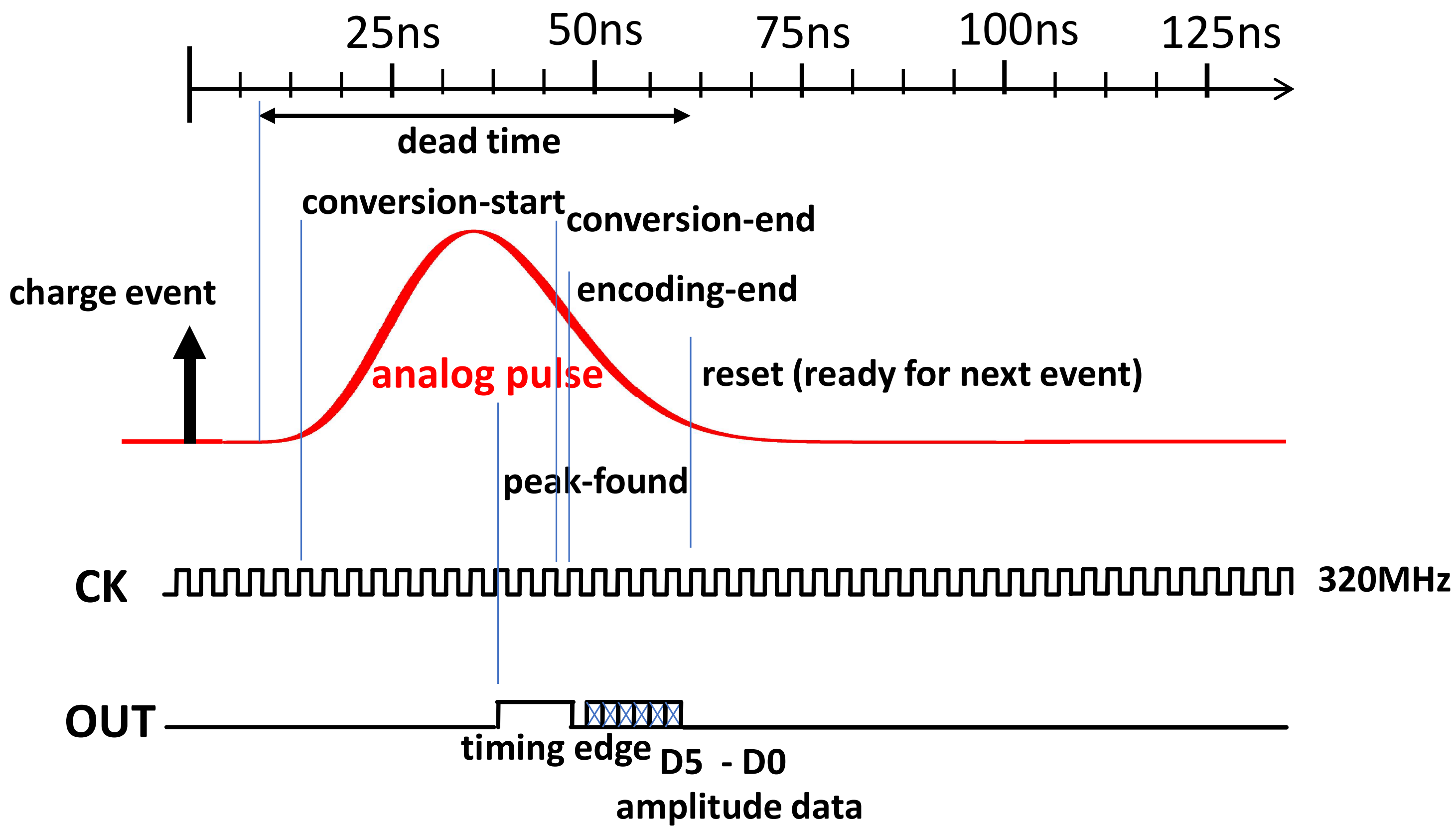
Peak Detector with Current-Mode ADC in VMM



Current-output peak detector

- Conversion starts at beginning of shaped pulse
- Clock-less, low power, high linearity, low noise
- Can be used as peak detector
- Conversion time set by unit currents
- VMM3S: increase unit current by factor 2

Direct Output with VMM3S

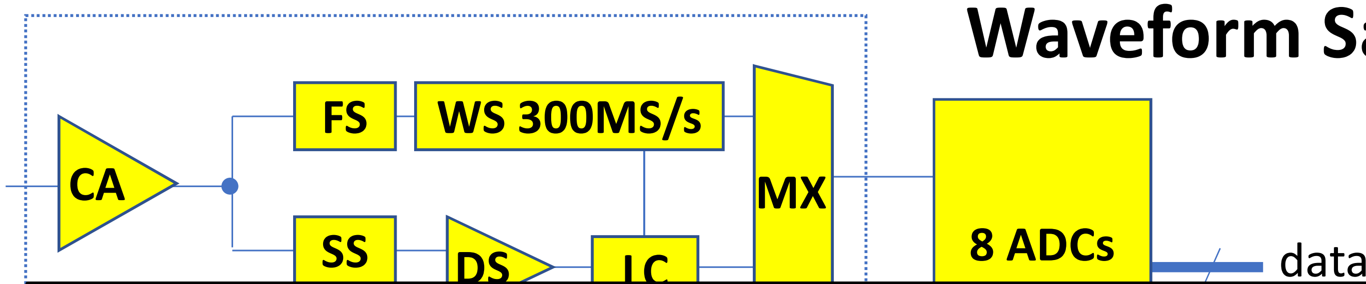


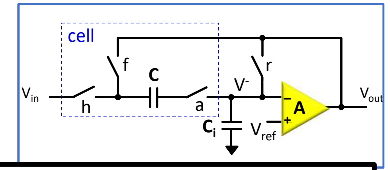
- ADC conversion time < 25ns
- Dead time < 45ns
- D5-D0 shifted at 320MHz DDR in SLVS
- Estimated power increase ~500μW/channel

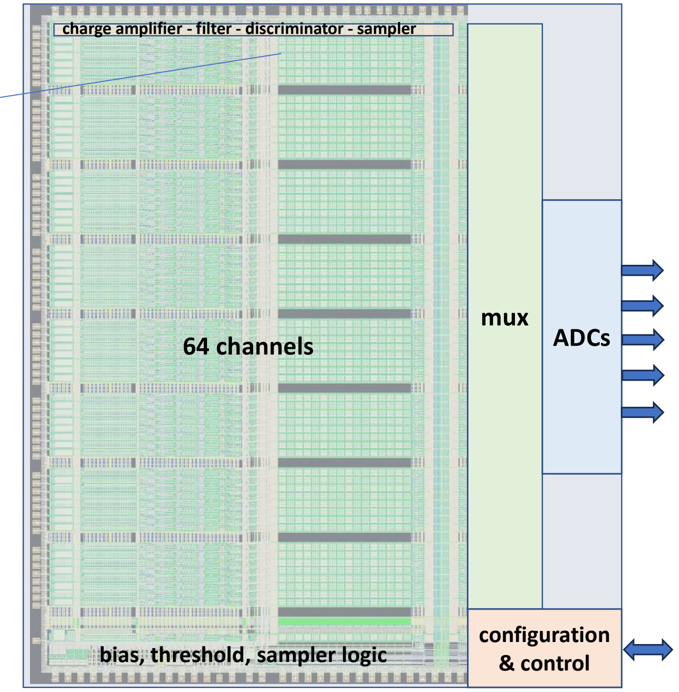
Summary of Planned Modification for VMM3S

Item	Modification	Benefits
Gain	Add gain 64 mV/fC	Matches SoLID maximum charge
Shaping	Increase order to 7th cc DDF	Faster return to baseline, lower noise Improved timing, marginal impact on ENC
6-bit ADC	Increase unit currents	Reduced conversion time to 25ns
Readout clock	Increase to 320 MHz	Increased data rate to 640 Mb/s
6-bit to mux	Option to route 6-bit ADC to multiplexer	Efficient readout at lower rates
Yield issue	Protect from manufacturing issue (exchanges with Global Foundries)	Increase yield from 70% to > 95%
On-demand *fixes and improvements*	In progress	

Waveform Sampling ASIC







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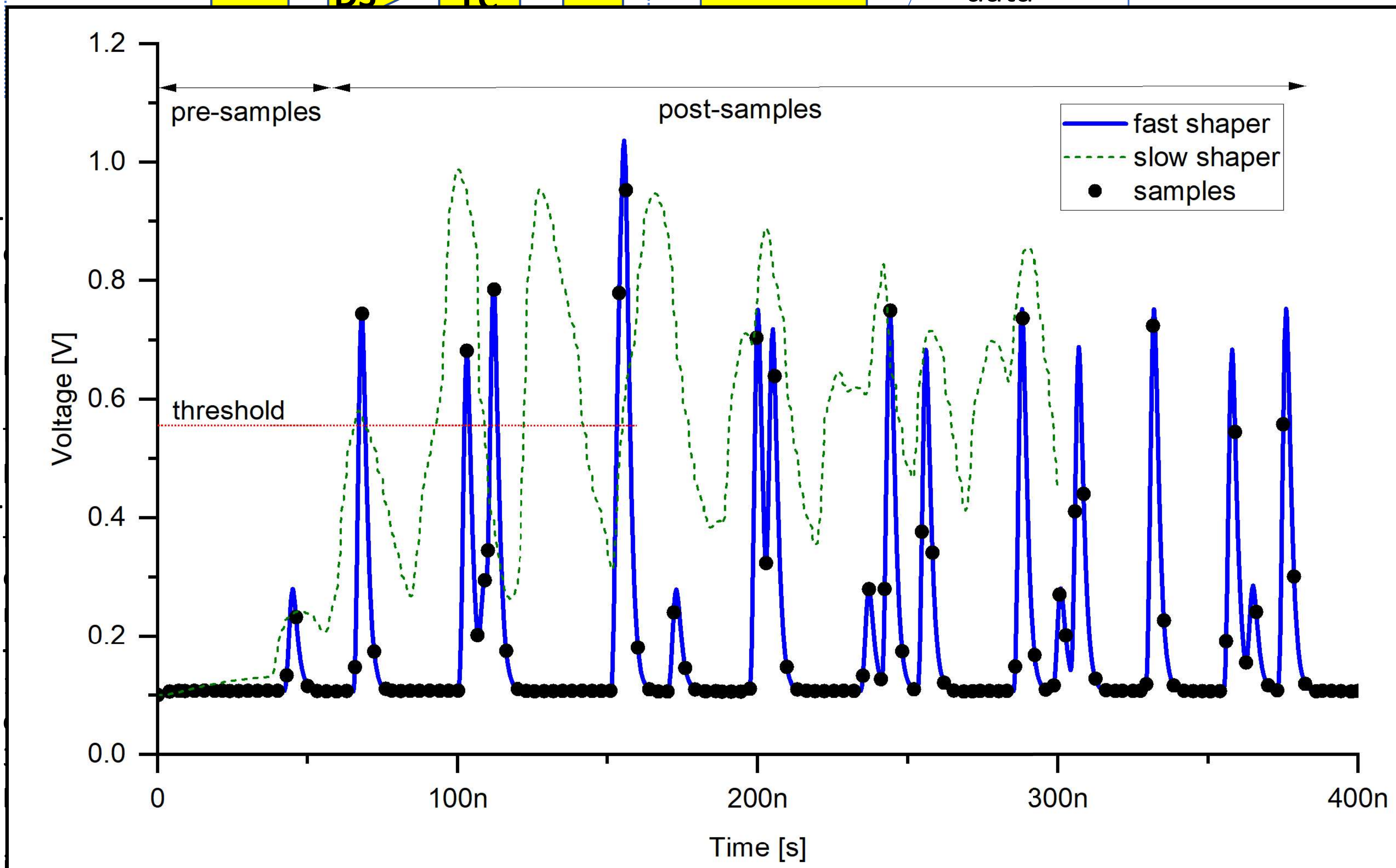


ey Circuits
very high order low-noise shaper in DDF
waveform sampler based on proven
high-precision low-noise architecture
ADC from leading expert

igital Signal Processing
dedicated DSP core with ANN may be
integrated as needed

ey Features
analog zero-suppression
efficient data generation and transfer
highly programmable, flexible design
can evolve to higher event rate
high-resolution and low-power

Next-Generation Custom ASICs for Advanced Gas Detectors

ASIC	Details	Status
VMM3S (SoLID)	An evolution of VMM3a for higher rate	In planning Awaiting funds
Waveform Sampling (SoLID)	Waveform acquisition and digitization ASIC for very high luminosity applications	Advanced conceptual Awaiting funds
VMM4	Migration to 65nm, 128-channels, new ADCs, faster parallel multiplexing interface, new digital core	In discussion
Straw Tube Tracker (DUNE)*	64-channel, dual sub-channel, 10pC, sub-ns at >4fC	In planning Awaiting funds

* Roberto Petti, University of South Carolina

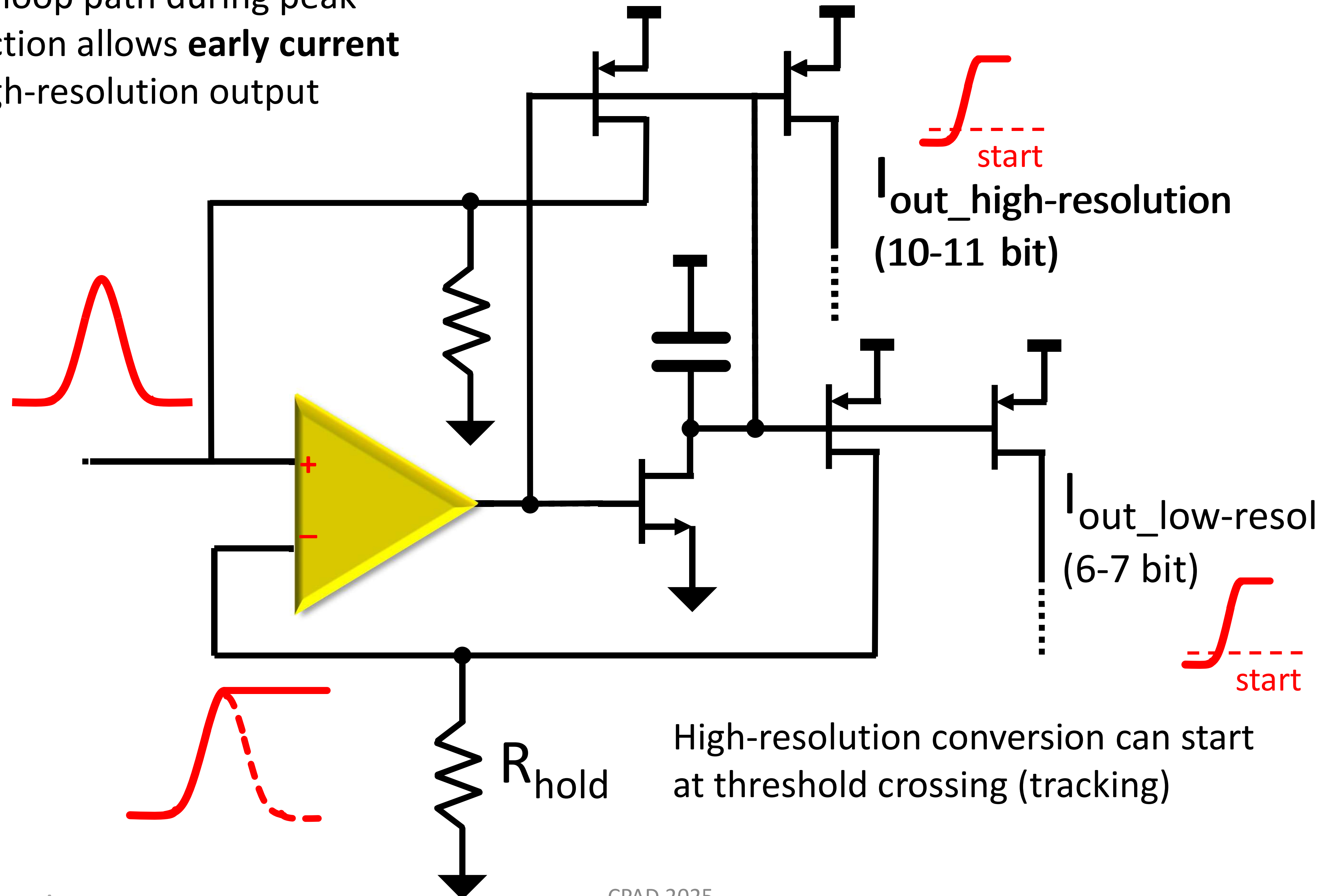
Approach: optimize design efficiency, reduce risk and cost, while pushing technological boundaries

Collaboration model: funding institutions get GDS file and technical support

Backup Slides

Multi-Phase Current Output Peak Detector with Early Current

A off-loop path during peak detection allows **early current** at high-resolution output

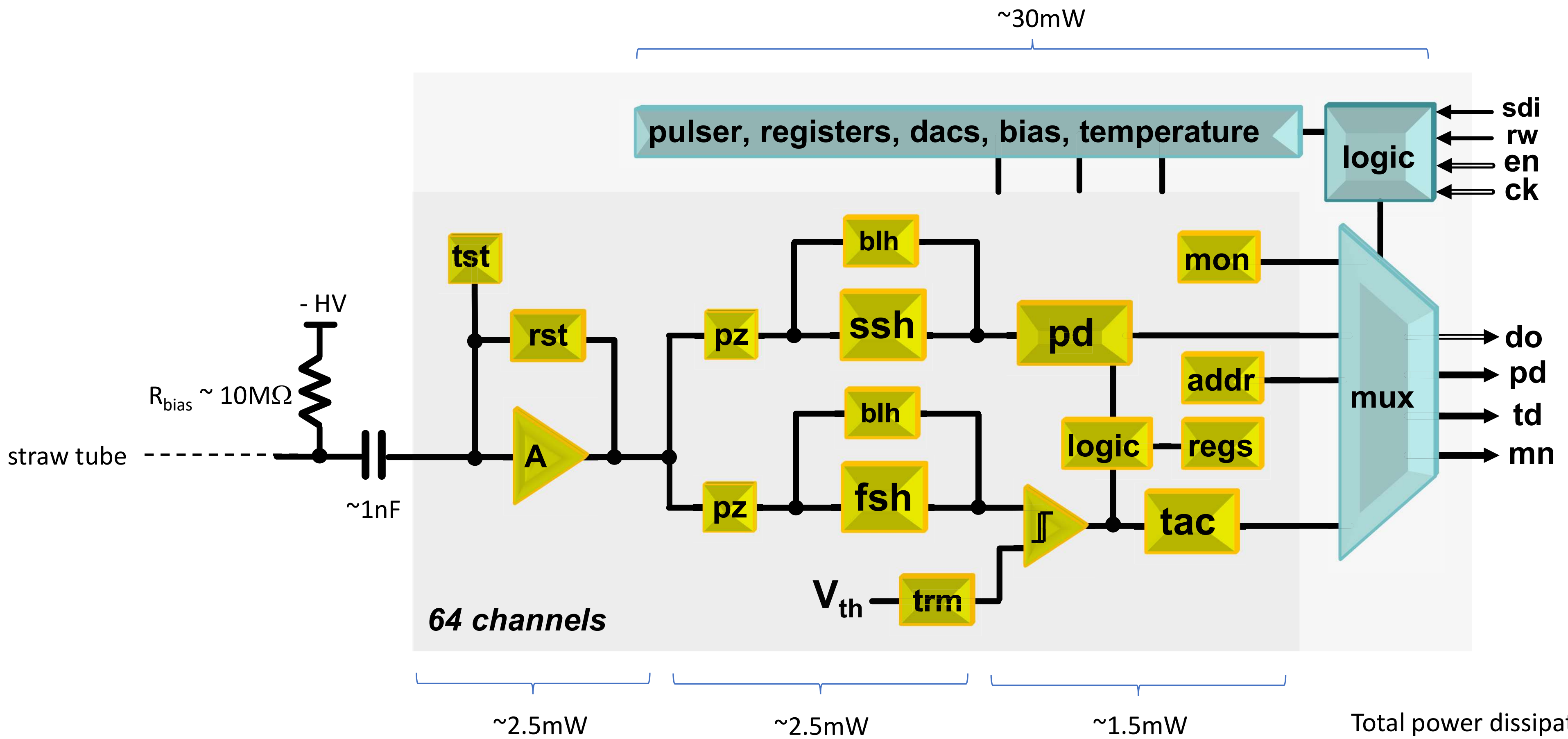


High-resolution conversion can start at threshold crossing (tracking)

ASIC for Straw Tube Tracker (DUNE)

collaboration with Roberto Petti, University of South Carolina

- programmable test pulse generator
- programmable event threshold
- temperature sensor
- circuits based on verified high-resolution architectures



CMOS/LVDS interface for configuration & control with programmable termination

mixed-signal event output:
- data-flag with serialized address
- peak amplitude
- TAC amplitude
- analog monitor

Total power dissipation: 7.5mW x 64 +30mW = 510mW @ 1.8V

- optimized for 50pF
- charge amplifier linear to 10pC
- dedicated front-end supply
- programmable gain
- programmable test capacitor
- continuous adaptive reset

- programmable fast shaper for timing measurement
- programmable slow shaper for charge measurement to 10pC
- high-speed low-hysteresis discriminator with trimmer
- leading-edge timing detection on fast shaper
- timing resolution < 1ns at 4fC
- programmable low-noise time-to-amplitude converter (TAC)
- peak detection on slow shaper

- event flag with programmable delay
- sparse readout with event multiplexing
- programmable analog monitoring
- local registers
- channel power-down