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A readout ASIC on CMOS 28 nm for SiPM/PMT readout at cryogenic temperatures

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Light readout systems with single-photon resolution are essential for next-generation HEP experiments, including dark matter searches, neutrino detectors, and noble liquid experiments. Technologies such as silicon photomultipliers (SiPMs) and photomultiplier tubes (PMTs) offer low noise and scalability, making them well-suited for large-area detector arrays.

This work presents a cryogenic R&D ASIC prototype, fabricated in 28 nm CMOS technology, designed to mitigate signal degradation and reduce background noise in large-scale light readout systems. The ASIC integrates multiple IP blocks, including a front-end readout channel with programmable gain transimpedance amplification, semi gaussian pulse shapers, waveform digitization, and a digital back end with high-speed CML output buffers. The analog front-end features three pulse shaping stages with selectable shaping times (30ns/60ns), offset and bias current trimming, each followed by a 12-bit, 100 MS/s ADC. On-chip, high-speed digitization at cryogenic temperature can simplify system-level design, minimize noise pickup, and improve signal quality, offering significant benefits for future experiments such as XLZD and others. Additionally, the ASIC incorporates on-chip supply regulation with bandgap reference circuits and cap-less LDO regulators, eliminating the need for bulky external decoupling capacitors. This design could not only fulfill the stringent radiopurity requirements of rare-event research but also establishes a path towards scalable, high-performance light readout solutions in future HEP detectors. We describe the design of the first prototype, together with possible future developments targeting cryogenic applications, as well as room temperature applications (e.g., calorimetry).

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