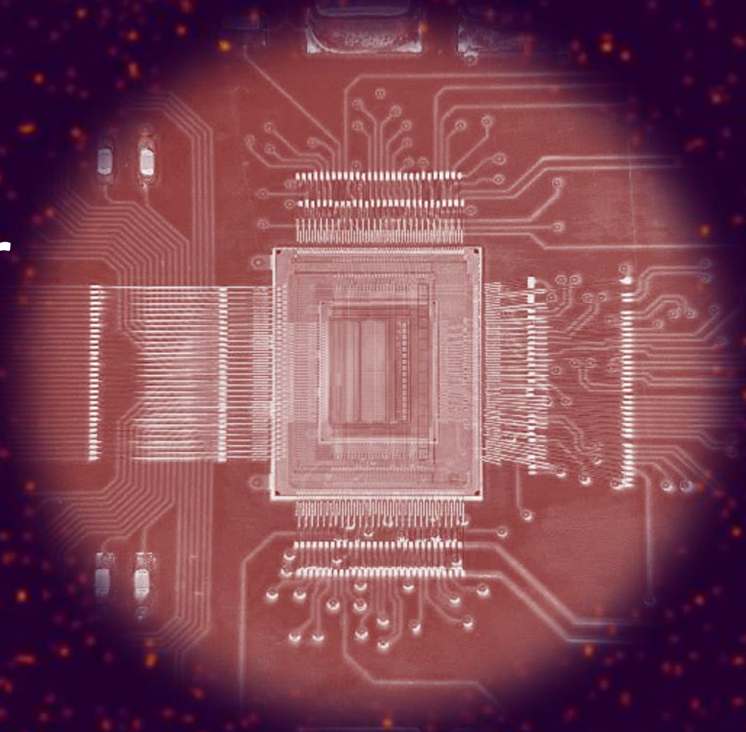
Coordinating Panel on Advance Detectors – CPAD 2025
Inn at Penn, University of Pennsylvania

RDC4 Readout and ASICs

A readout ASIC on CMOS 28 nm for SiPM/PMT readout at cryogenic temperatures



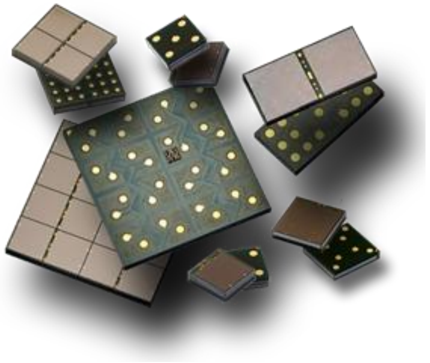
Bojan Markovic
on behalf of SLAC TID-ID IC Department

Oct. 9th, 2025

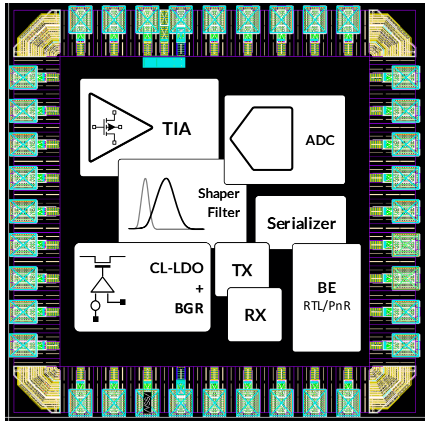
Motivation

Goals of the Photon Readout Systems Development

- **Support** dark matter, neutrino science, and noble liquid detectors in HEP experiments
- **Detect** faint optical signals for rare particle interactions
- **Utilize** SiPMs and PMTs for low noise, fast timing, and scalability
- **Ensure** compatibility with cryogenic environments
- **Enhance** energy resolution for better discovery potential
- **R&D prototype** integrating analog and digital IPs in 28 nm CMOS



R&D prototype



Potential science case

- **XLZD** - Next generation liquid xenon observatory for dark matter experiment and neutrino physics [1]

[1] - The XLZD Design Book - https://arxiv.org/pdf/2410.17137

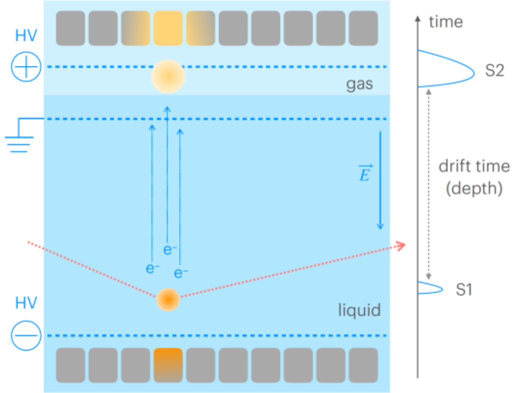
XLZD Signals

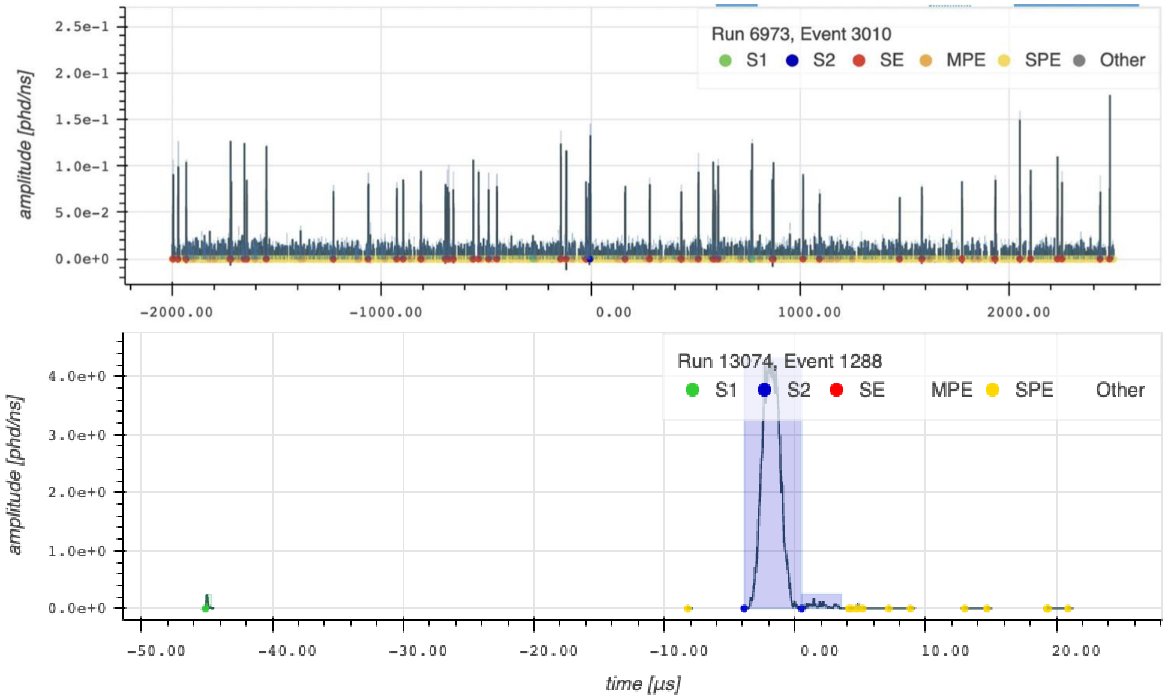
Detection principle:

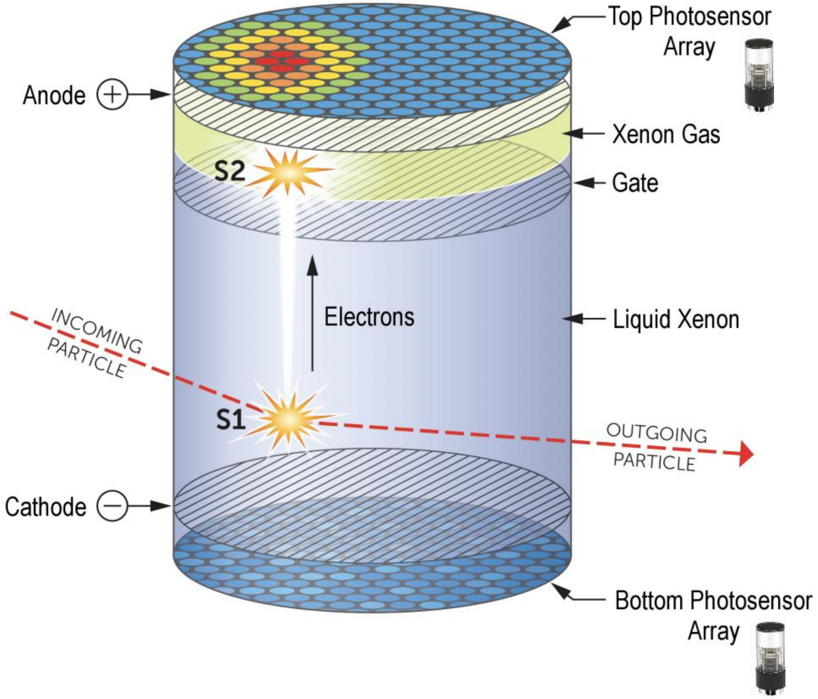
- Particles interact with xenon and produce two light signals: **S1 + S2**
  - S1 signal is typically ~100-200 ns wide, S2 is ~1 us
- Variable event size
  - Maximum time difference between S1 & S2: ~1500 us (event windows of ~5ms or longer)

Goal of this development:

- **Detect/digitize** S1 & S2 signals from particle scatters along with smaller signals near the main event



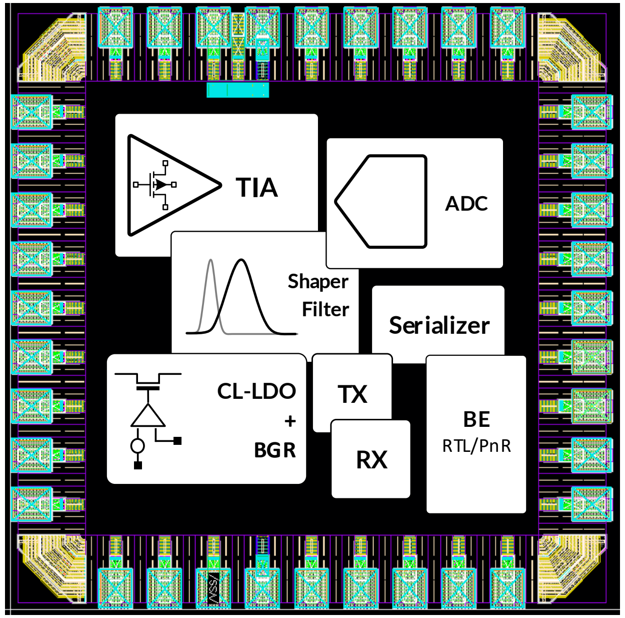




- TPC in early stages of detector design
- 3 m tall filled with ~40-80 tonnes of LXe
- PMT arrays on top (~1000) and bottom (~1000)

IC Design Challenges

- Specialized readout electronics in cryogenic environments
- Fast digitization under strict power constraints to prevent LXe bubbling
- Large dynamic range: single to ~10^4–10^6 p.e. from PMT/SiPM signals
- Strict radiopurity requirements for LXe environment
- Limited voltage headroom in advanced CMOS
- Low-noise electronics for high SNR
- Programmability and testability due to lack of transistor models



Technology Choice: TSMC 28nm CMOS Process

Technical motivation:

- Next-gen CMOS node identified by HEP community
- Good performance at cryogenic temperature
- Almost mandatory to support advanced on-chip data processing and data reduction: digital > analog

Transistor Models:

- Not currently available → Foundry models extrapolated down to 160 K
- LBNL and SLAC are collaborating to develop a Cryo-PDK for core devices (see Brian's talk, ID#183)

Advanced node is attractive for graduate students; we have noticed great engagement over the past years:

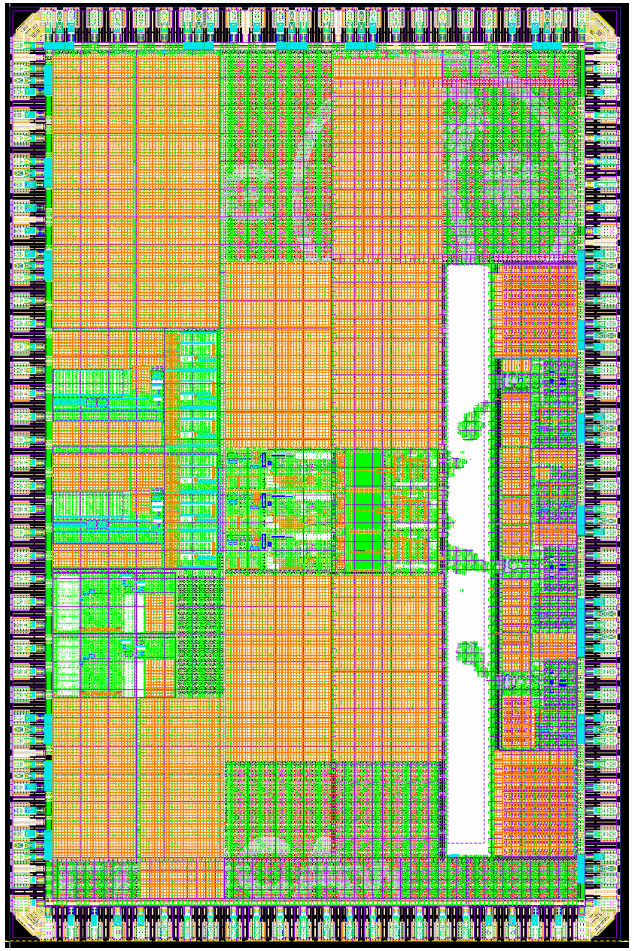
- Victor Turbiner (ex-HEPIC, graduate student at SLAC/Stanford)
- Kevin Boateng (ex-HEPIC, Stanford)
- Marissa Hsu (ex-HEPIC, Stanford, now with Boeing)
- Will Johnson (ex-HEPIC, Stanford)

Specifications

Technology	CMOS 28 nm
Supply voltage	1.6 V – FE readout 0.9 V – ADC, digital backend, output drivers
Temperature	300 K → 160 K (LXe regime)
Min. signal | Max. signal	1-2000 photo-electrons @ PMT/SiPM gain 1e6
x3 channel gain (parallel readout)	High-Gain x1 Medium-Gain x1/40 Low–Gain x1/400
Filter	Semi-gaussian with 30/60 ns shaping time
Signal-Noise-Ratio @ 1 ph. el.	50 @ 300 K | 60 @ 160 K
On-chip digitization	100 MSps sampling rate, 12-bit resolution
On-chip supply regulation	Optional at 1.6V, on-chip band-gap reference generation
Fast I/O drivers	CML standard operating at 10 Gbps
Power consumption	< 50 mW / channel

PHOCA v1

PHOton
Cryogenic
ASIC



PHOCA v1: top-level layout sent for fabrication in July

IPs developed on CMOS 28nm

Designed for operation at room and/or cryogenic temperature

IPs developed as part of KA25 in 2025:

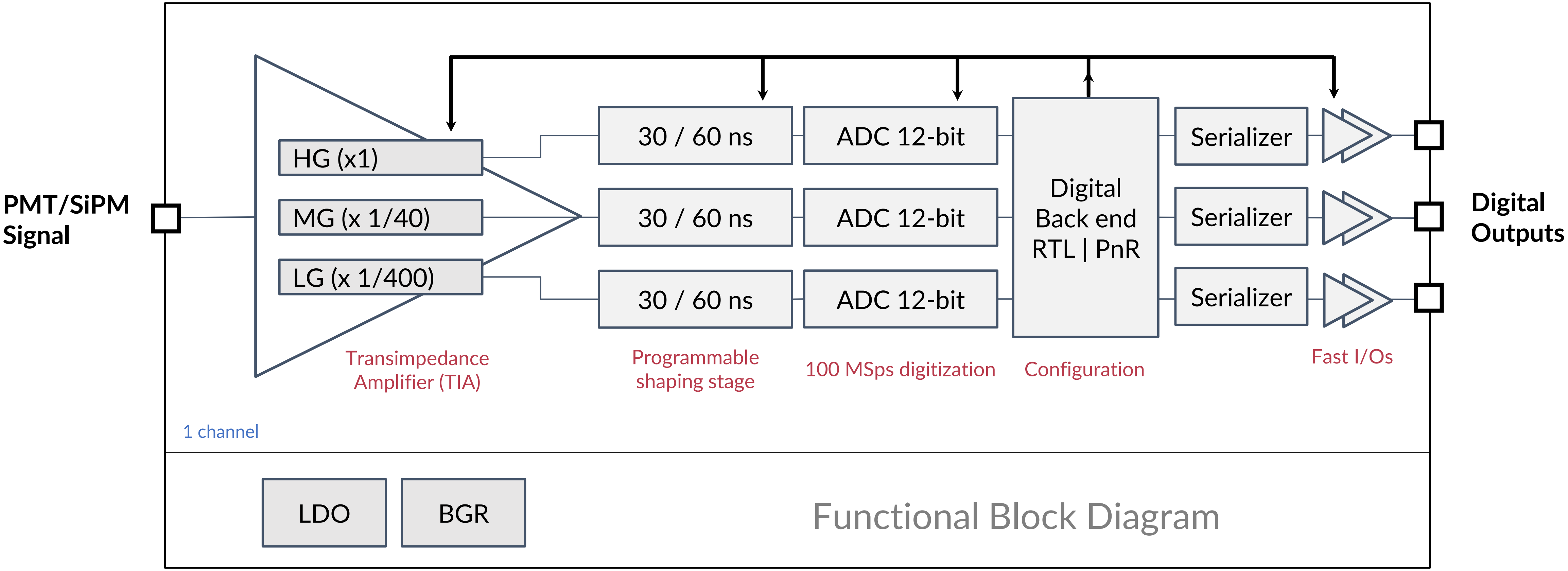
[*] HEPIC intern

- Transimpedance amplifier (TIA) for PMT/SiPM readout (IC team, M. Hsu)
- Semi-gaussian shaper (IC team)
- 100 MS/s, 12b Analog-to-Digital converter (IC team, K. Boateng)
- High-speed serializer, input/output CML drivers (IC team)
- Bandgap reference (BGR) circuit (IC team, BUAP)
- Low dropout (LDO) capacitor-less voltage regulator (IC team, BUAP)
- Top-level integration (IC team, V. Turbiner)

Existing IPs from previous years / other projects:

- Low-power, small-area Time-to-Digital converter with 6 ps res. (pixel detectors)
- Custom cells for SRAM-based In-Memory Computing (IMC)
- Embedded FPGA

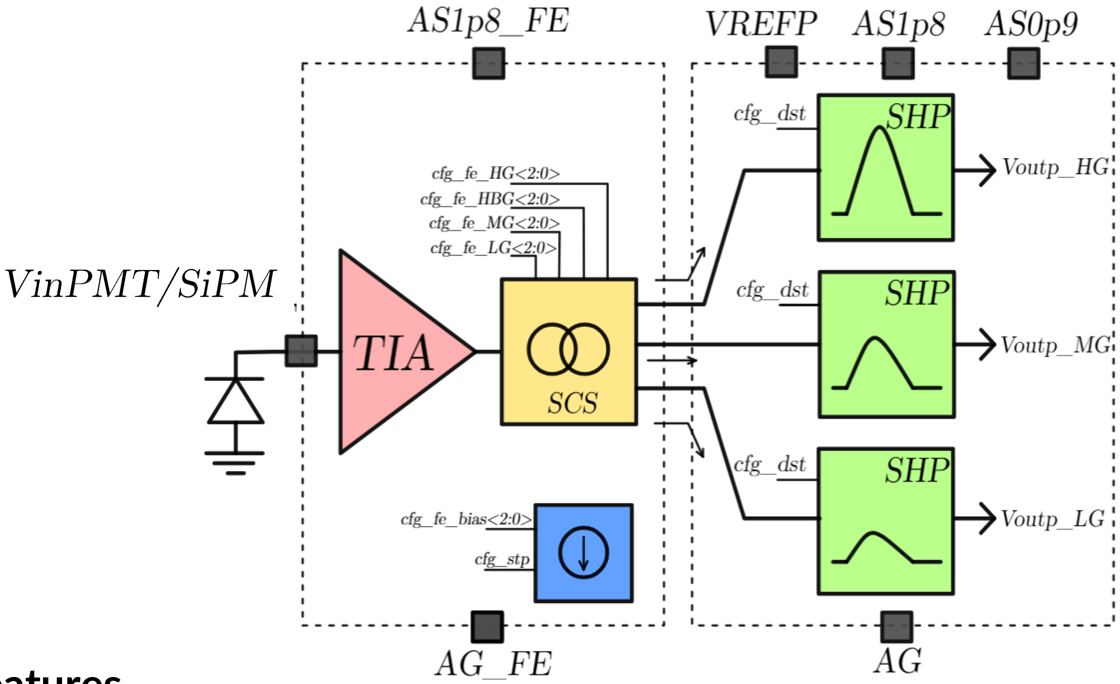
Readout ASIC on 28nm CMOS

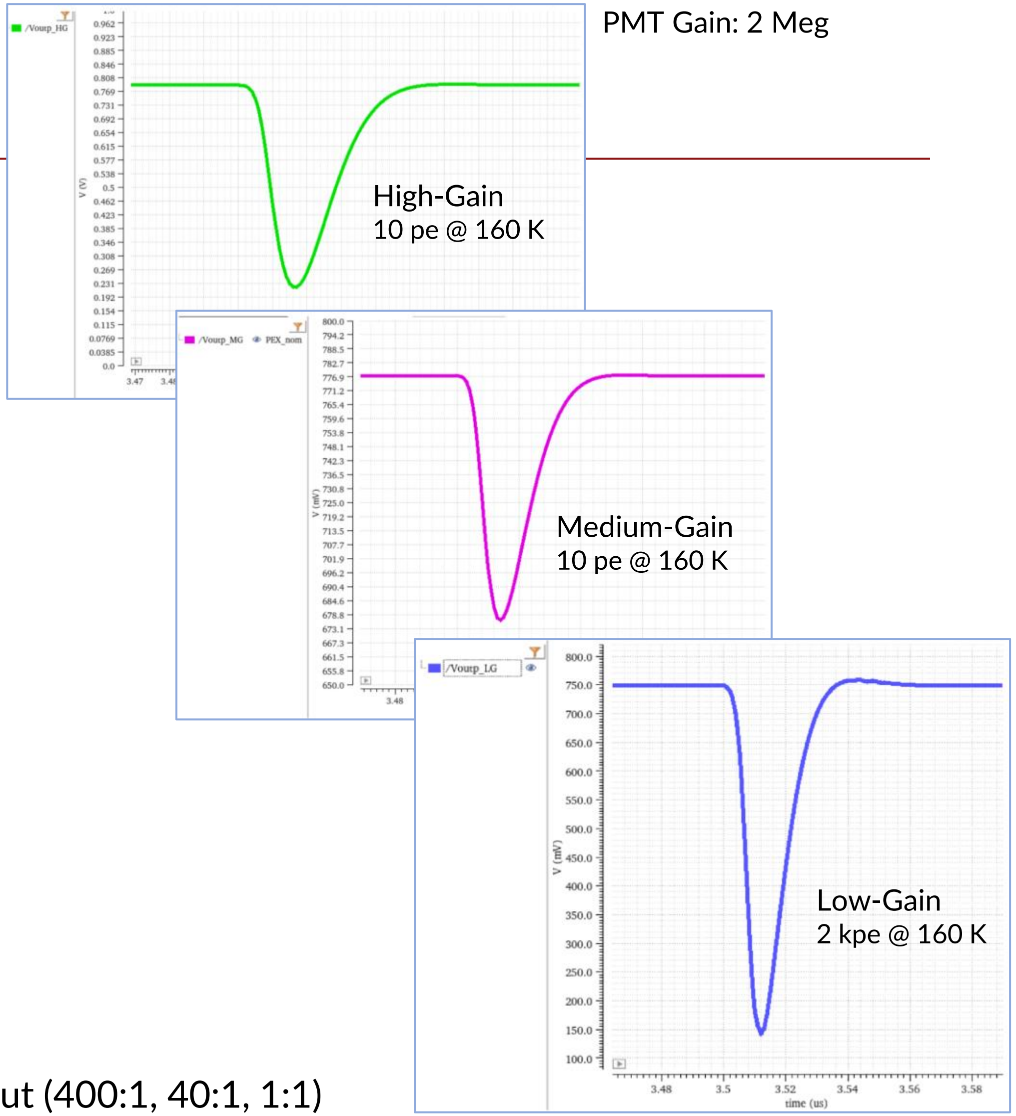


- Target specifications derived from potential upgrade of PMT readout in XLZD experiment
- Collaboration with XLZD partners will help characterization efforts at cryogenic temp in real experimental setup

Readout ASIC on 28nm CMOS

Front-End Channel



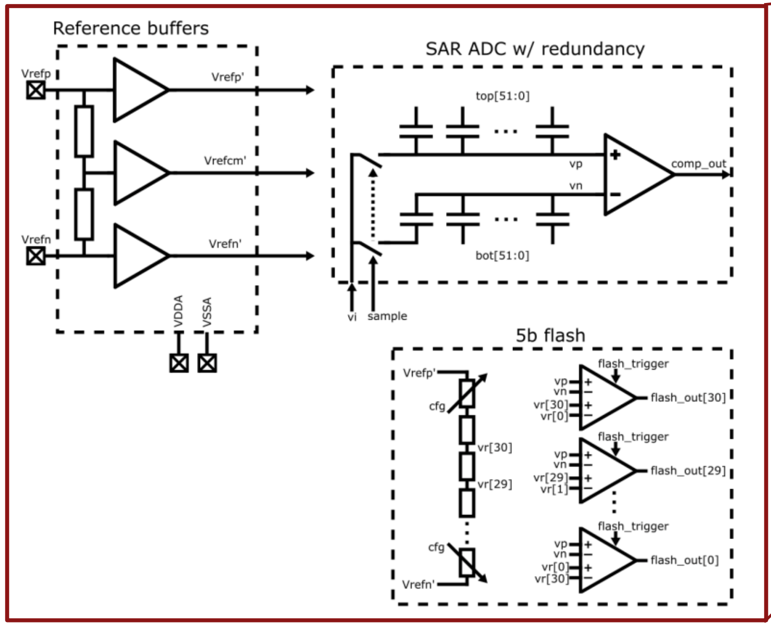


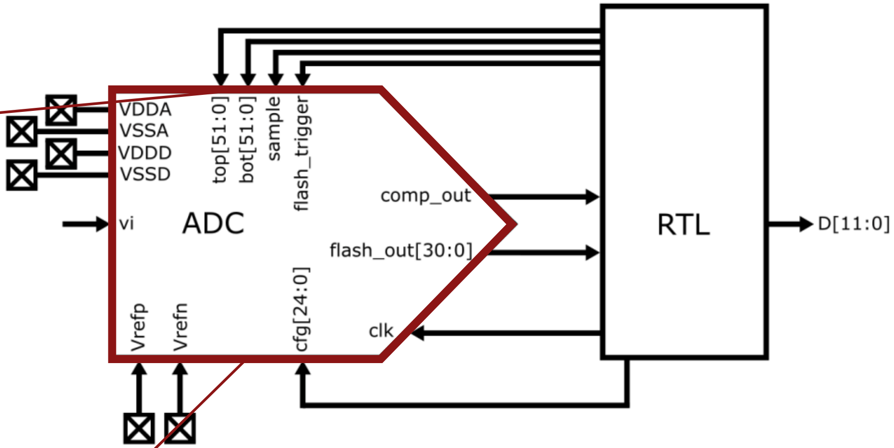
Key features

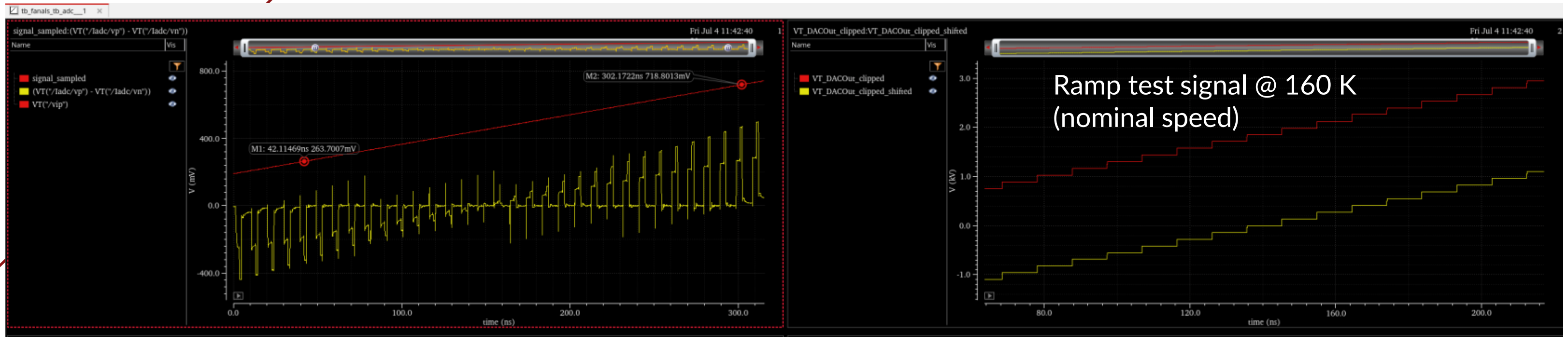
- **Transimpedance Amplifier (TIA):** Converts input current into voltage
- **Current Signal Scaling (CSC):** Generates three scaled copies of the TIA output (400:1, 40:1, 1:1)
- **Semi-Gaussian Shapers (SHPs):** Three-pole low-pass filters producing semi-Gaussian pulses to limit bandwidth and improve SNR
- **Programmable settings:** Bias, shaping time, baseline and gain to optimize operation and performance at cryogenic temperatures

Readout ASIC on 28nm CMOS

A/D Converter





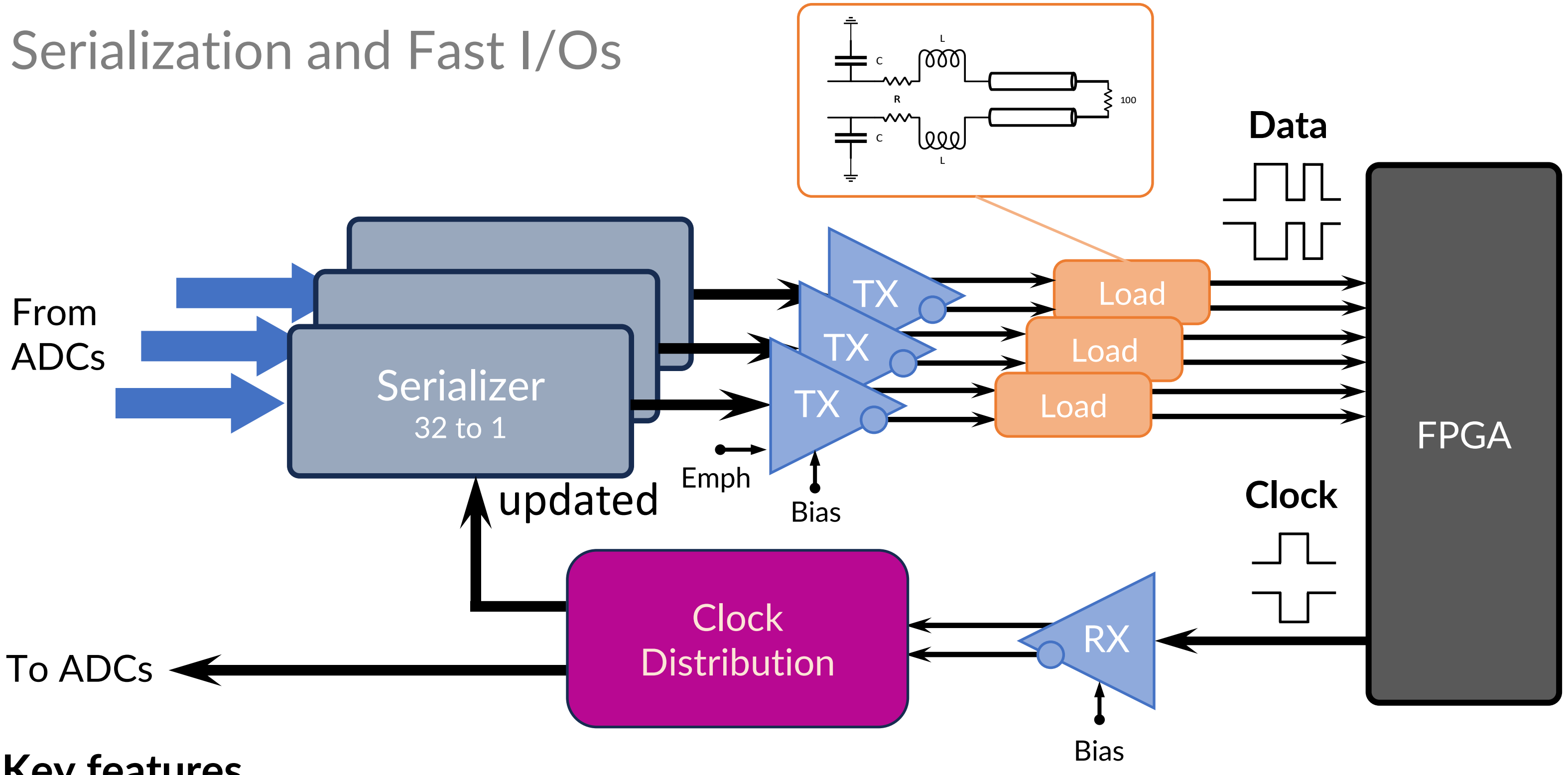


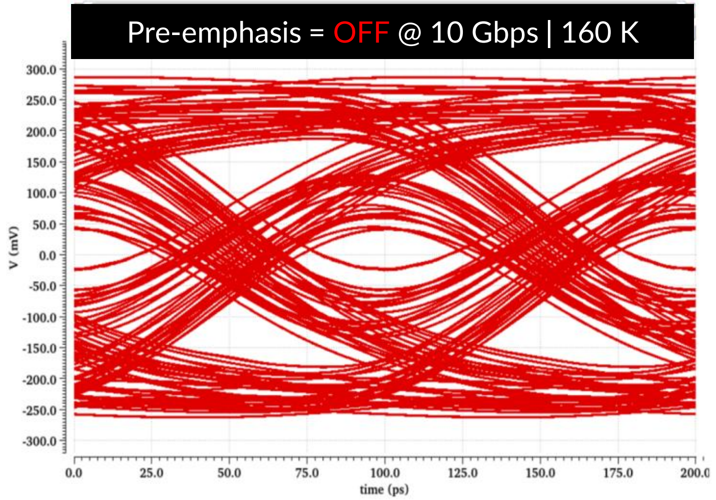
Key features

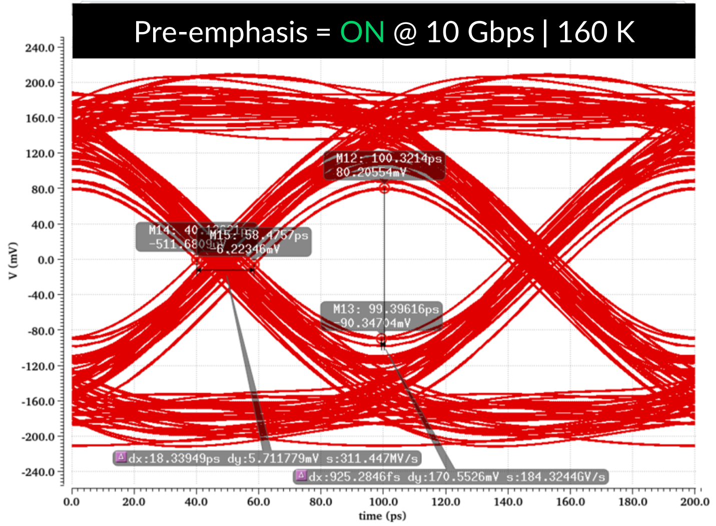
- **Hybrid 12-bit ADC architecture:** 7-bit SAR + 5-bit Flash
- **High-speed operation:** 100 MSps sampling rate
- **On-chip reference:** Three reference buffers provided
- **Programmable settings:** Bias, reference signals and dynamic range to optimize performance at cryogenic temperatures

Readout ASIC on 28nm CMOS

Serialization and Fast I/Os





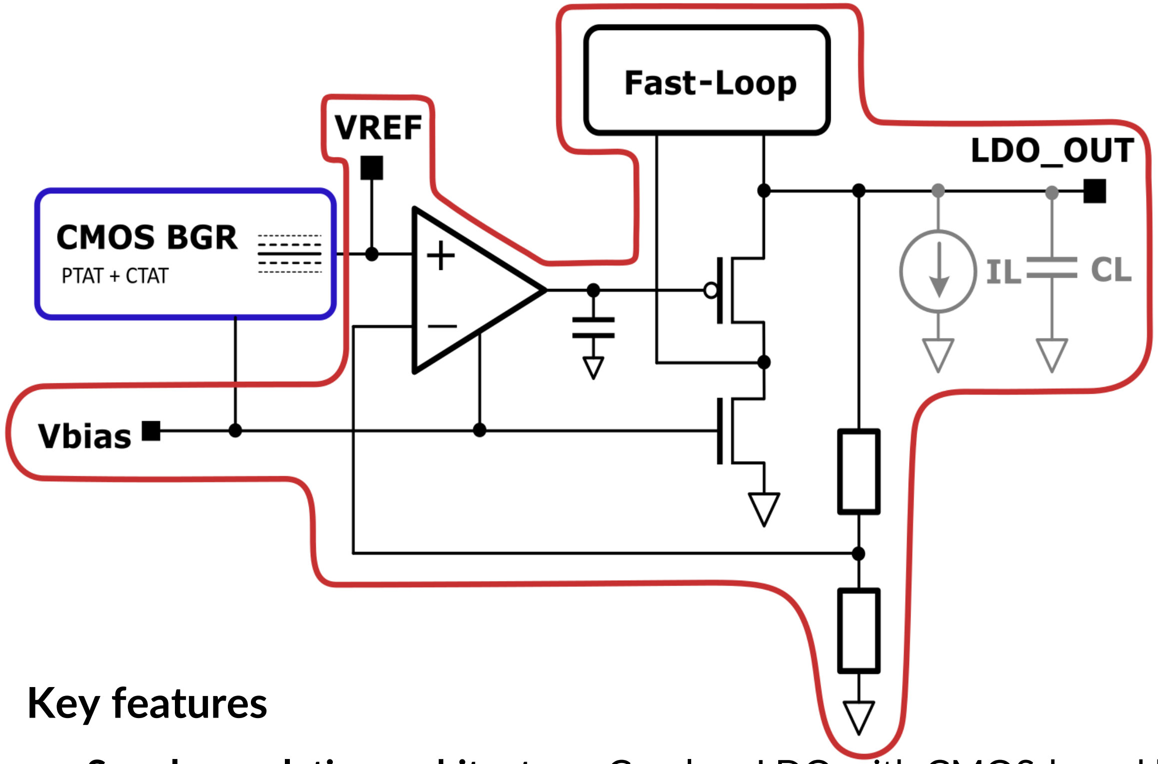


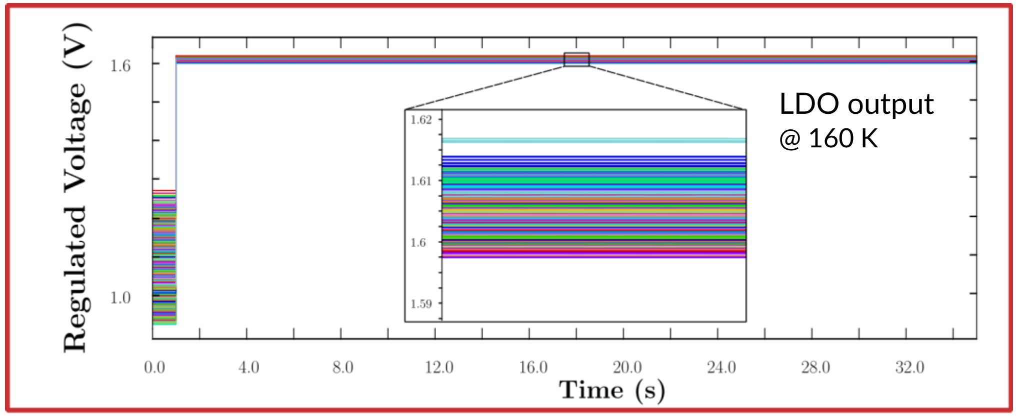
Key features

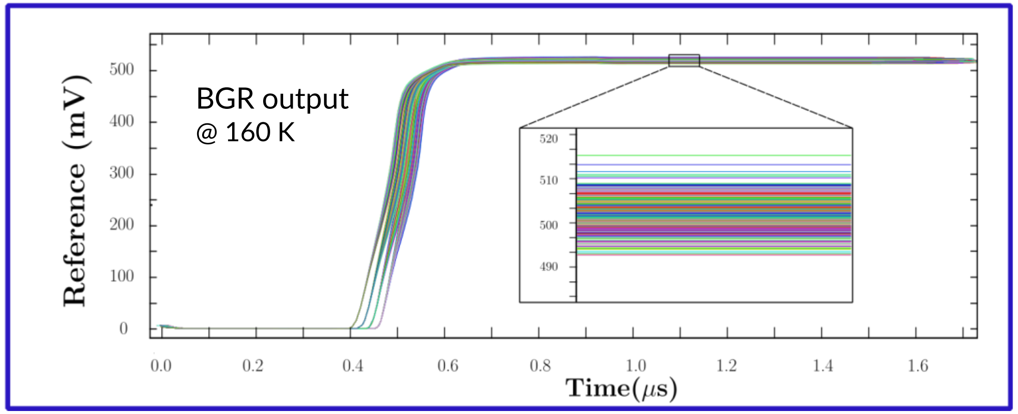
- **TX architecture:** CML standard with pre-emphasis for 10 Gbps operation
- **RX architecture:** CML standard
- **Serializer:** 32-to-1 full custom design
- **Programmable settings:** Bias and pre-emphasis circuitry to optimize performance at cryogenic temperatures

Readout ASIC on 28nm CMOS

On-Chip Supply Regulation





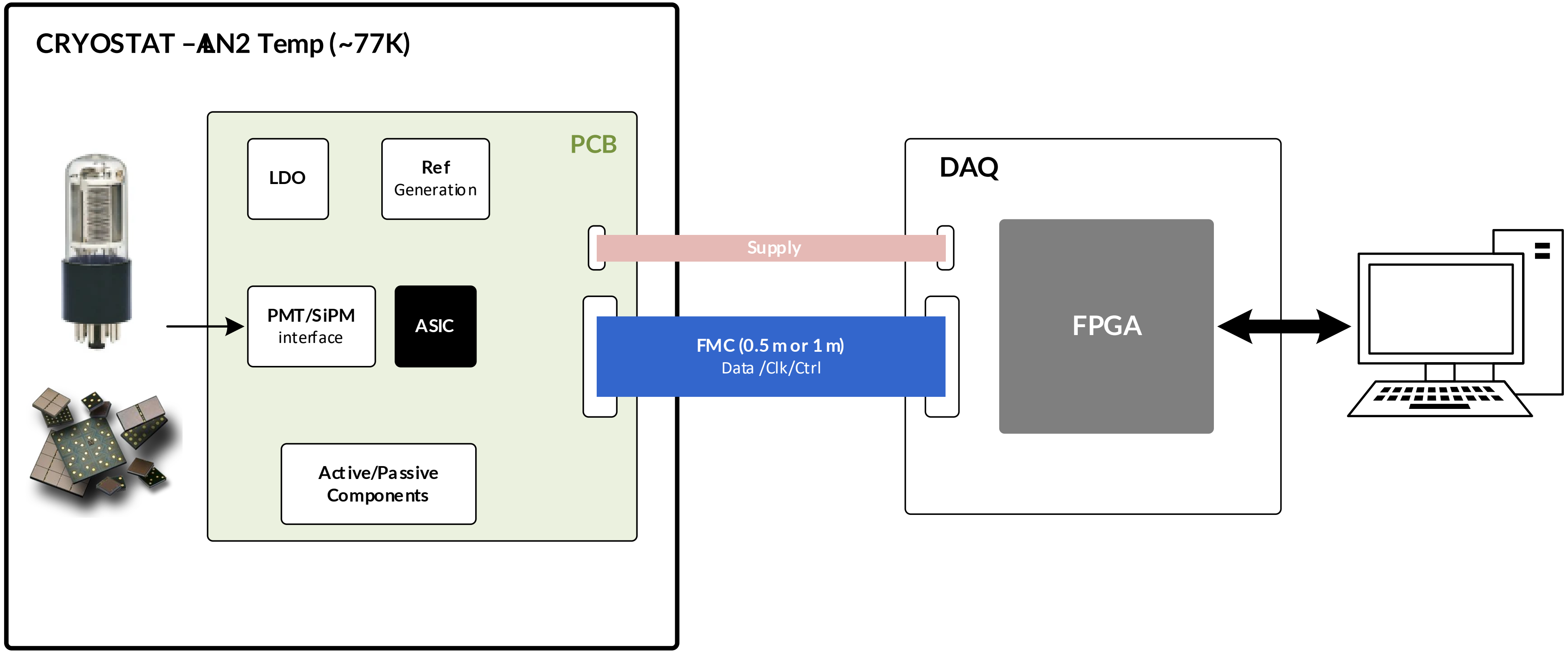


Key features

- **Supply regulation architecture:** Cap-less LDO with CMOS-based bandgap reference
- **Supply voltage:** 1.6 V @ 50 mA load
- **Reference signal:** 500 mV (programmable)
- **Programmable settings:** Bias and bandgap reference voltage to optimize performance at cryogenic temperatures

Next Steps

System Level



- Expected delivery of the PHOCA chips: **Middle October**
- In progress: PCB design, DAQ/firmware

Acknowledgments

Thanks!

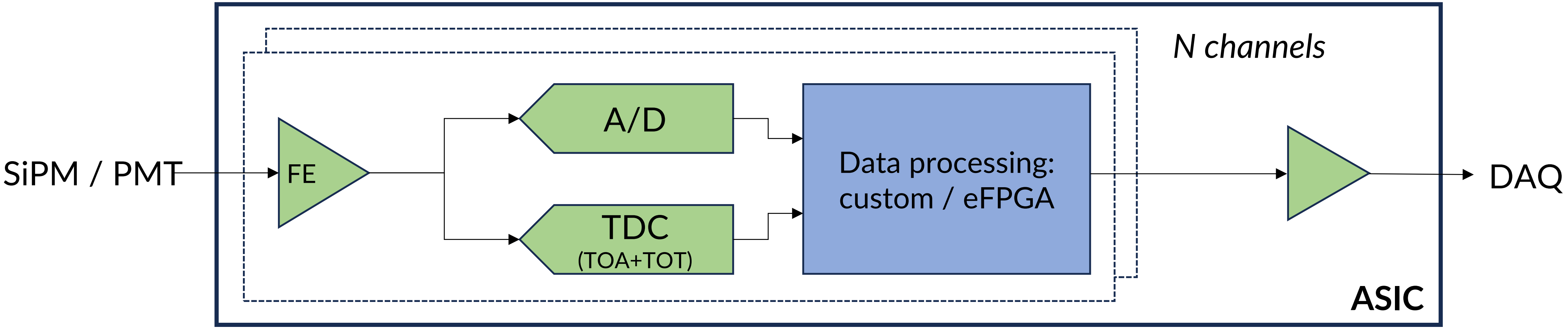
Q/A

Contact info:

- Hugo Hernandez Herrera (hdhernan@slac.stanford.edu)
- Llorenc Fanals-i-Batllori (fanals@slac.stanford.edu)
- Aldo Pena Perez (aldopp@slac.stanford.edu)

Backup

Next-gen Photon Readout ASIC: Next Steps in FY26



- Key Analog/Mixed-signal IP blocks designed, will be characterized
- Identify on-chip data processing challenges/needs for future detectors in collaboration with partners, *e.g.*: energy/timing reconstruction with multiple signals
- Since data processing algorithms are experiment-specific, our KA25 efforts will focus on technological R&D:
  - eFPGA for general-purpose, re-programmable logic: both AI/ML & “traditional” logic
  - Port algorithms from collaborators to custom “hard-coded” RTL and evaluate performance
  - SRAM-based In-Memory Computing architecture