

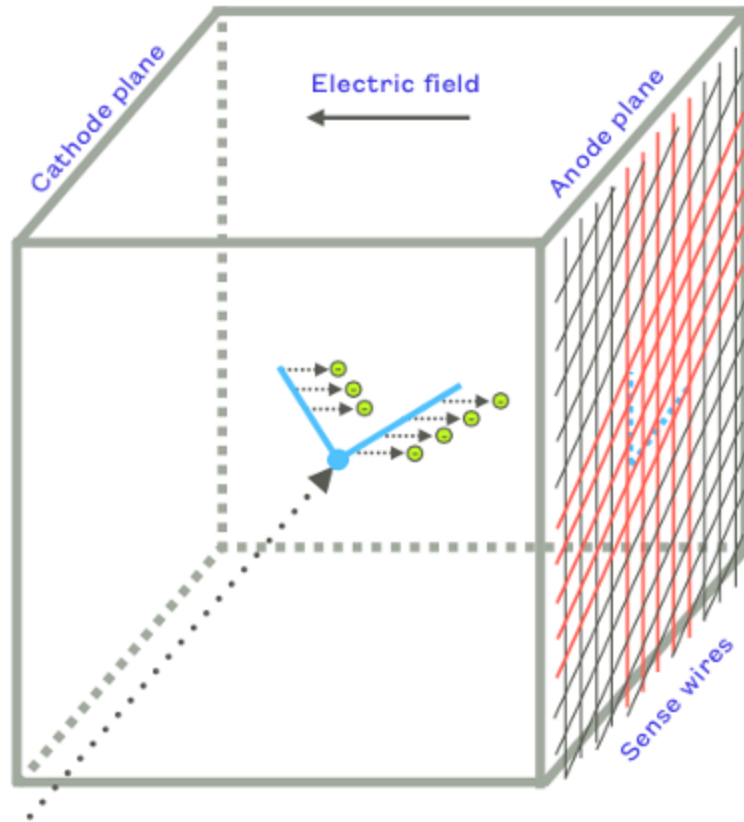
LArPix Pixelated Charge Readout System

Brooke Russell on behalf of LArPix

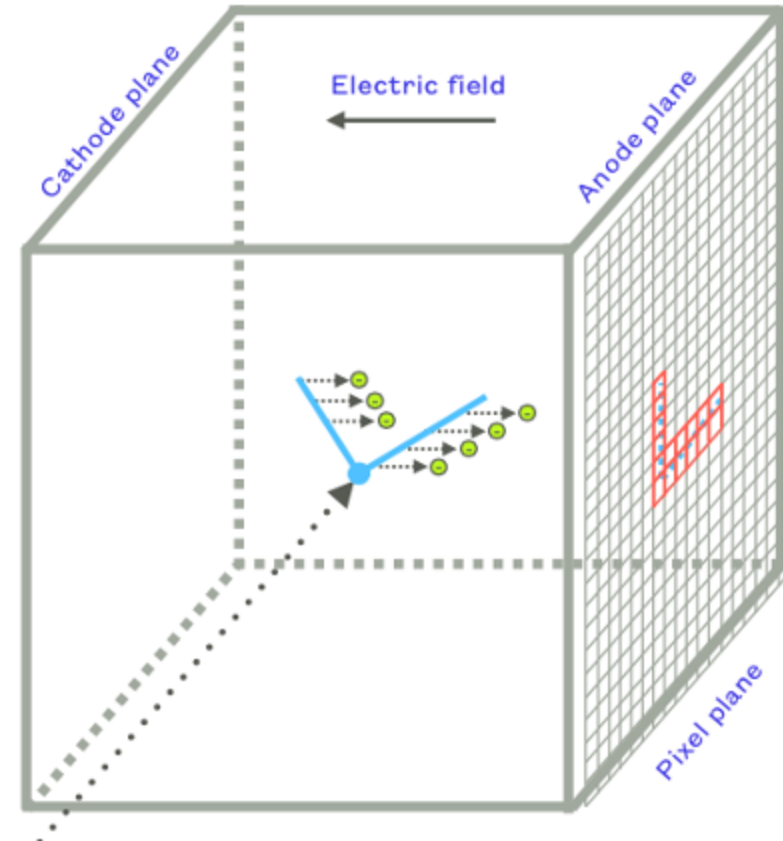
Coordinating Panel on Advanced Detectors @ Penn

October 9, 2025

Liquid Argon Time Projection Chamber Ionization Sensing

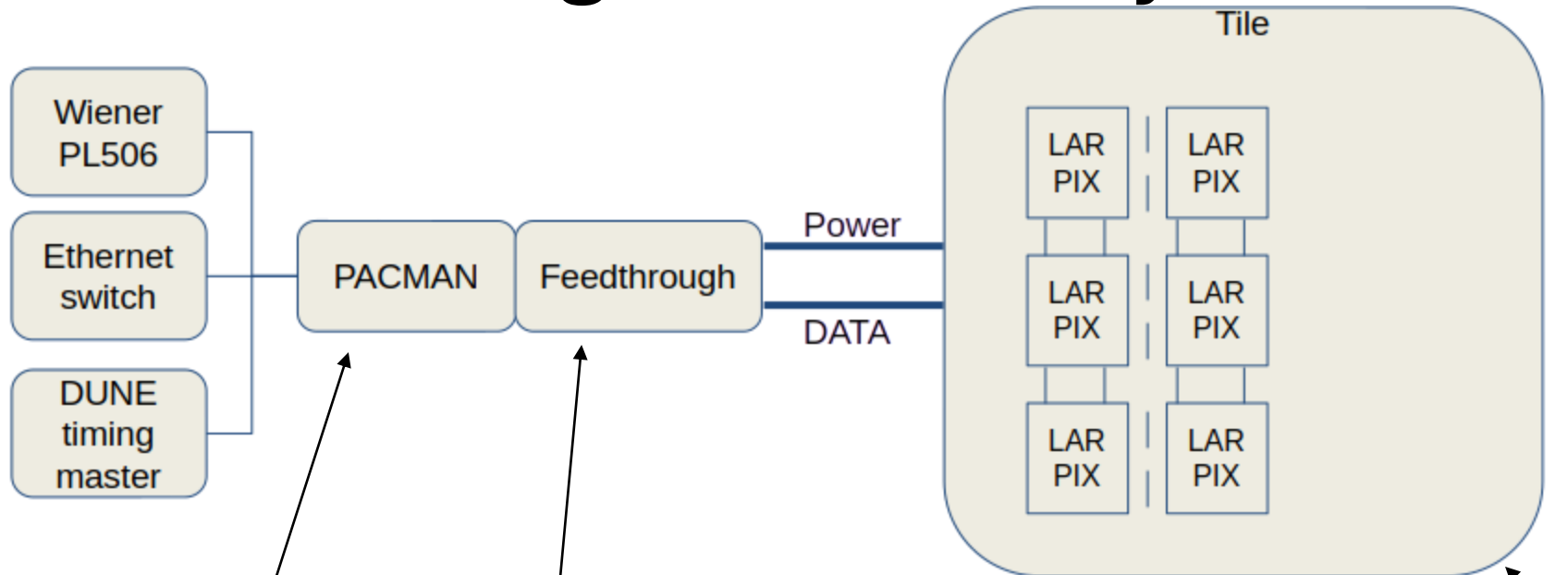


Traditional projective readout with wires or strips



Anode pixelization for native 3D readout

LArPix Charge Readout System-level Design



LArPix Hydra network enables redundant data transport on and off tile. No single point of failure.

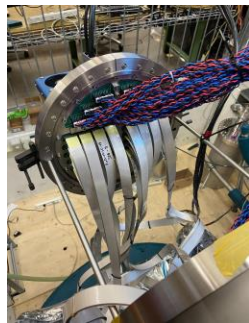
Distributed data buffer minimizes throughput requirements.

Network topology can be chosen to minimize buffer usage or latency.

COTS or externally supplied



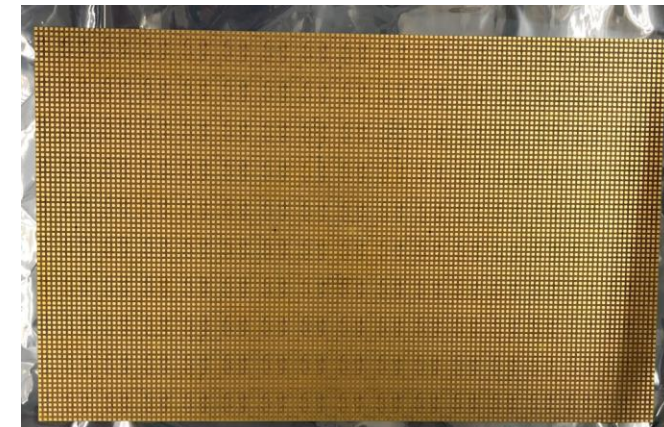
Low voltage, low complexity design, use of COTS FPGA module



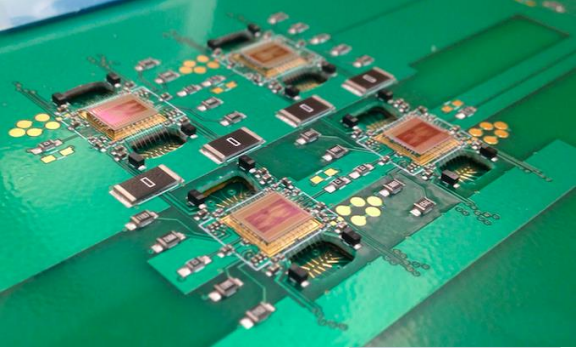
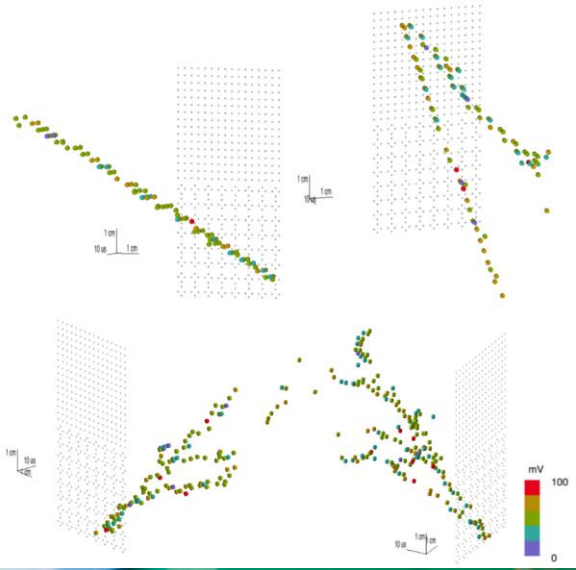
Passive, low complexity PCB

Low data rate enables use of simple ffc cables

Standard PCB technology leverages industry pricing, production, assembly capability



LArPix Evolution



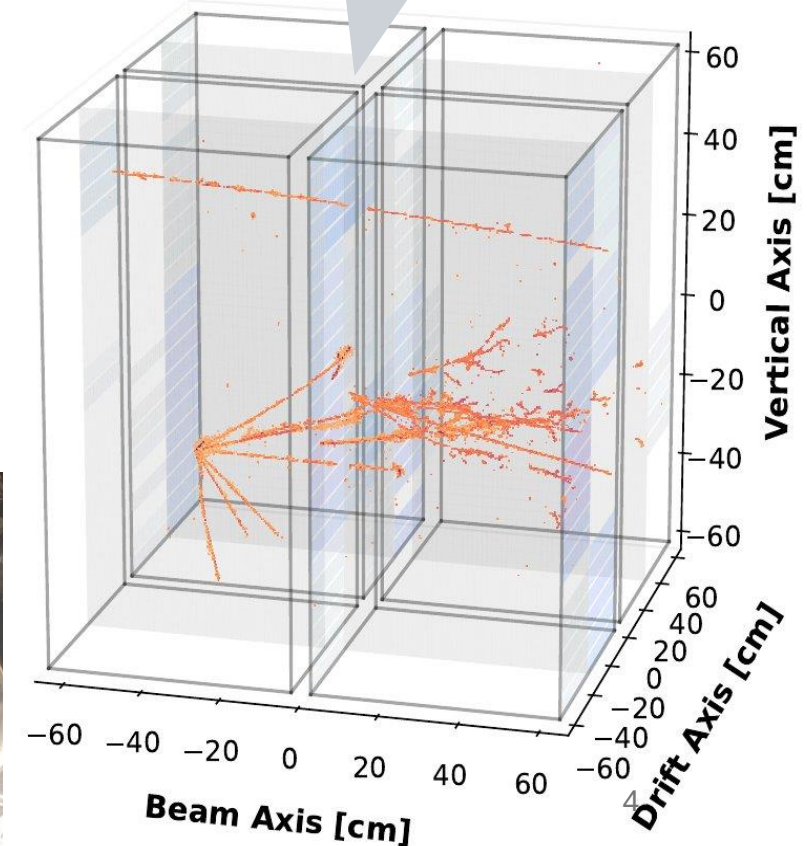
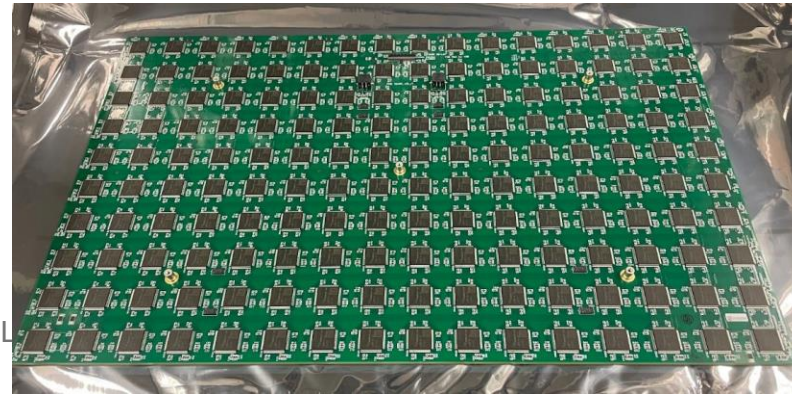
LArPix-v3, 2025-

LArPix-v2, 2019-2024

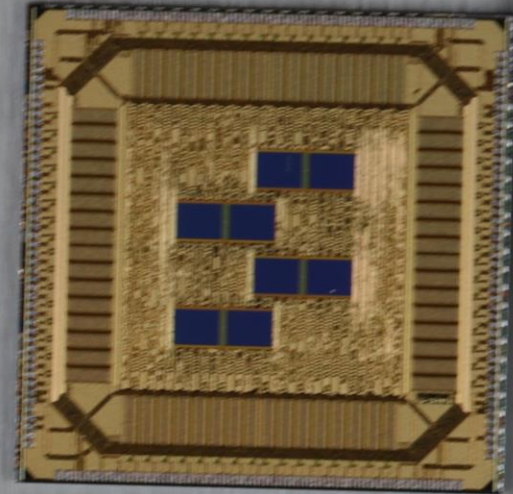
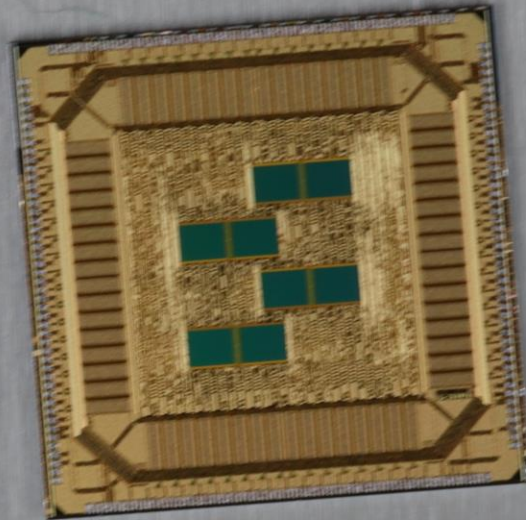
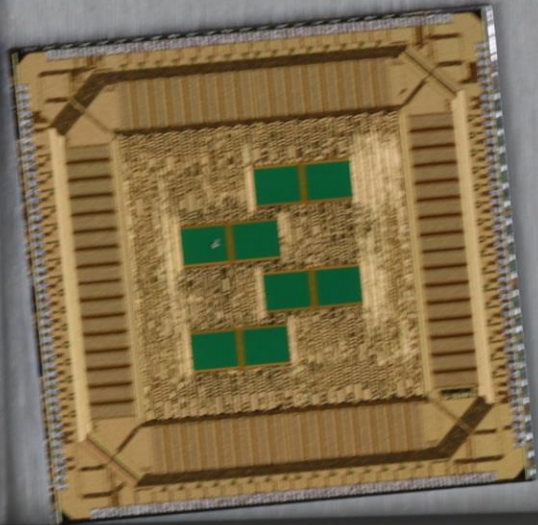
- 400k channel systems with 3.72 mm pixels
- >10k digital multiplexing
- 500 e- ENC @ 87K
- Demonstrated industry-produced, scalable system architecture

LArPix-v1, 2016-2018

- $O(10^3)$ channel readout via 2 wires
- 275 e- ENC @ 87K
- Demonstrated technical feasibility



LArPix ASIC



The LArPix ASIC

- the many times reproducible element of the *LArPix pixelated charge readout system*
- a low-power, cryo-compatible 64-channel custom detector system-on-a-chip for charge-sensitive signal amplification and self-triggered digitization

LArPix-v3 ASIC

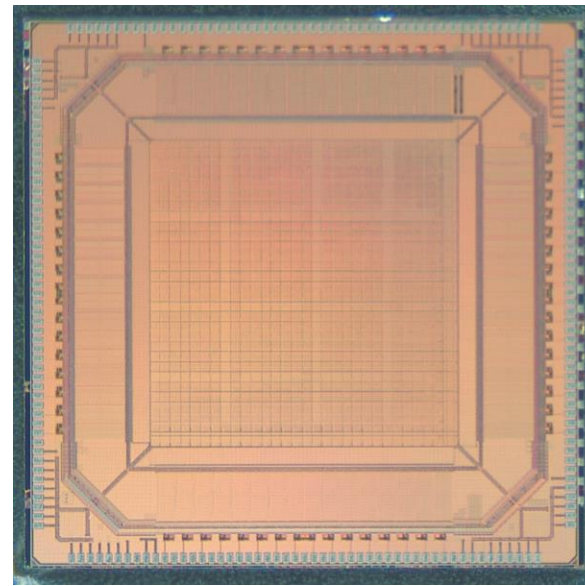
Design ported to 130 nm CMOS

Analog design changes:

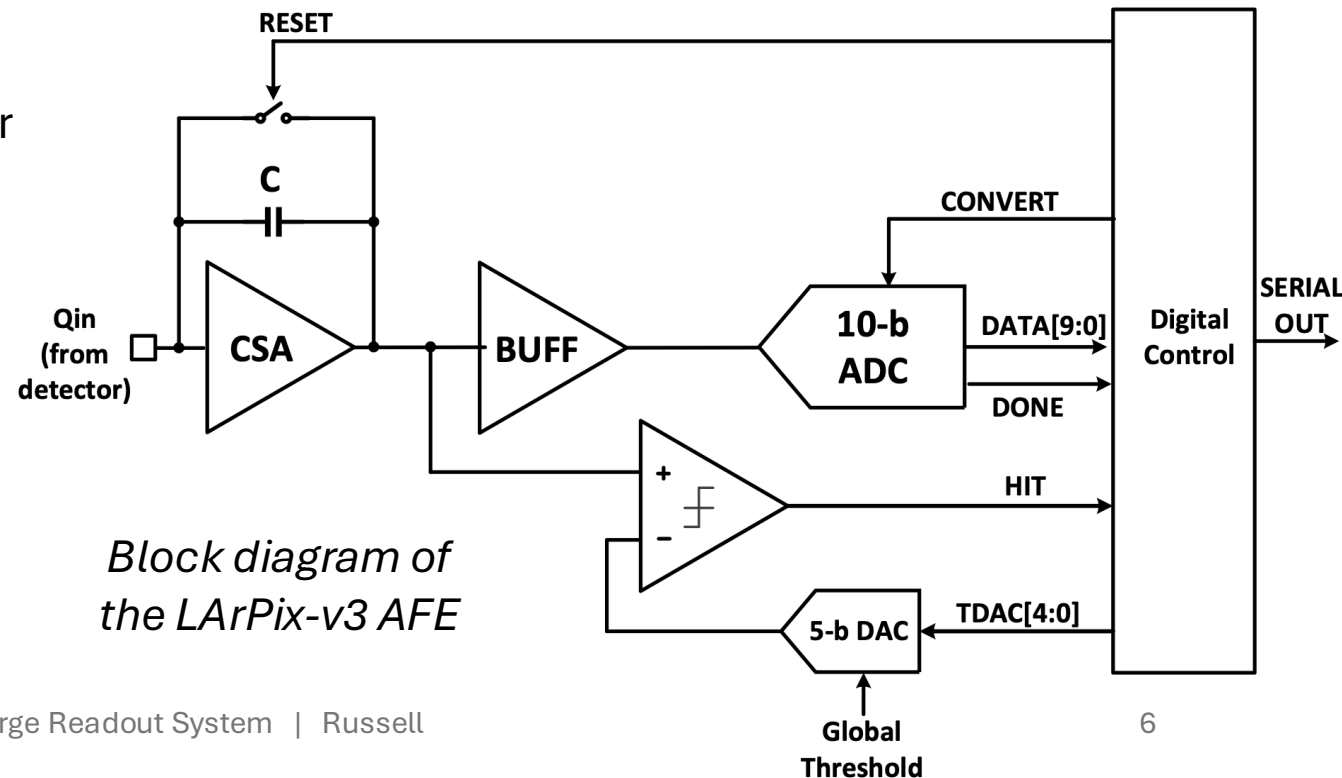
- Asynchronous 10-bit SAR ADC
 - Differential design with bi-directional switching, reduces area and power
 - Asynchronous logic: internally-generated clock speeds ADC conversion
- Super source follower design front-end buffer
 - $\sim 20 \mu\text{W}/\text{channel}$
 - 2x higher signal-to-noise ratio

Digital design changes:

- Latch-based SRAM
- Data transmitted on every rising clock edge (10 Mbit at 10 MHz CLK)
- Correlated double-sampling capability
- On-chip data diagnostics and logging



Die photo of the
5.4 mm x 5.4 mm
LArPix-v3 chip

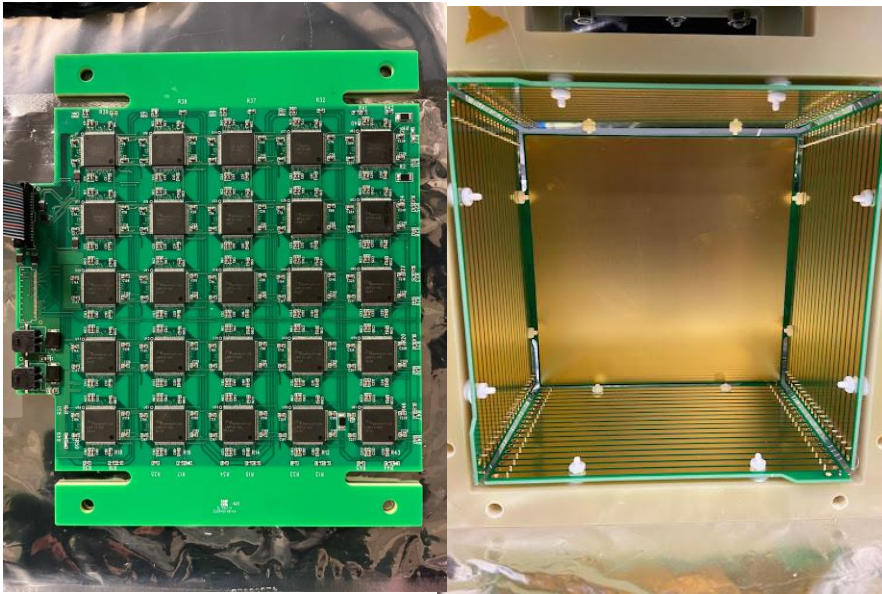


Block diagram of
the LArPix-v3 AFE

LArPix-v3 Performance

94% batch testing yield w/ ~6.5k chips tested

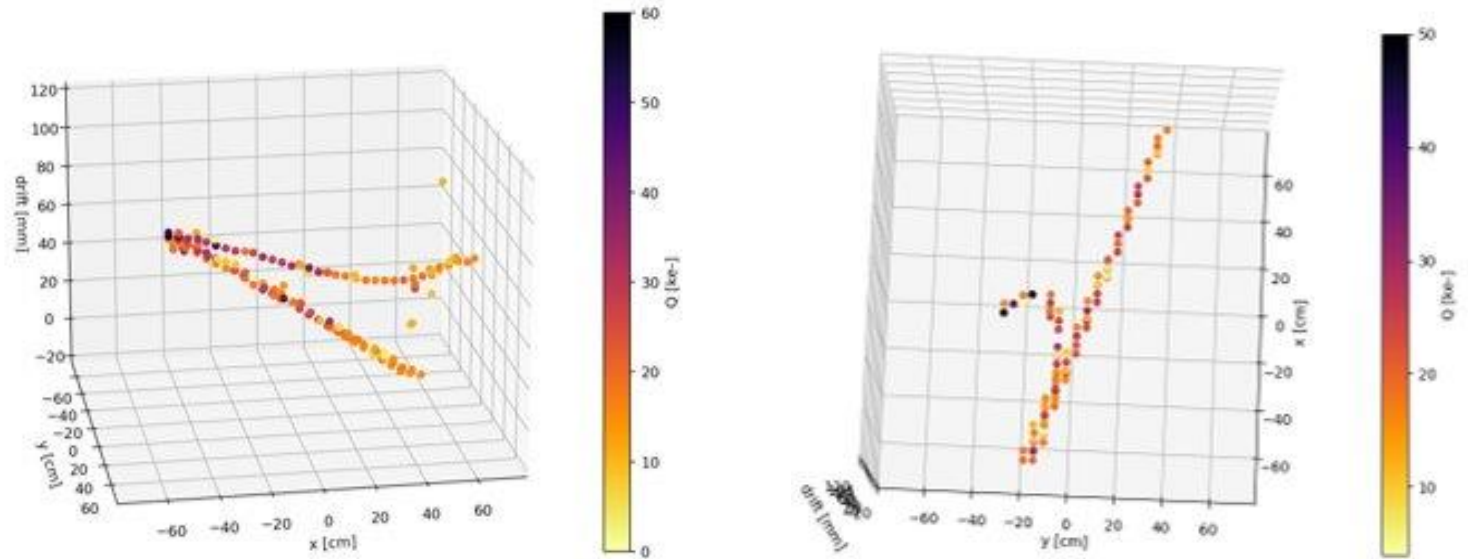
- 2.6% noisy
- 2.7% I/O failures



15 cm x 15 cm anode tile
1600 pixels at 3.7 mm pixel pitch
10 cm LArTPC maximum drift

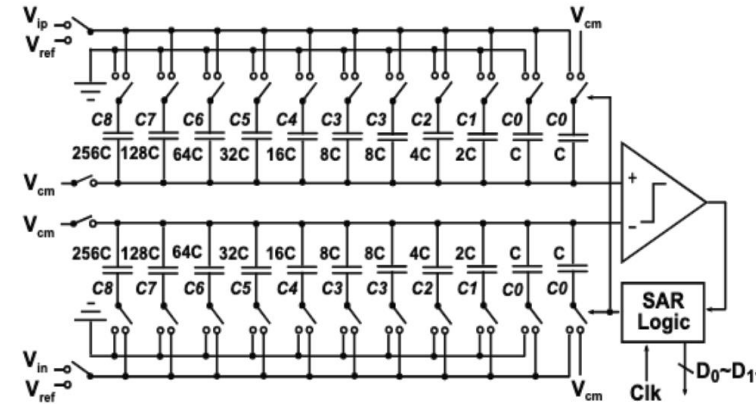
Specification @ 77K	LArPix-v2b	LArPix-v3
CMOS technology	180 nm	130 nm
Noise	800 ENC	500 ENC
Power per channel	142 μ W	173 μ W*
ADC resolution	8 bits	10 bits
Dynamic range	300 ke-	400 ke-
Minimum resample time	1.1 μ s	1.4 μ s

*Dominated by analog power, can be reduced with reduction in dynamic range

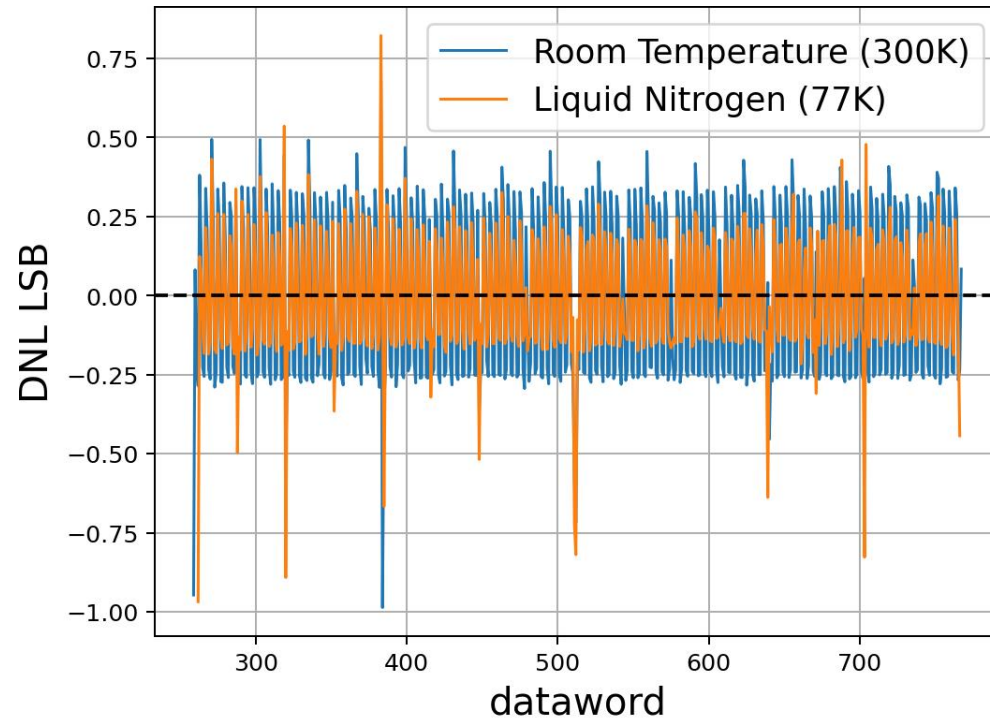


Mini LArTPC operated at LBNL

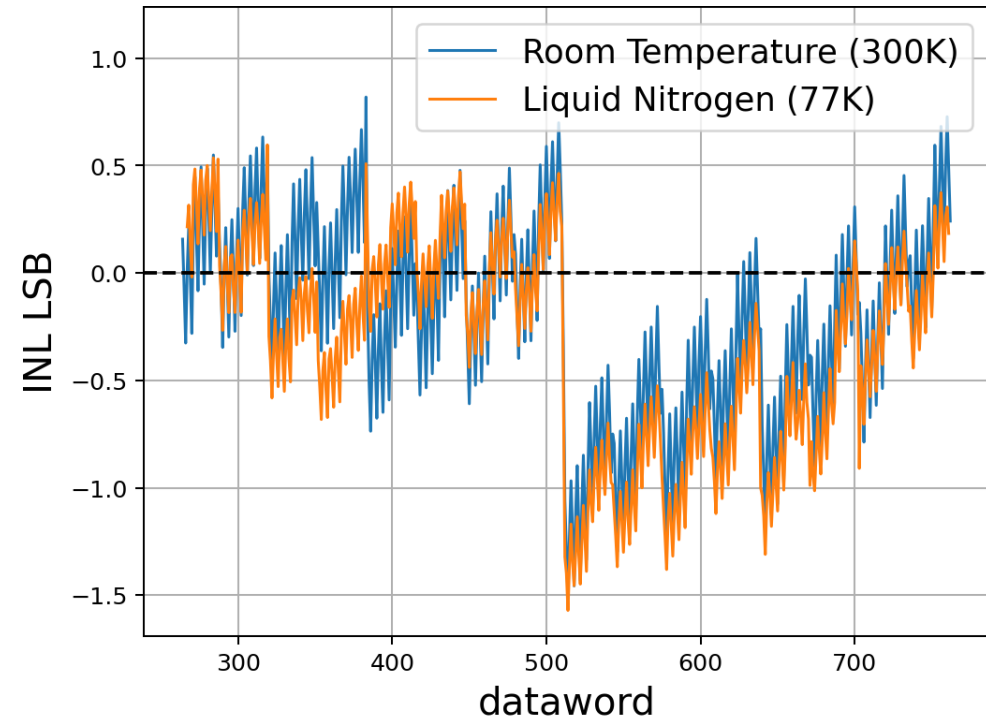
LArPix-v3 ADC Linearity



*LArPix-v3 chip
asynchronous
SAR ADC*

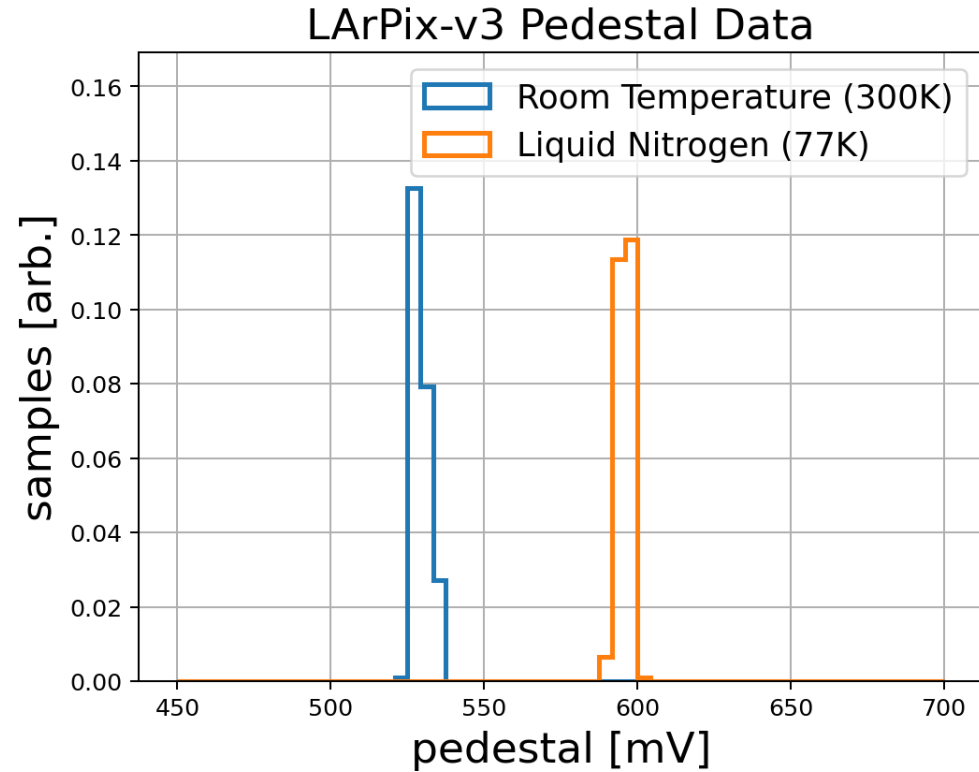


DNL mostly within 0.3 LSBs at
cryogenic temperatures



Missing codes attributed to
systematic layout mismatches

LArPix-v3 Noise



ASIC Version	Noise [e- ENC]	Design change relative to previous version
v1	275 ^[1]	
v2a	950 ^[2]	Significant increase in design complexity, functionality
v2b	800 ^[3]	Reduced metal fill
v3	500	Removal of low-gain option, new buffer, new ADC

[1] *JINST* **13** (2018) 10, P10007

[2] *Instruments* **8** (2024) 3, 41

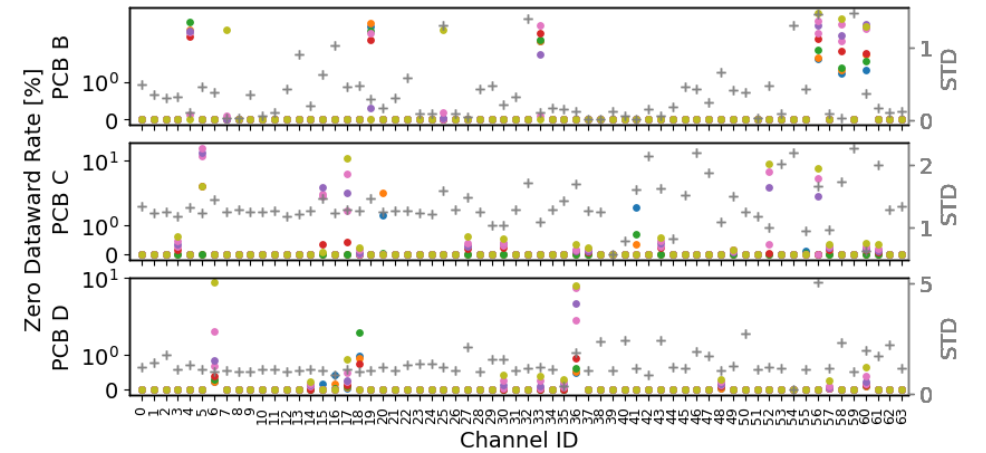
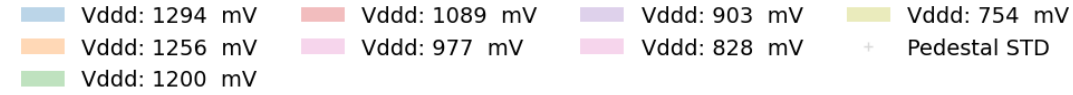
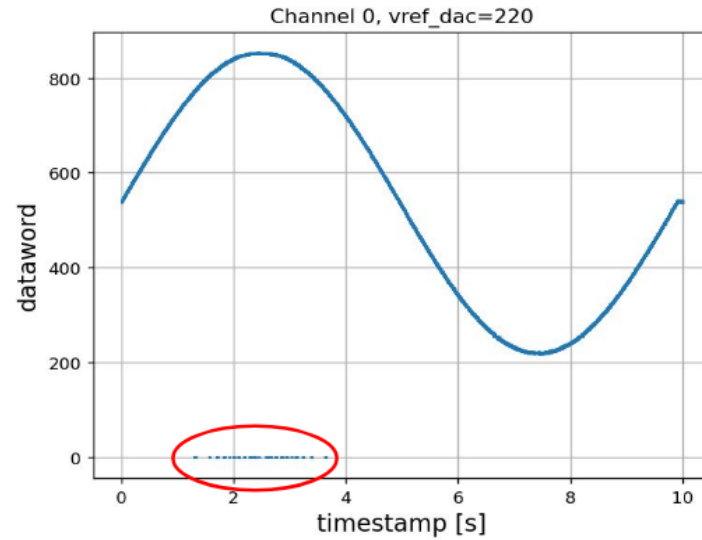
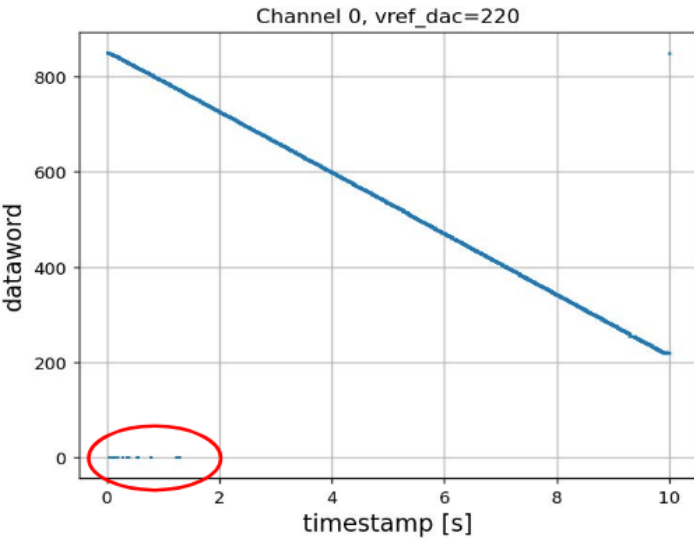
[3] *Annu. Rev. Nucl. Part. Sci.* **74** (2024) 529

MIP S:N >35:1

Shift in pedestal voltages at cryogenic operation attributed to elevated CMOS threshold voltage

~0.1% of ADC reads produce incorrect value of '0'

0-dataword Bug



Attributed to implementation error – conflict in asynchronous vs. synchronous logic between ADC and digital core

Remediation identified to safely transfer ADC data into core clock domain ==> mitigated in revised v3b design

Periodic Reset Charge Injection

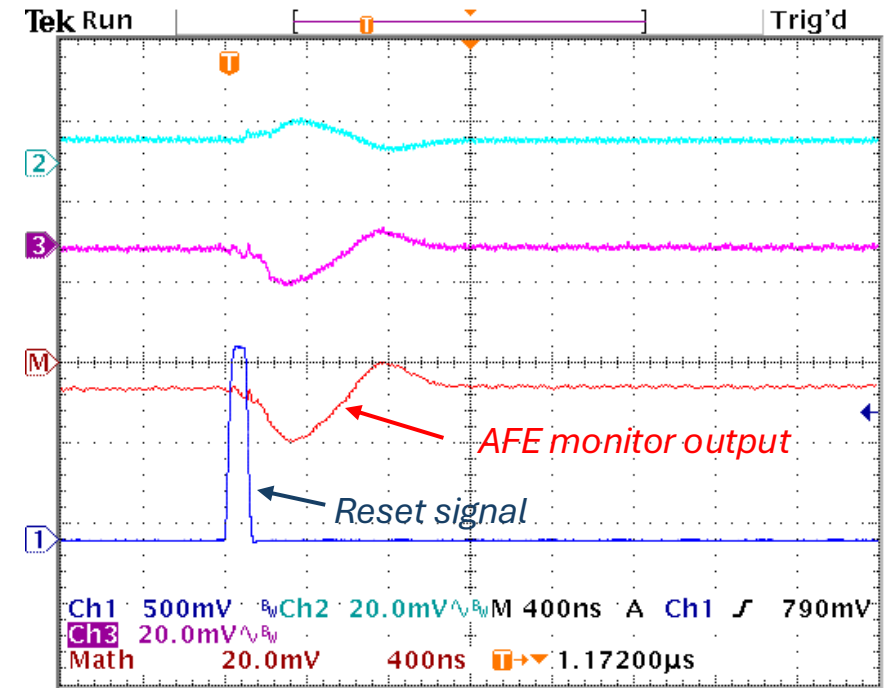
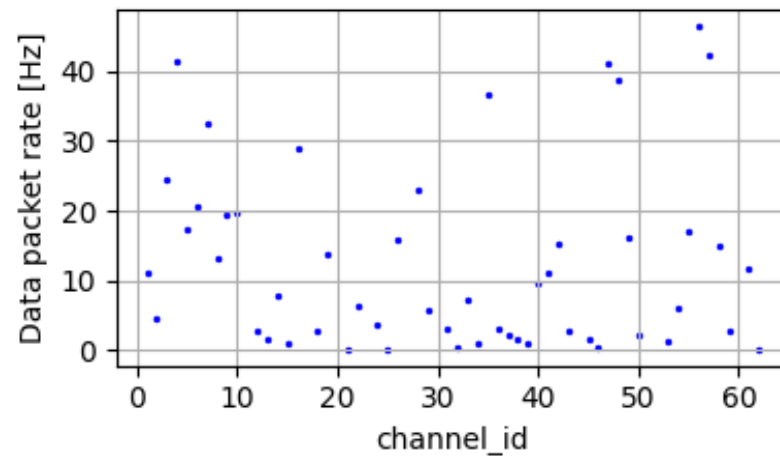
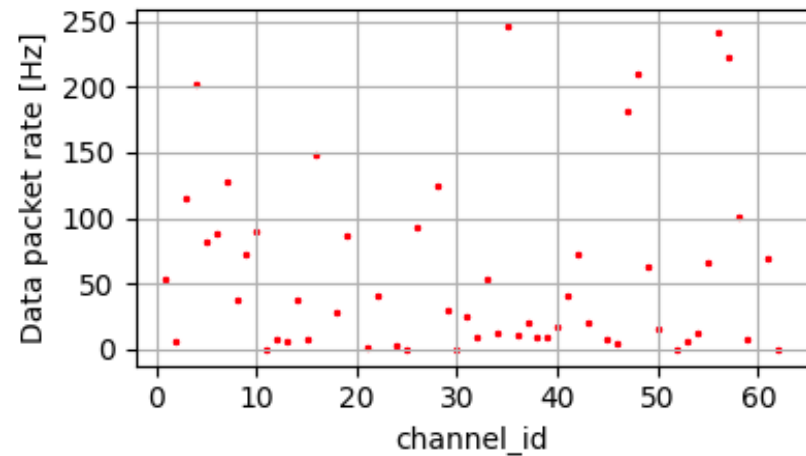
Noise introduced by periodic front end reset causes spurious triggers at low thresholds ($\sim 3000 e^-$)

Self triggered LArTPC data with high / low reset frequency

Chip 44

PRC = 128

PRC = 1280



Input of discriminator moved to the output of the CSA (v3) instead of the output of the buffer as previously implemented (v2)

Design remediation options under evaluation; negligible effect at higher (~ 5000 electrons) operating thresholds

LArPix Anode Tile

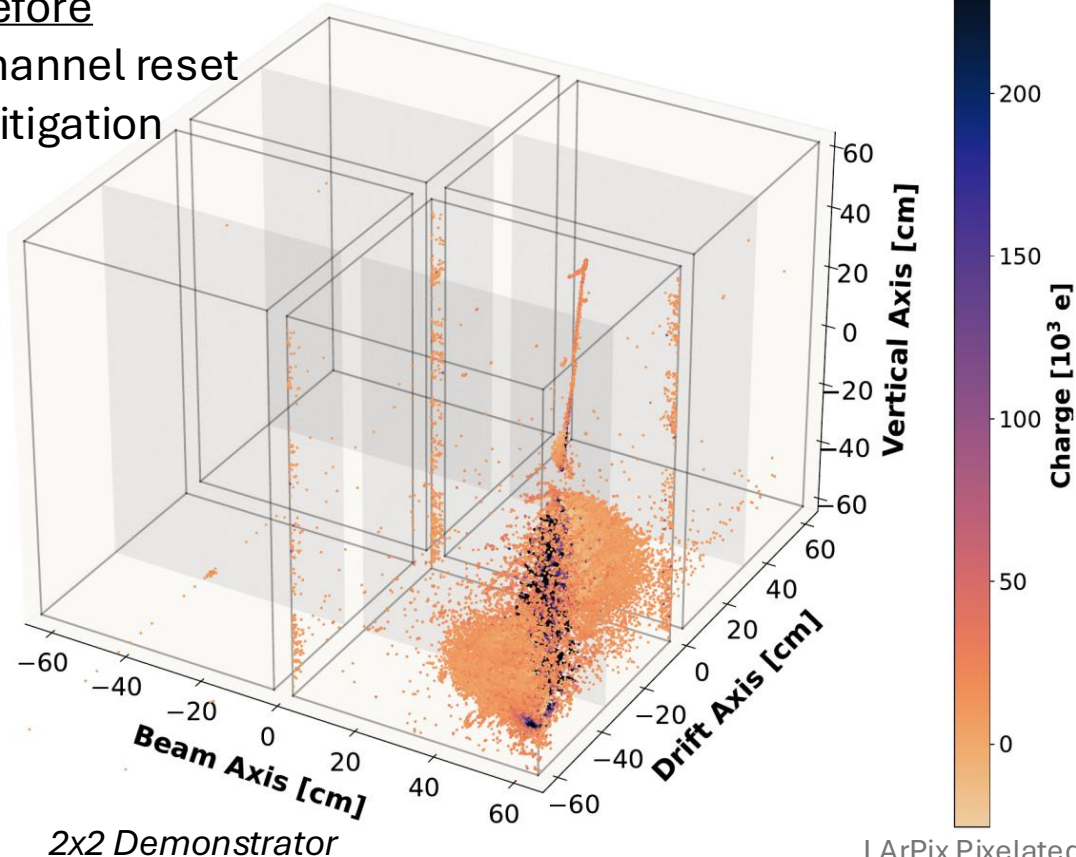


Far-field triggering

Significant pre-triggering observed for large particle showers

Partially mitigated with periodic AFE reset, similar to high-pass filter

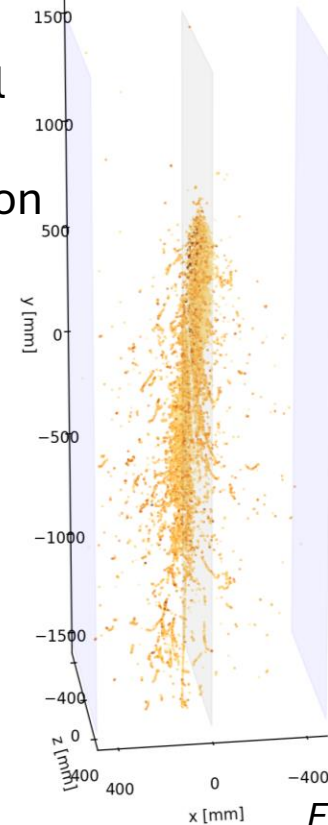
Before
channel reset
mitigation



2x2 Demonstrator

After
channel reset
mitigation

Event 5486, ID 5486 - 2024-11-06 21:03:14 UTC

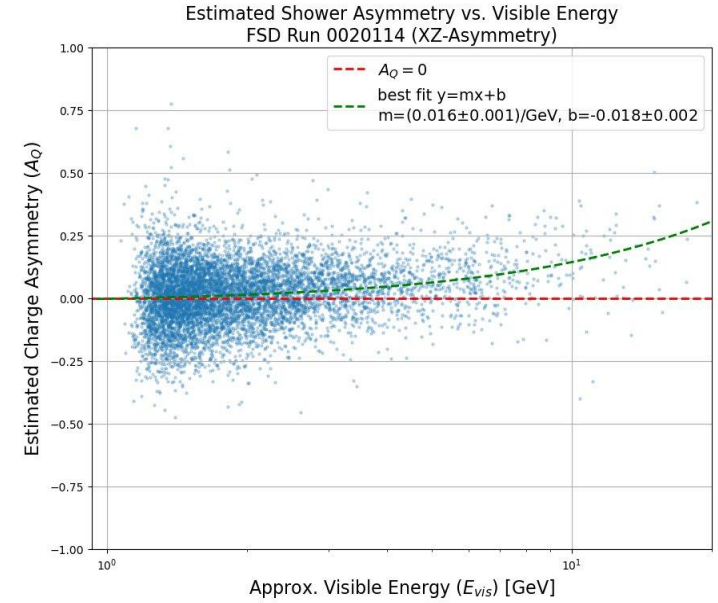


Full-Scale

Demonstrator

Anode shield plane R&D:

- Add copper-clad & perforated PCB in front of anode tile
- Bias to approx. -1 kV to ensure full ionization electron transparency to anode

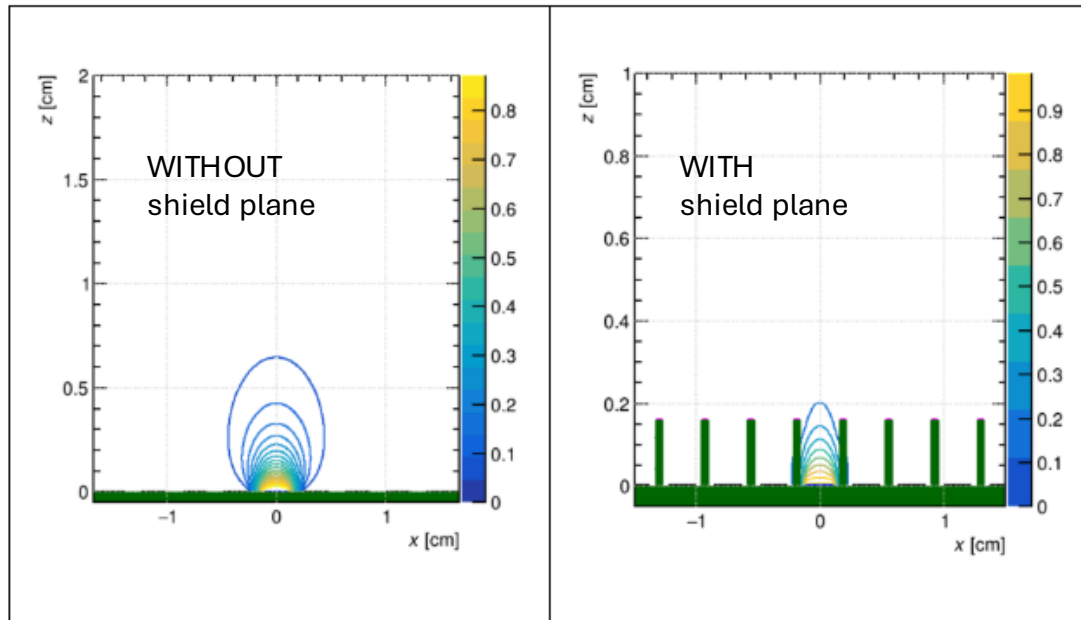
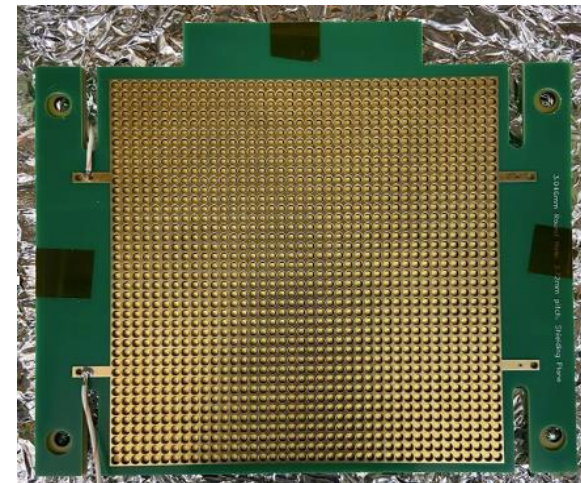
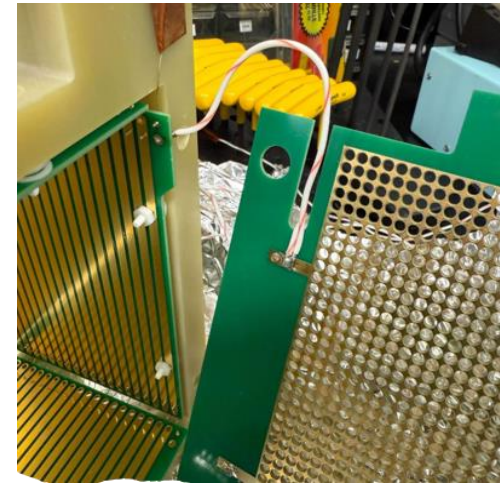


Shield Plane R&D

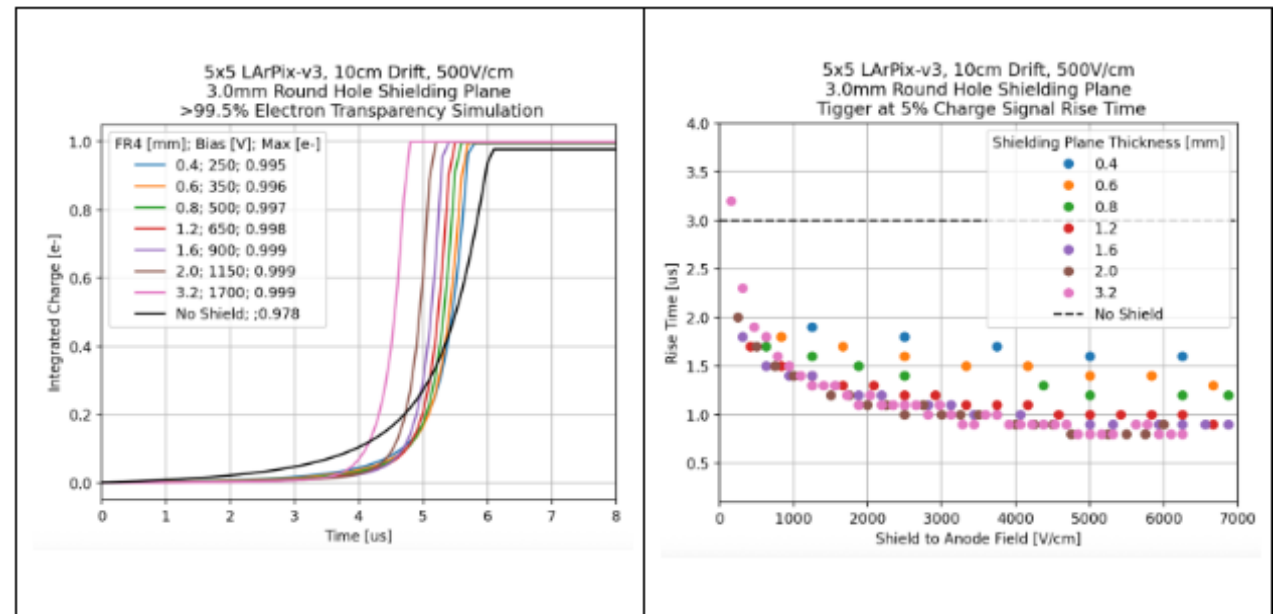
Simulations solve for the electric field in 50 V bias voltage steps with Garfield++

For each step, 10k electrons drifted from 10 cm above a pixel-pitch area (3.72 mm² for 5x5 chip array LArPix v3 mini tile)

The number of electrons landing on the pixel pad was recorded to calculate electron transparency.



Weighting potential comparisons

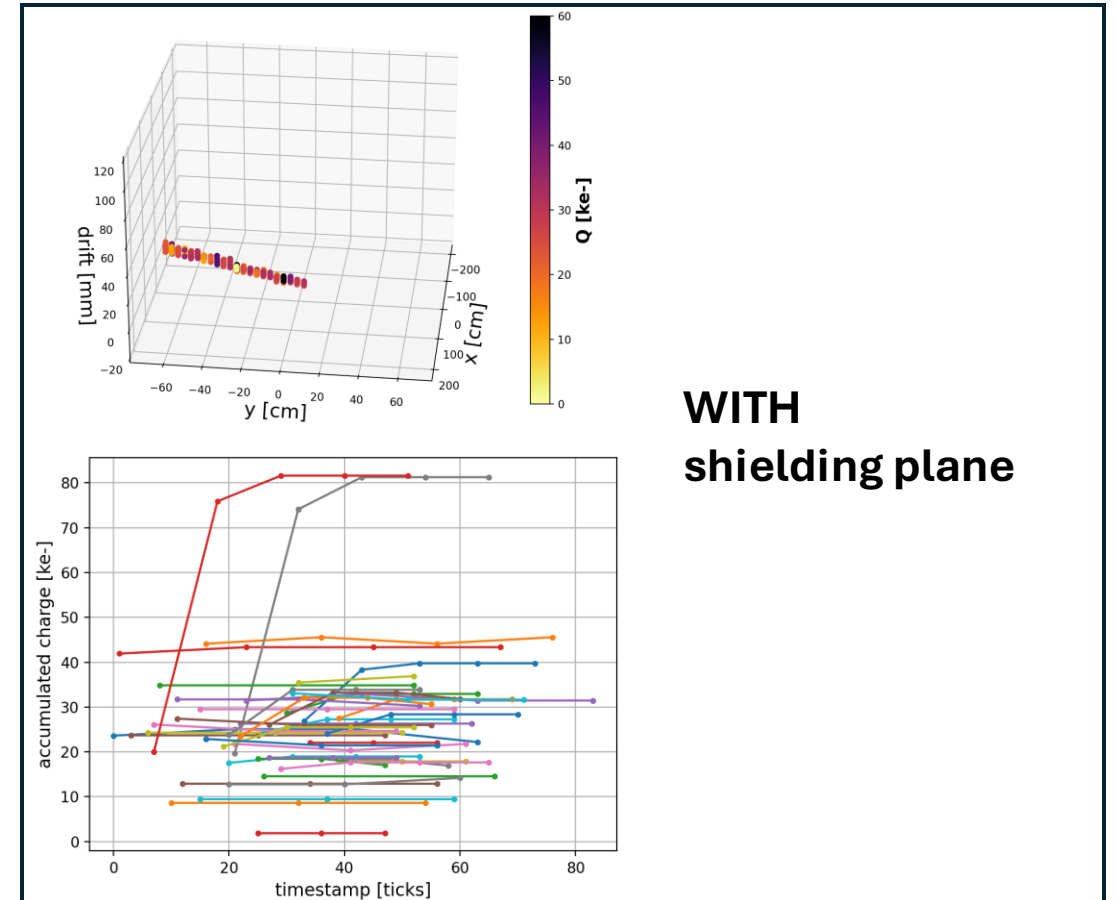
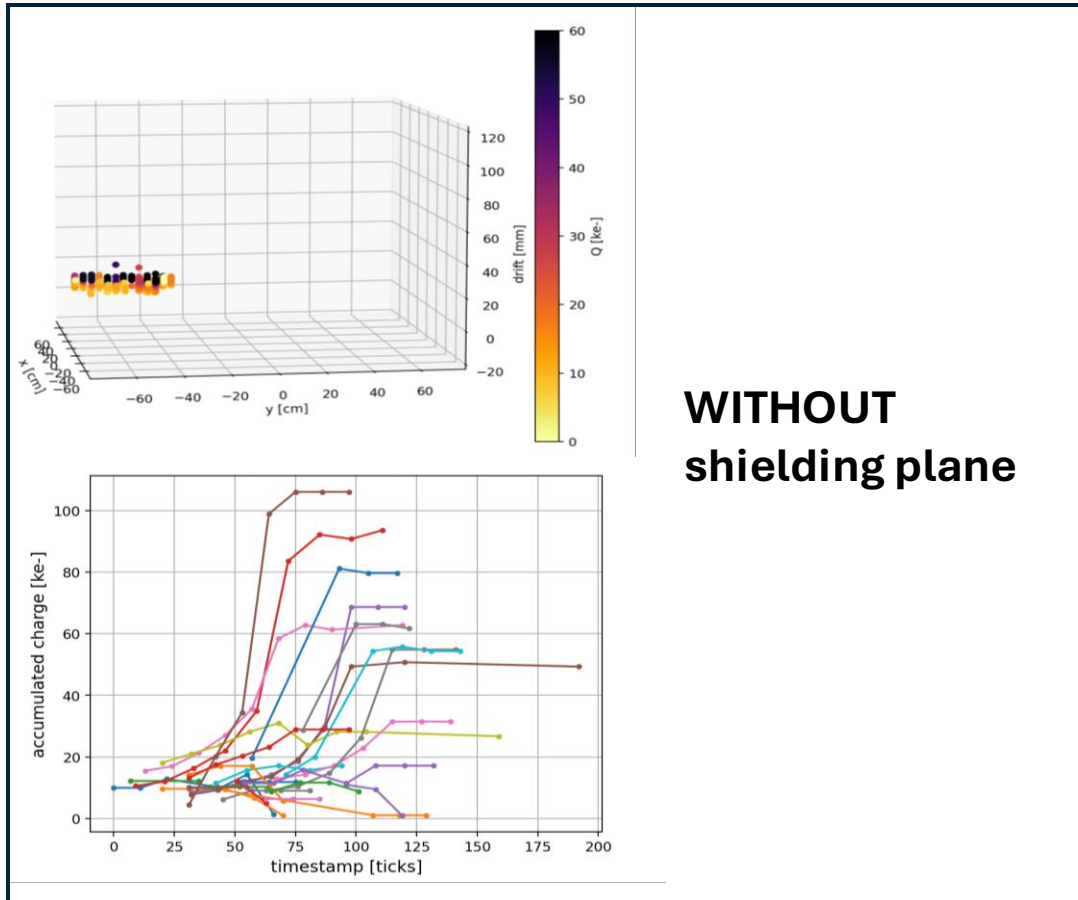


Simulated integrated signal rise time with and without shield

Impact on Response Shape

Signal induction reduced to near field with shield plane

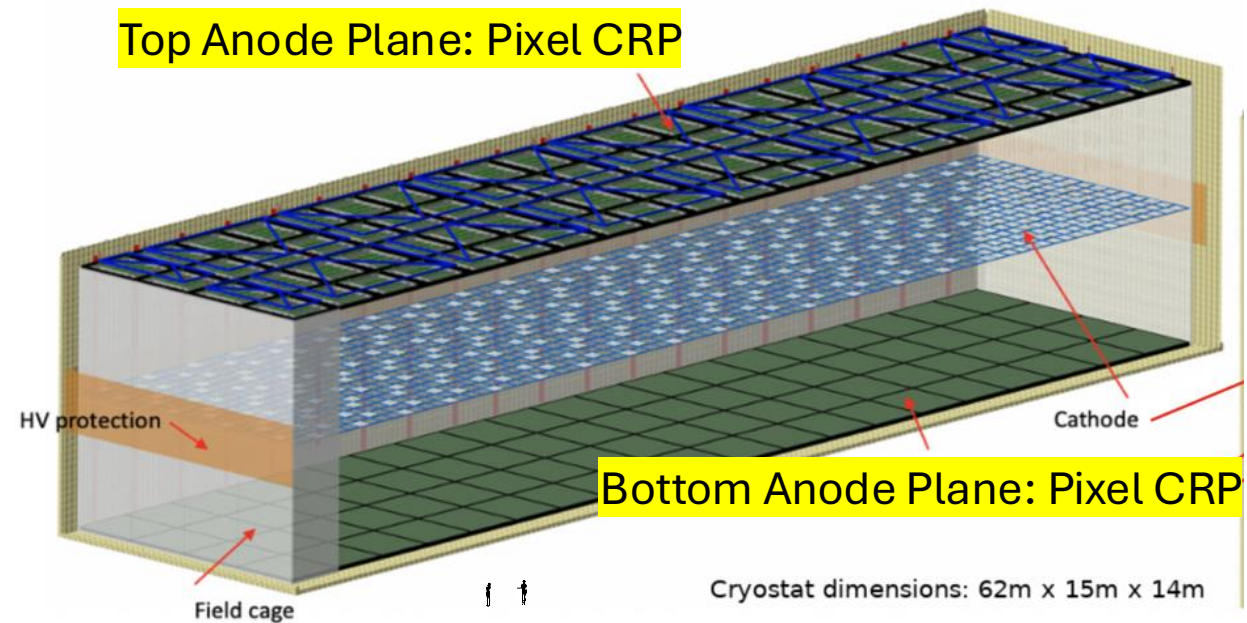
Data collected in ADC burst mode:
successive integrations when
charge exceeds channel threshold
until signal settles



Scalability to $O(10^8)$ channel systems

DUNE Phase 2 will feature two additional far detector modules

See [DUNE Phase 2 plenary presentation](#)
Friday at 9am



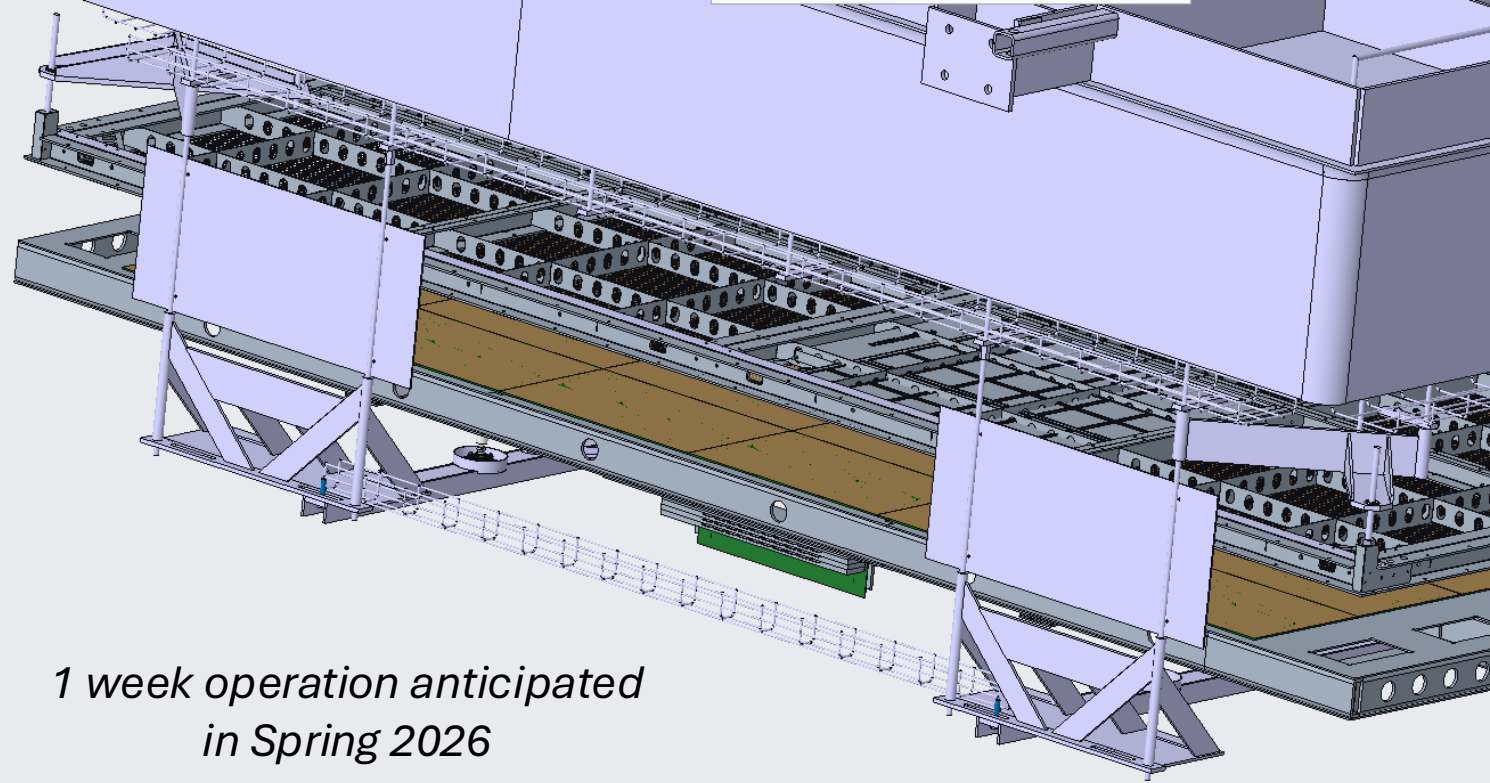
- Top & Bottom Pixel charge readout plane (CRP) readout:
- 160 CRPs instrumenting 1440 m²
 - 114M pixels driven by 1.79M ASICs on 11.2k tiles

LArPix in CERN Cold Box

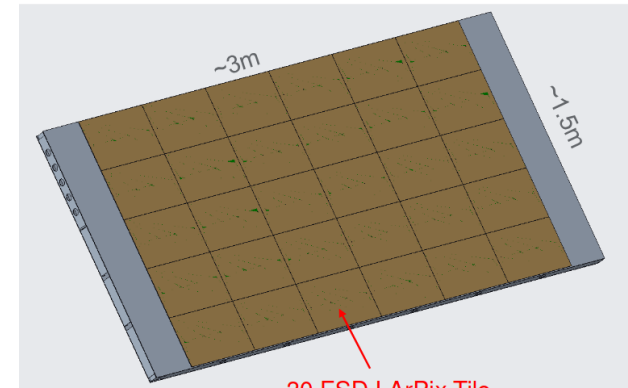
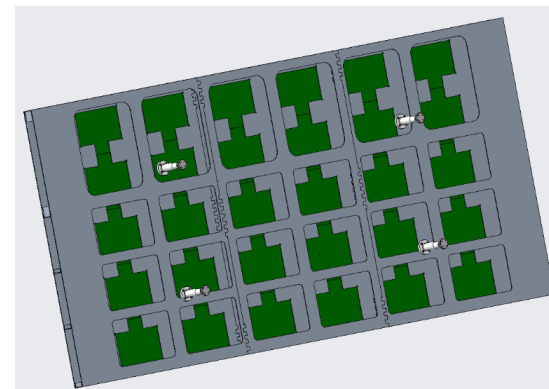
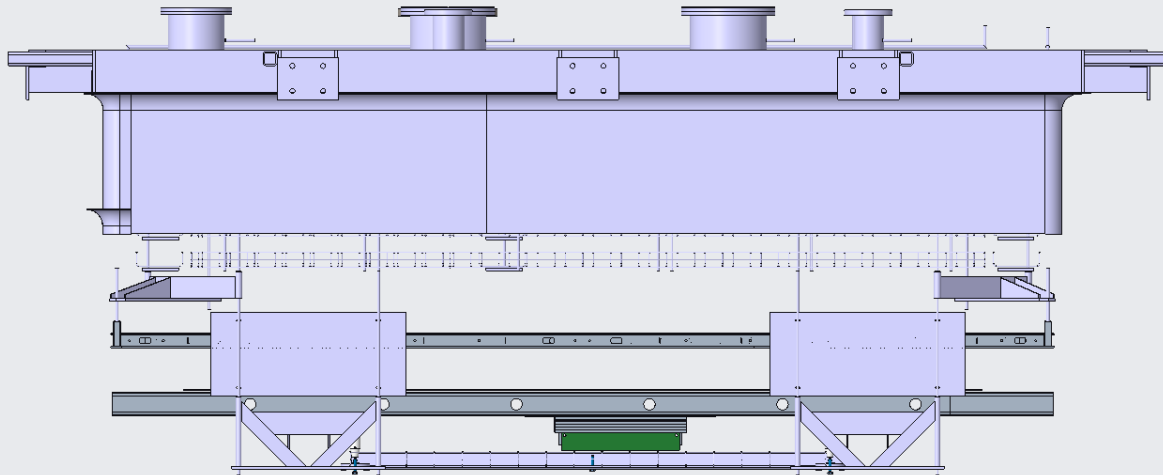
Instrument a bottom anode CRP with LArPix anode tiles

- 3 m by 3m anode area
- 614.4k pixels at 3.72 mm pitch
- 40x (20x) LArPix-v2d (LArPix-v3) FSD-sized LArPix anode tiles

CRU & CRP dimensions are designed to be identical to VD CRP

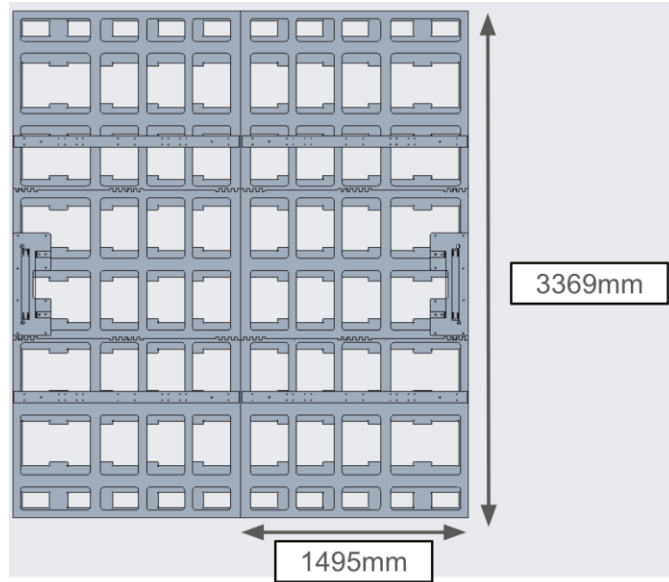


*1 week operation anticipated
in Spring 2026*



Preparations for pixel anode support frame

Cryo-cycle test at University of Grenoble (August 2025)



MADCAP

Multiplexer ASIC for Data and Clock Aggregation and Propagation

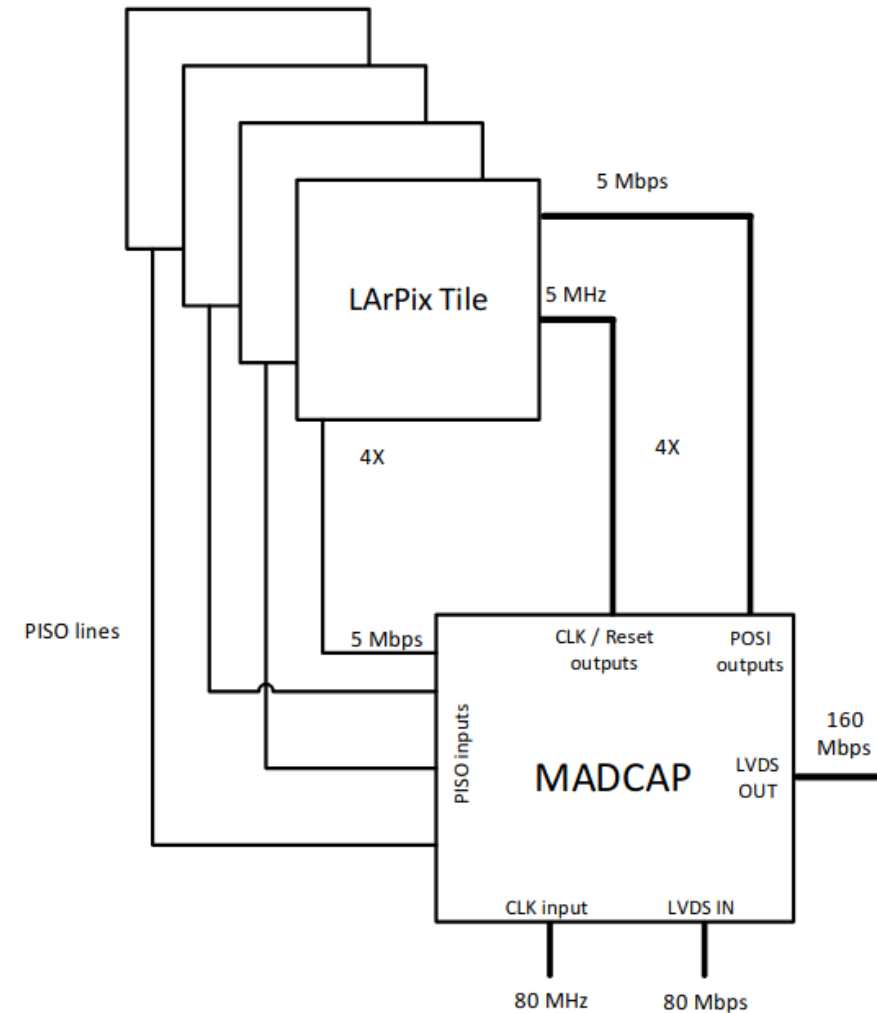
30-meter cable distance from bottom DUNE far detector anode

A data aggregator to reduce the cable plant by a factor of 8

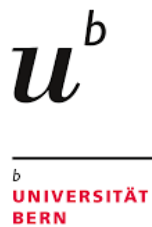
- 160 Mbps data output in a 12 byte superpacket

Roughly 4 μ W/LArPix channel power overhead

Same package and CMOS process as LArPix-v3



LArPix Partners



Summary

- LArPix-v3 port to 130 nm was successful
 - 10-bit ADC is functional
 - Improved monitoring features
 - Multiple bugs identified and to be addressed in v3b
- Anode shield plane R&D in progress
 - Demonstrated signal induction reduction
 - Larger-scale TPC tests planned
- LArPix system architecture scaling to ~100M channels
 - Preparations for CERN vertical drift cold box operations in progress
 - Cryo-compatible low-power digital multiplexer ASIC in development