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A Smart Readout ASIC with Digital Signal Processing and Machine Learning Integrated into the Front-End

Thursday 9 October 2025 12:00 (20 minutes)

The explosive growth in data rates being seen by next-generation detectors calls for transformative solutions that integrate intelligence at the edge. In this talk, we will present a smart readout application specific integrated circuit (ASIC) that incorporates advanced digital signal processing (DSP) and artificial neural networks (ANNs) directly into the detector front-end. By leveraging high-level synthesis for the DSP circuitry and custom RTL design for the ANNs, we co-optimize multi-layer perceptrons (MLPs) for regression and classification tasks, including amplitude estimation and pulse shape discrimination. A stochastic rounding technique ensures convergence of training with quantized weights, enabling deployment of compact AI models on-chip. This tight integration of DSP and machine learning in front-end electronics opens the door to real-time feature extraction and low-latency edge processing, leading to improved energy-efficiency and reduction in data transmission rates to further data acquisition systems.

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