The Analog Photon Processor ASIC

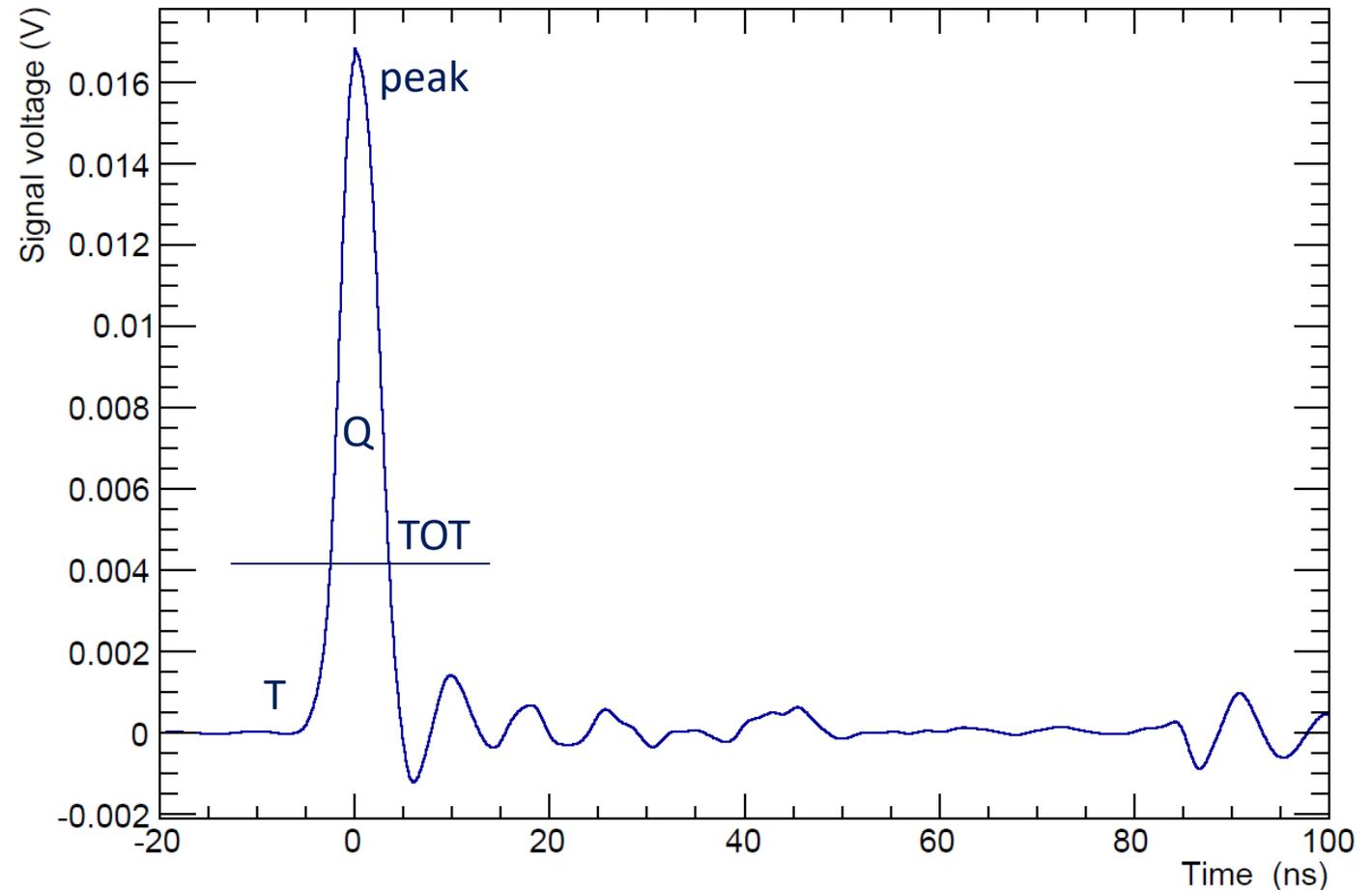## Coordinating Panel for Advanced Detectors Workshop

Adrian Nikolica, for the UPenn Instrumentation Group

nikolica@hep.upenn.edu

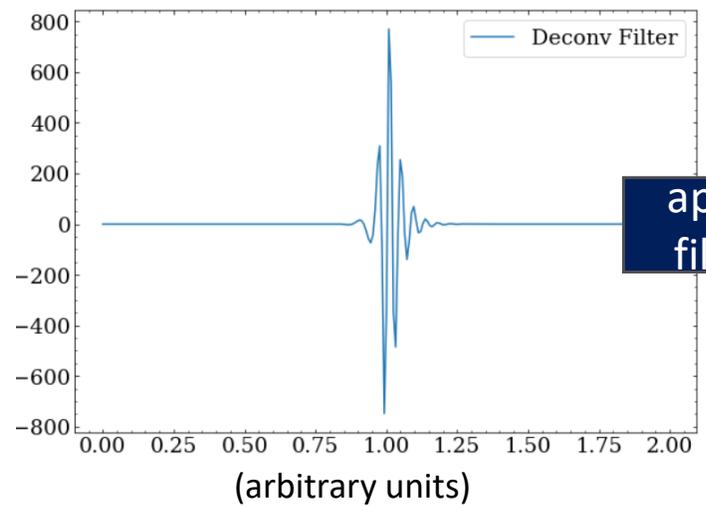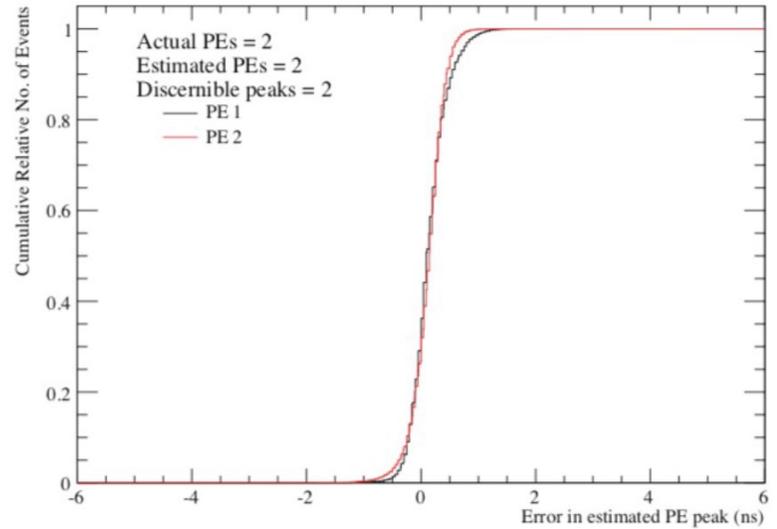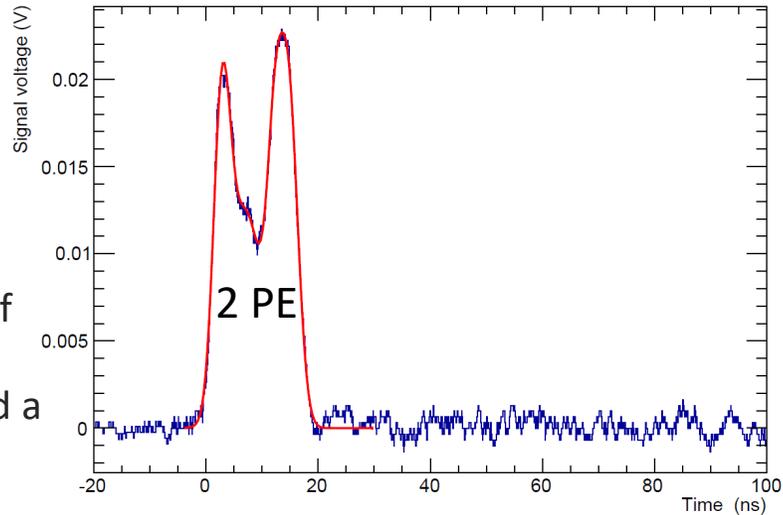University of Pennsylvania, 9 October 2025

1

APP concept

- Motivation:
  - Cherenkov, scintillation, or hybrid detectors
  - We are interested in the number of photoelectrons (PE), and their arrival times
  - Prototype targeted to fast, large area PMTs

- Can we avoid full digitization?
  - Petabytes – exabytes per year in 10^4 channel systems
  - Power hungry
  - High cost
  - Resolution and dead time (closely spaced pulses)

- Need these parameters to characterize an arbitrary PMT pulse:
  - Leading edge time
  - Trailing edge time – get time over threshold (TOT) from edge times
  - Peak amplitude
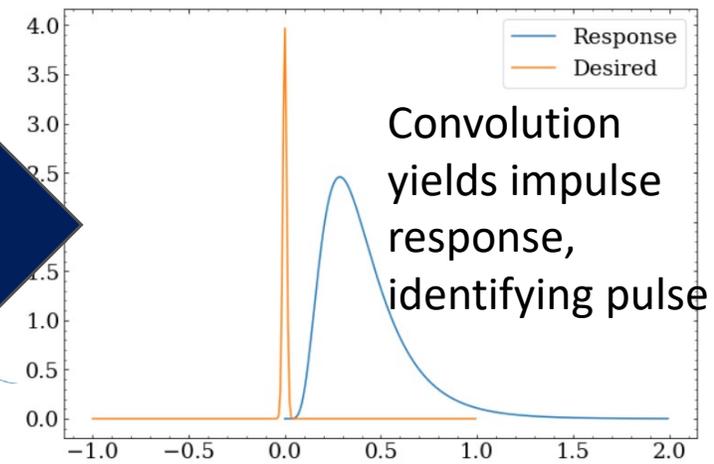 - Peak time
  - Total charge (Q)

PE measurement and counting

- How can we determine #PEs ?

- Maximum likelihood estimation
  - Calculate 3-D probability density functions using TOT, Q, peak
  - Obtain good estimate of number of PE in a pulse for 1—8 PE
  - Proof of concept that we only need a few measurements

- Frequency domain
  - Convolve filter response of ideal log-normal pulse with input signal
  - Sensitive to filter kernel, aliasing problems

- Many other approaches: matched filter, interpolation, etc.

- Many approaches work best offline, or are difficult to implement with electronics
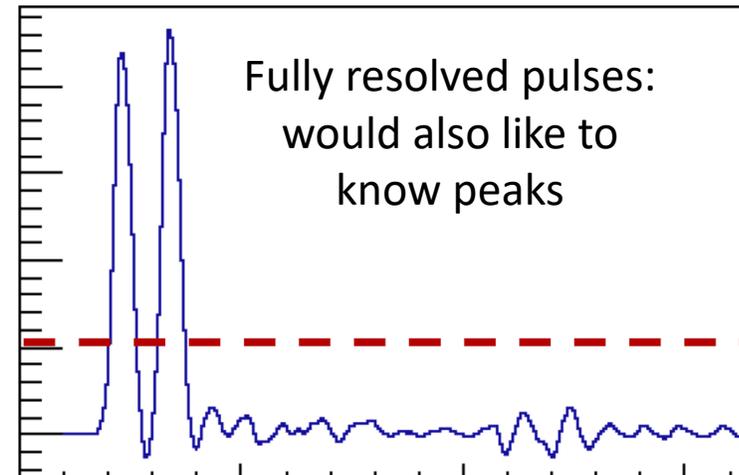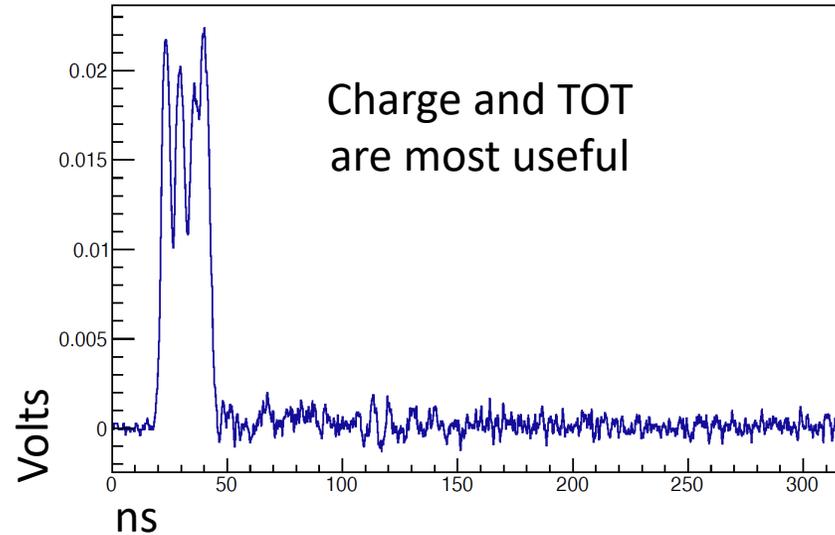

apply filter

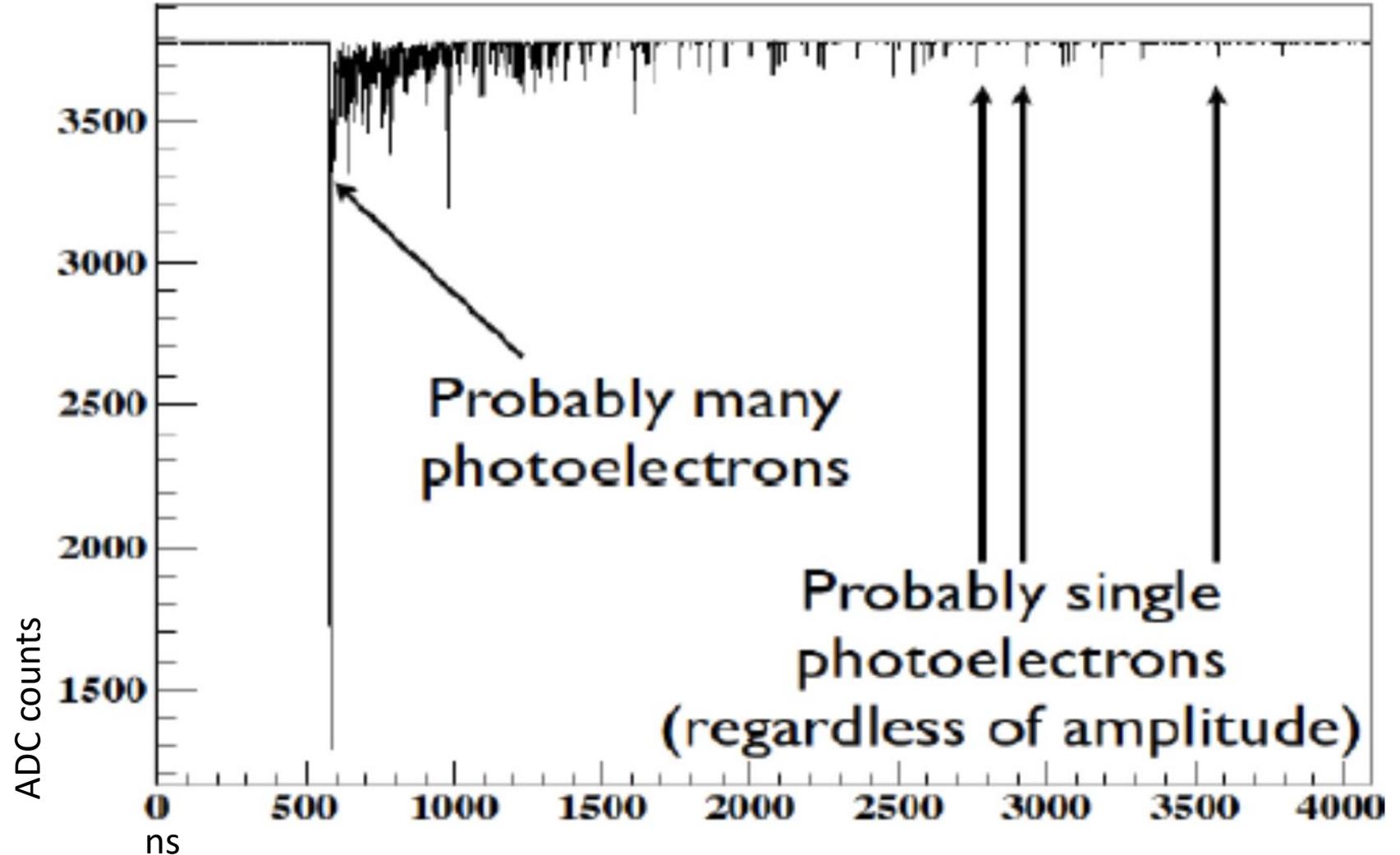Convolution yields impulse response, identifying pulse

PE measurement and counting, cont.

- We can do this with an ASIC, with local analog memory, read out with low cost ADC

- Analog circuit blocks
  - Peak detector
  - Integrator
  - Time to amplitude converter (TAC)

- SNO did this to some extent with TAC, charge (fixed windows)
  - No timing information on second hit

- Some older work in 0.35μm process
  - Not good for modern tubes with sub-ns TTS

- Some ASICs exist for this purpose, but "photon counting" mostly

Charge and TOT are most useful

Fully resolved pulses: would also like to know peaks
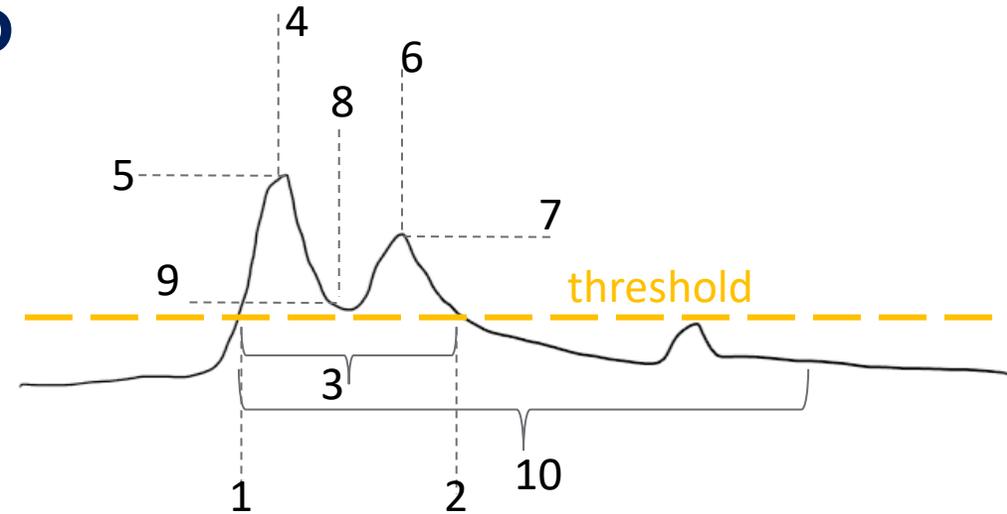
What happens in this case?

- Prompt region: Q gives good estimate of PE

- Tail region: PE counting more relevant

- We want:
  - Fast timing for Cherenkov light
  - Multi-PE resolution and large dynamic range for scintillation light

Probably many photoelectrons

Probably single photoelectrons (regardless of amplitude)

ADC counts

ns

LAr waveform

Basic requirements of APP

- We'd like to capture PMT pulses with:
  - Risetimes ~1ns or less
  - FWHM ~5ns or less
  - Better than 100ps timing resolution (much better than TTS)
  - ~5—500mV amplitude (up to 100 PE)
    - Motivates 2 gain paths

- Charge integral up to a few hundreds of ns up to microseconds
  - Programmable window for "late" scintillation light
  - After a few unresolved PE, most information also in Q

- We want to re-trigger with minimal deadtime
  - To catch closely spaced resolved PE
  - Motivates "analog FIFO"

- Channel density probably limited by cables in a PMT system – not true for pixelated detectors!
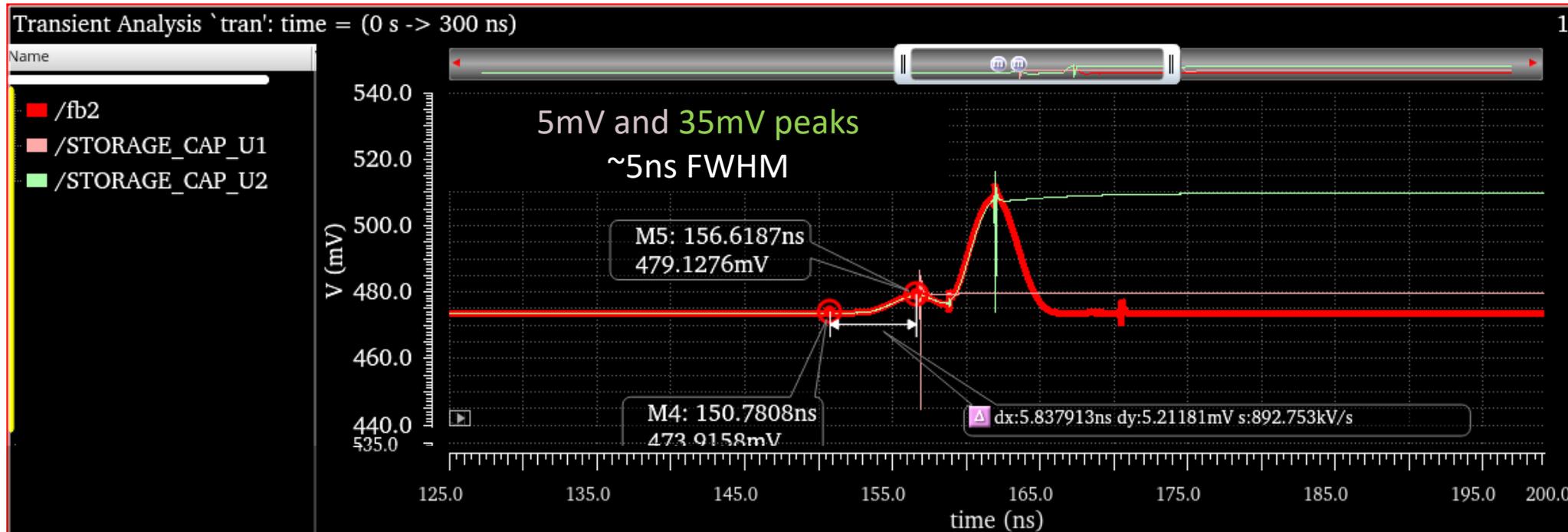

1. Leading edge of TOT "event"
2. Trailing edge of TOT event
3. Integral of TOT event (charge)
4. Time of 1st peak in the event
5. Amplitude of 1st peak in the event
6. Time of 2nd peak in the event
7. Amplitude of 2nd peak in the event
8. Time of 1st valley in the event
9. Amplitude of 2nd valley in the event
10. Integral of total charge over a programmable time starting with the 1st event

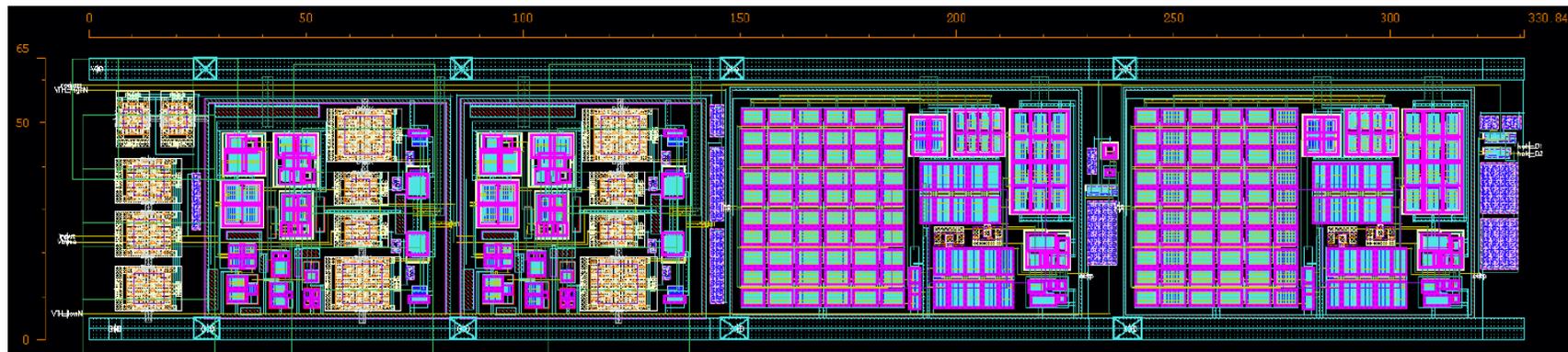Not every measurement needed for every application

Some measurements are cross-checks on others (e.g. "long charge")

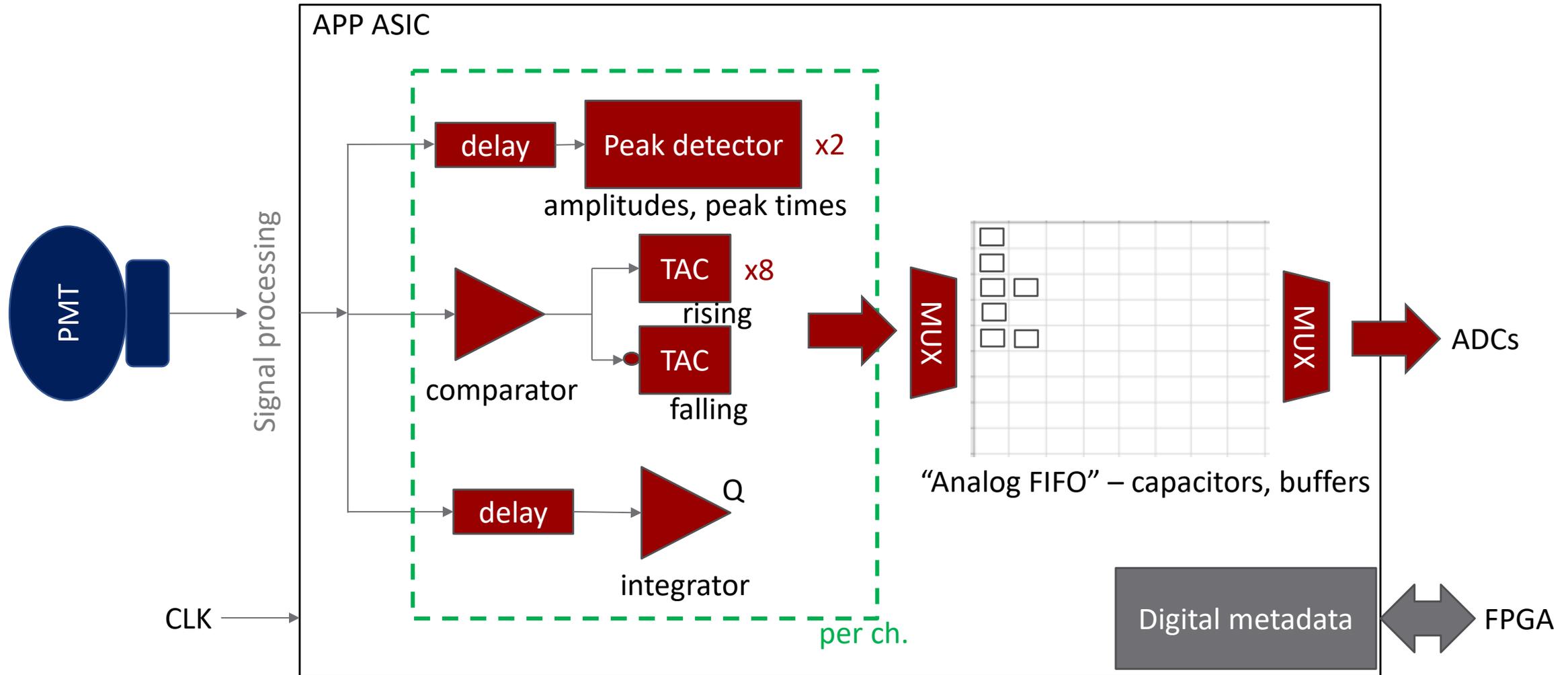# Peak detector circuit simulation
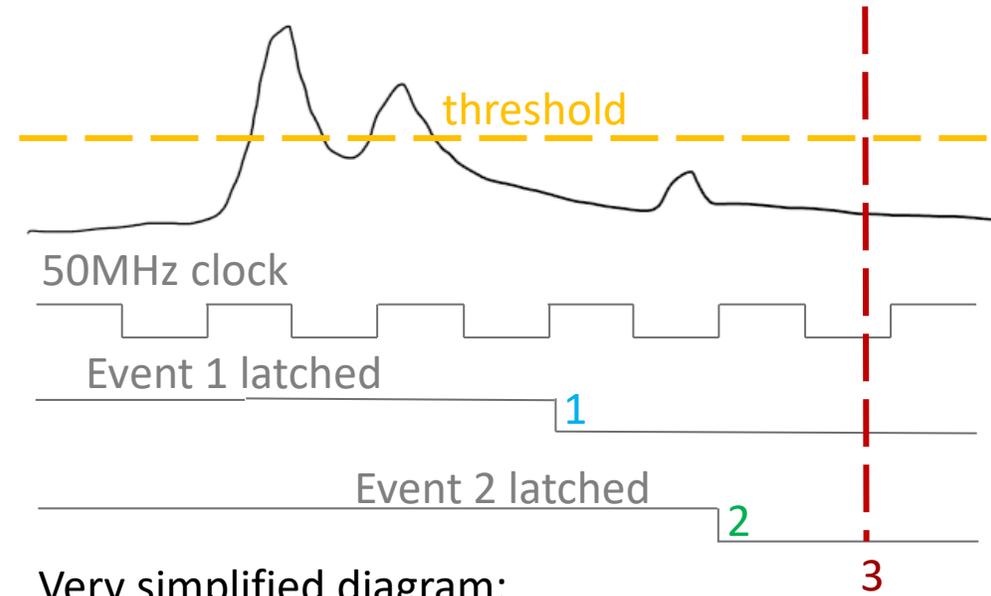
- Using TSMC 65nm process

Layout:

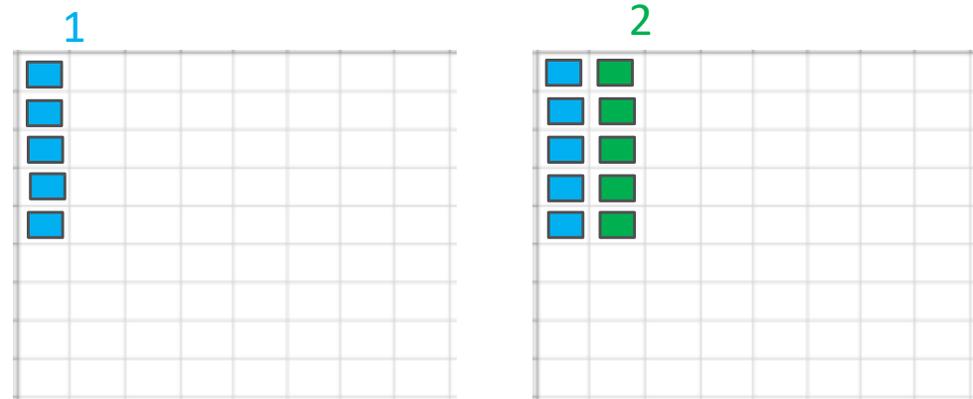# Block diagram (very simplified)

Example #1

- Ping-pong architecture can store 2 closely spaced peaks
  - Second peak is counted as a separate event, and measurements #6—9 are not stored
  - The "long charge" measurement #10 is always a separate analog memory

Metadata at 2:
b0001 – packet type (data)
b0 – not a "long charge"
32-bit timestamps x2 – leading/trailing edges
b0 – single peak
b001 – memory "column"

threshold

50MHz clock

Event 1 latched   1

Event 2 latched   2

3

Very simplified diagram:
2 sample snapshots of analog memory shown
(not all digital signals shown)

1   2

1. Leading edge time
2. Trailing edge time
3. Integral (Q)
4. Time of 1st peak
5. Amplitude of 1st peak
6. Time of 2nd peak
7. Amplitude of 2nd peak
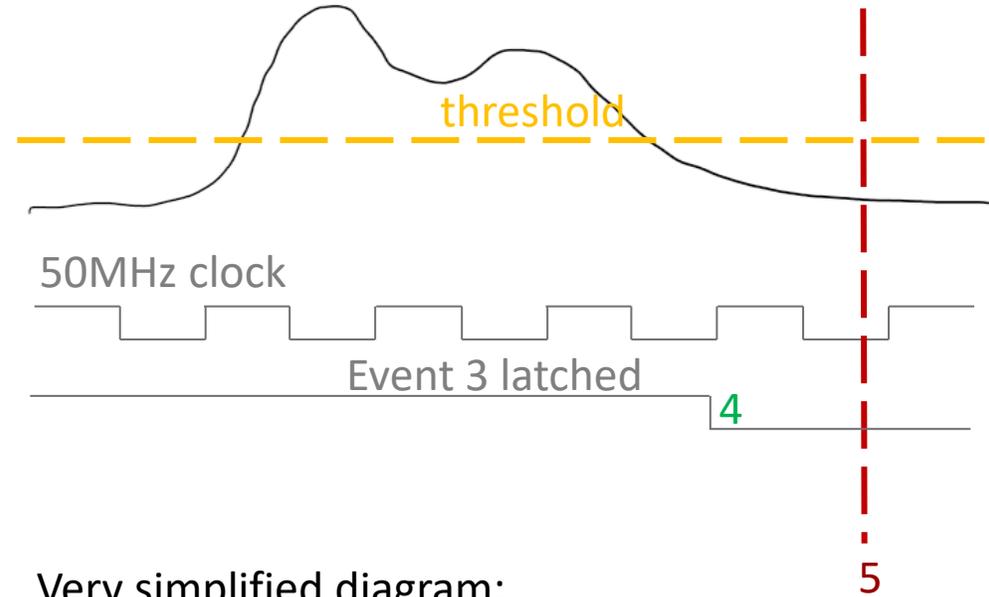8. Time of 1st valley
9. Amplitude of 2nd valley

10. Integral of total charge over a programmable time starting with the 1st event
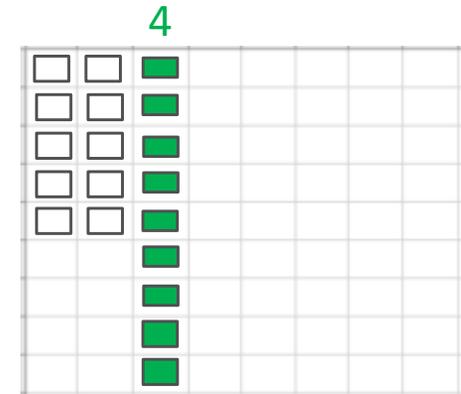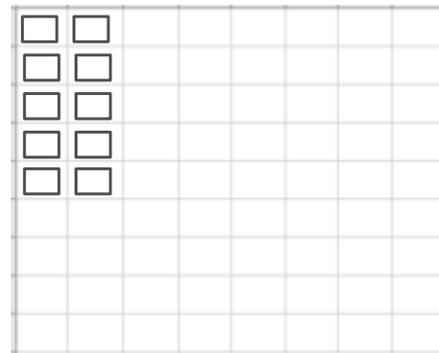
3

Example #2

- Ping-pong architecture can store 2 closely spaced peaks
  - Second peak is counted as a separate event, and measurements #6—9 are not stored
  - The "long charge" measurement #10 is always a separate analog memory
  - → Entire TOT is a double peak event

threshold

50MHz clock

Event 3 latched

4

5

Very simplified diagram:
1 sample snapshots of analog memory shown
(not all digital signals shown)

4

1. Leading edge time
2. Trailing edge time
3. Integral (Q)
4. Time of 1st peak
5. Amplitude of 1st peak
6. Time of 2nd peak
7. Amplitude of 2nd peak
8. Time of 1st valley
9. Amplitude of 2nd valley

10. Integral of total charge over a programmable time starting with the 1st event

5

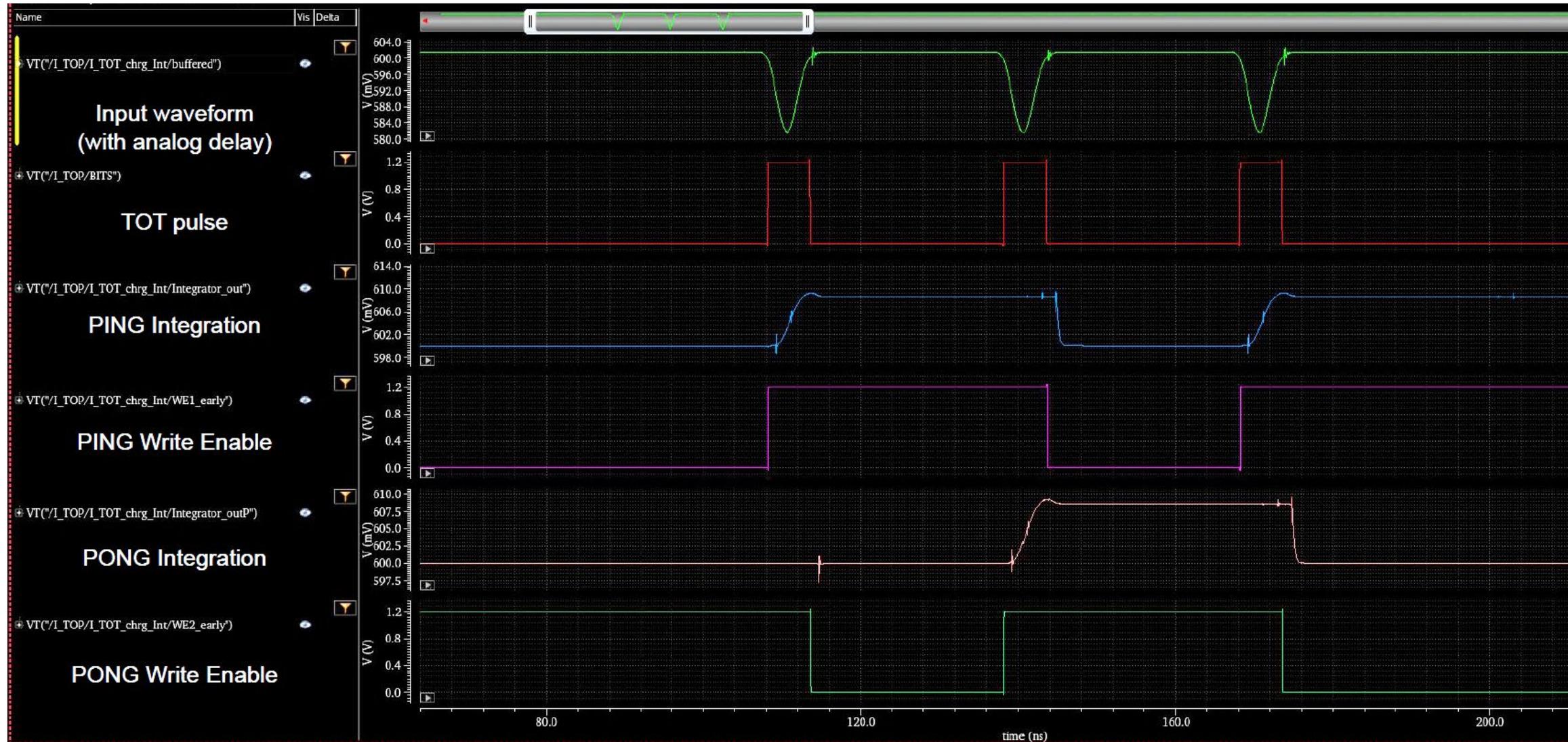Metadata at 4:
b0001 – packet type (data)
b0 – not a "long charge"
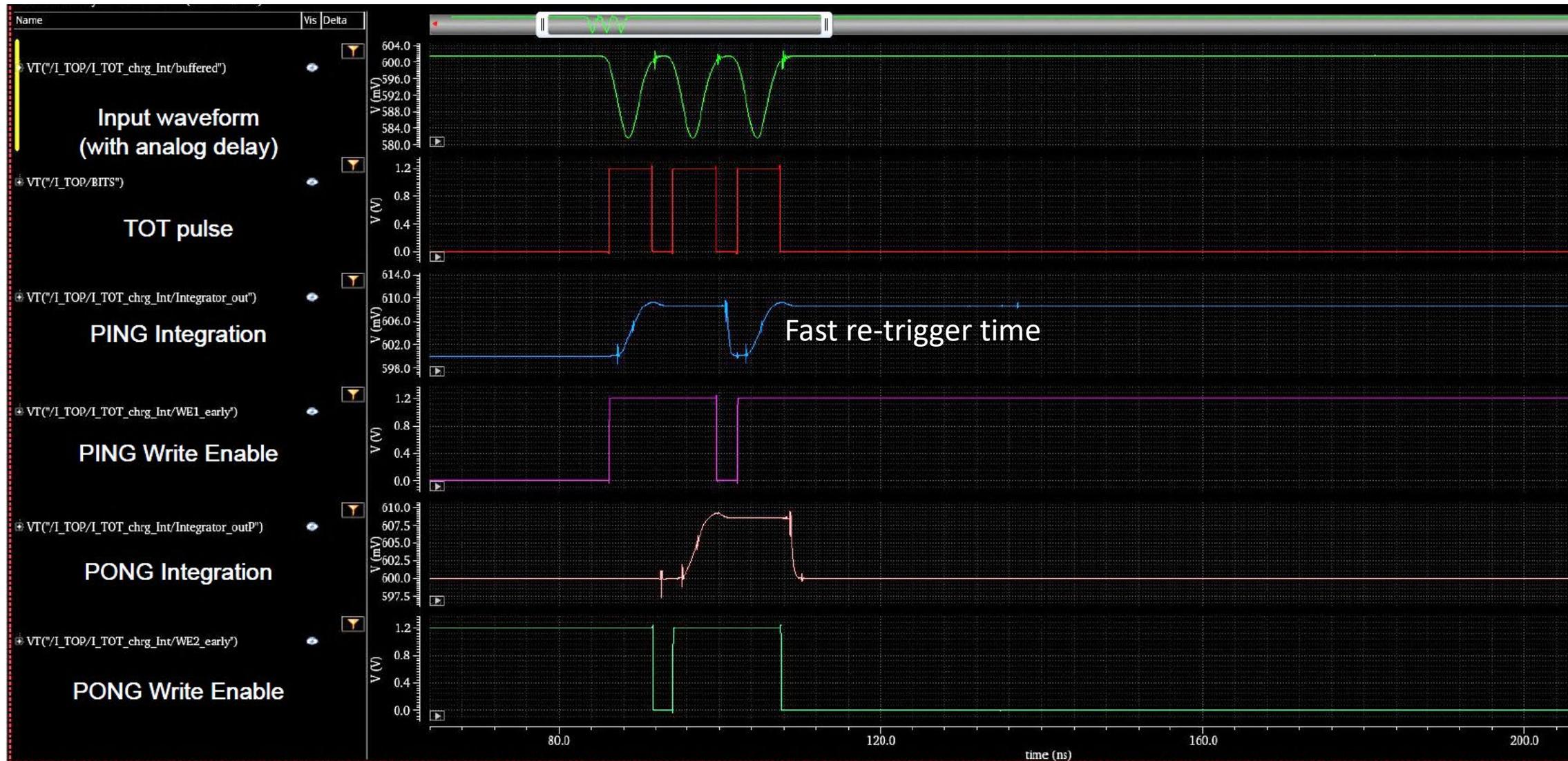**32-bit timestamps x2** – leading/trailing edges
b1 – double peak
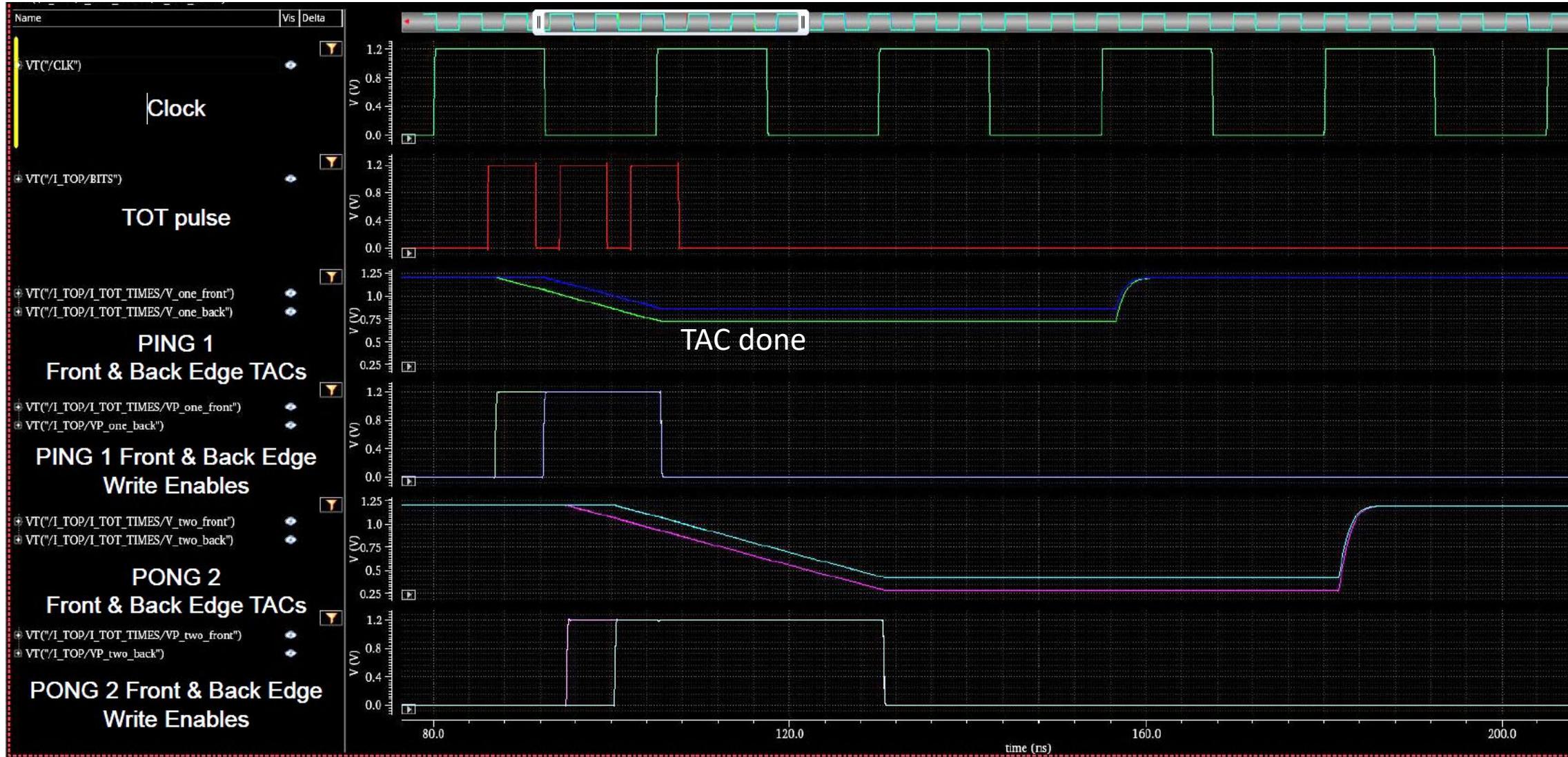**b010** – memory "column"

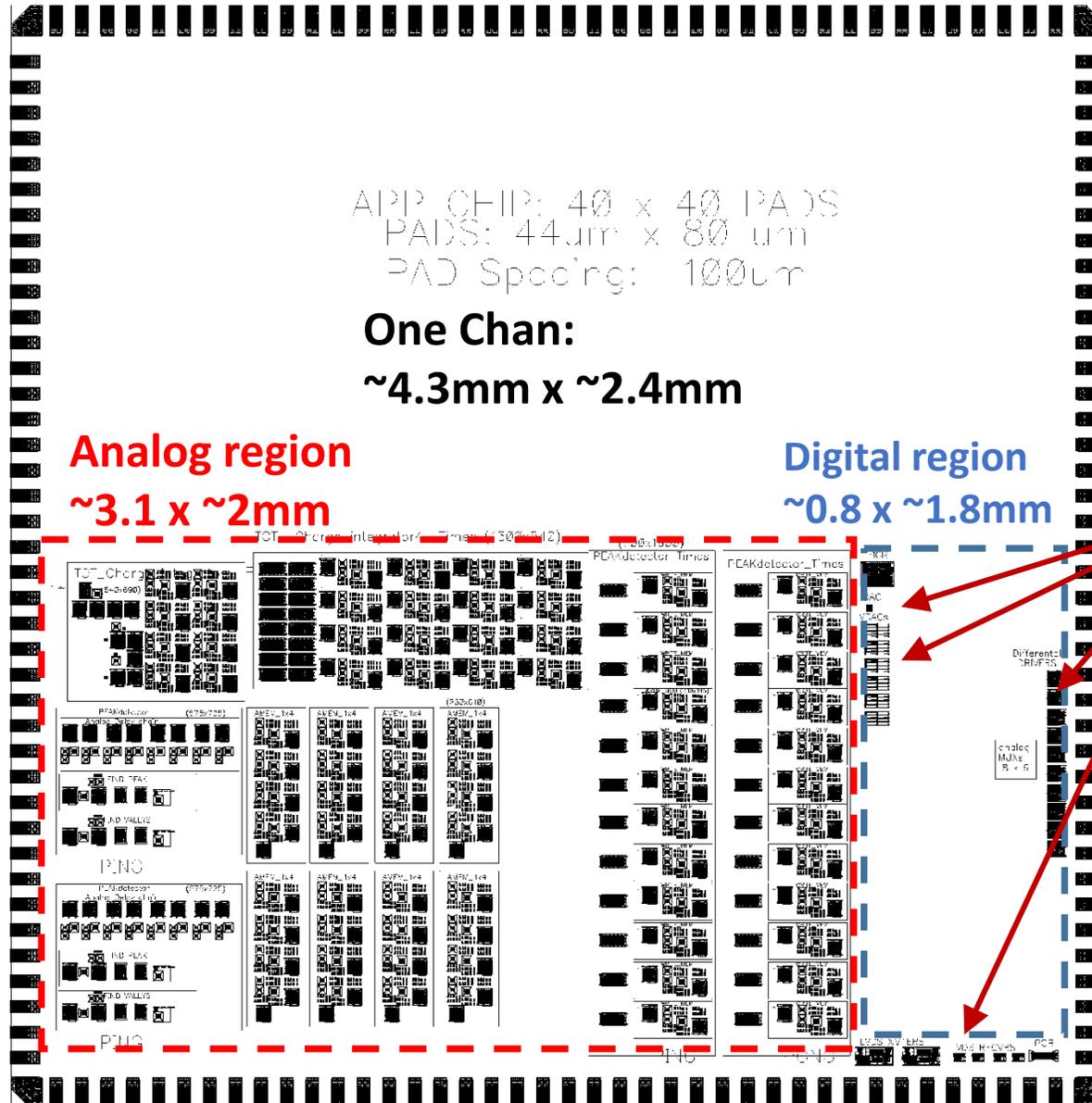# Example simulation – 8ns pulse separation

Example simulation – timing measurement

Preliminary area estimate

APP CHIP: 40 x 40 PADS
PADS: 44um x 80 um
PAD Spacing: 100um

One Chan:
~4.3mm x ~2.4mm

PMT inputs →

Analog region
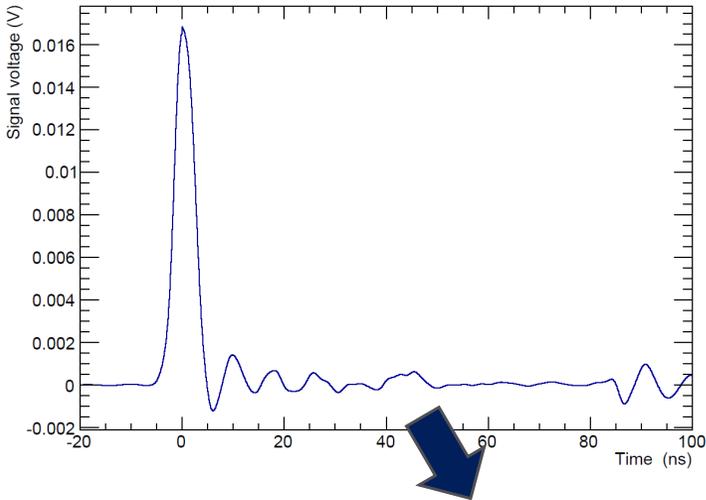**~3.1 x ~2mm**
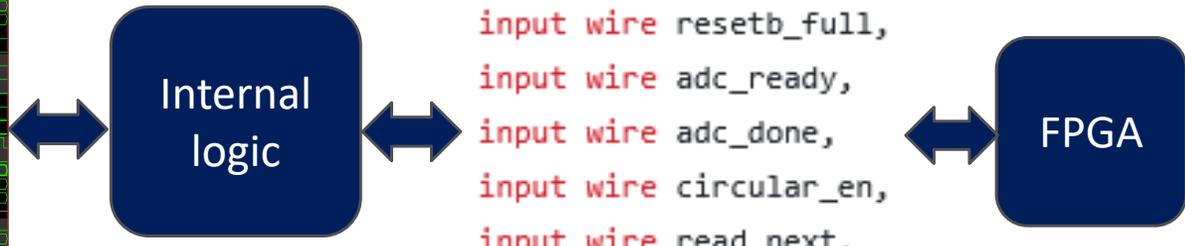
Digital region
~0.8 x ~1.8mm

Chip Services:
-Fully differential drivers (analog, LVDS)
-DACs (current and voltage)
-analog MUXs
-bandgap reference
-power on reset

`cocotb` simulation flow

Real data, converted to .csv and fed into simulator

- `cocotb` is a simulation framework that allows one to use Python to write testbenches
- Used successfully in the design and verification of ITK ASICs
- See talk by Paul Kenner and Ben Rosser: https://indico.global/event/14966/contributions/133732/

Behavioral model of analog blocks – fast simulation time
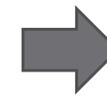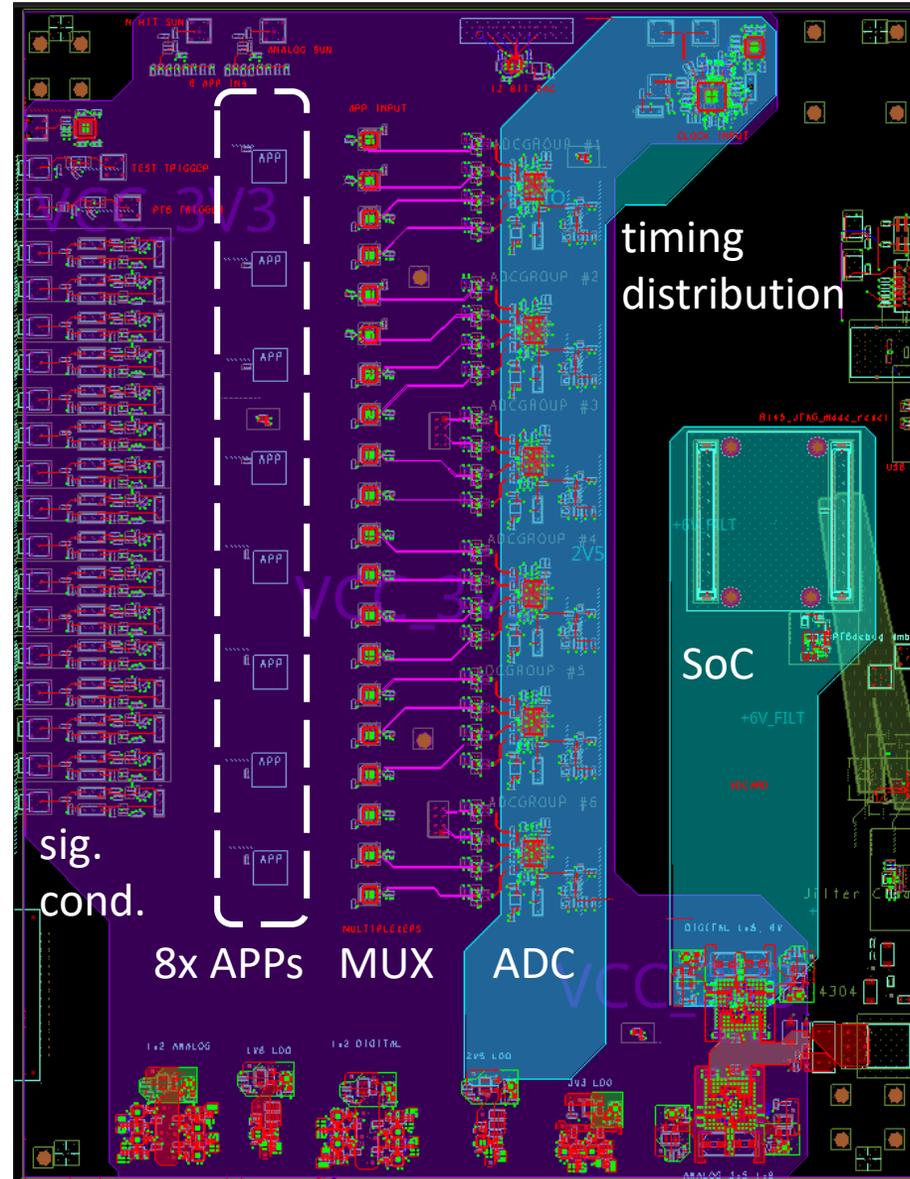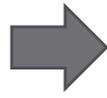
Internal logic ⟷ FPGA

```
// signals to/from outside world
input wire clk,
input wire resetb_full,
input wire adc_ready,
input wire adc_done,
input wire circular_en,
input wire read_next,
output wire amem_empty,
output wire amem_full
```
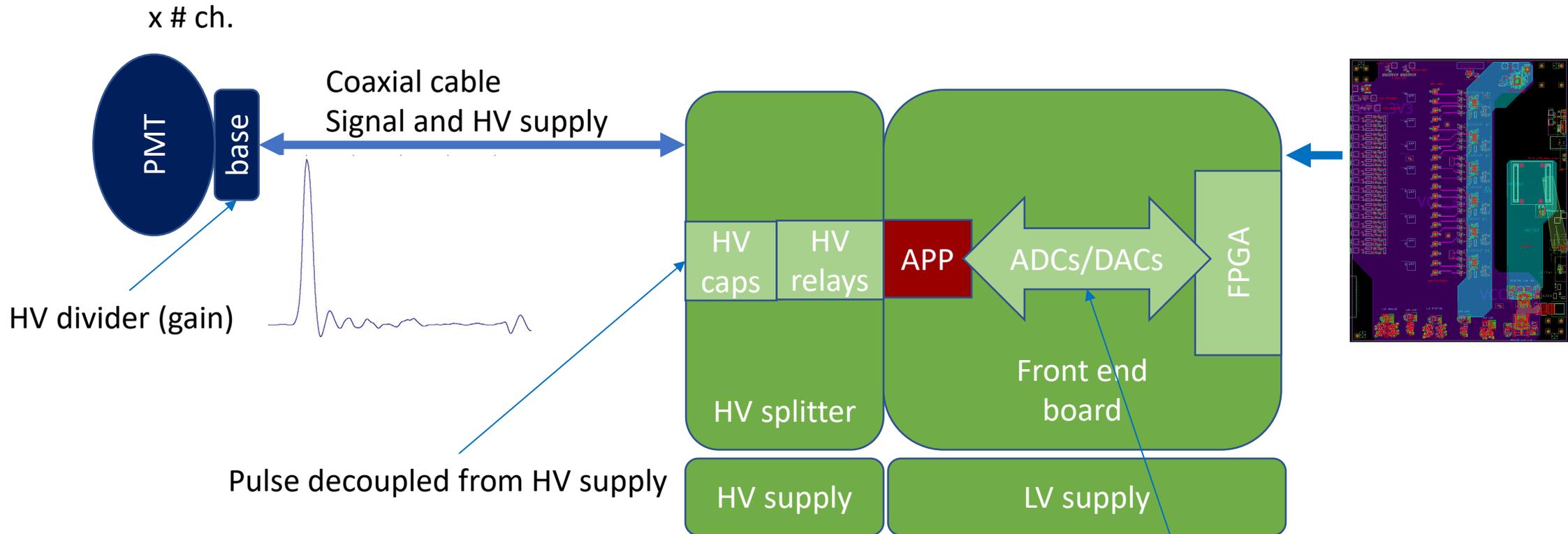
PCB for prototype testing

- We are designing a test structure/demonstrator for APP

- Commercial FPGA, Ethernet readout

- 14 bit commercial ADCs with convert trigger (not continuous sampling)
  - ENOB closer to ~12b, may only need 8—10b)
  - ~300 uV / count
  - sub 10ps TAC resolution
  - Probably limited by digitization time

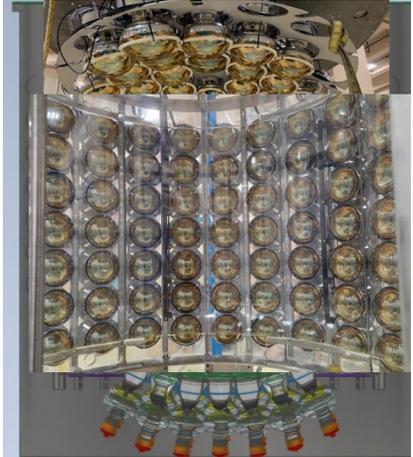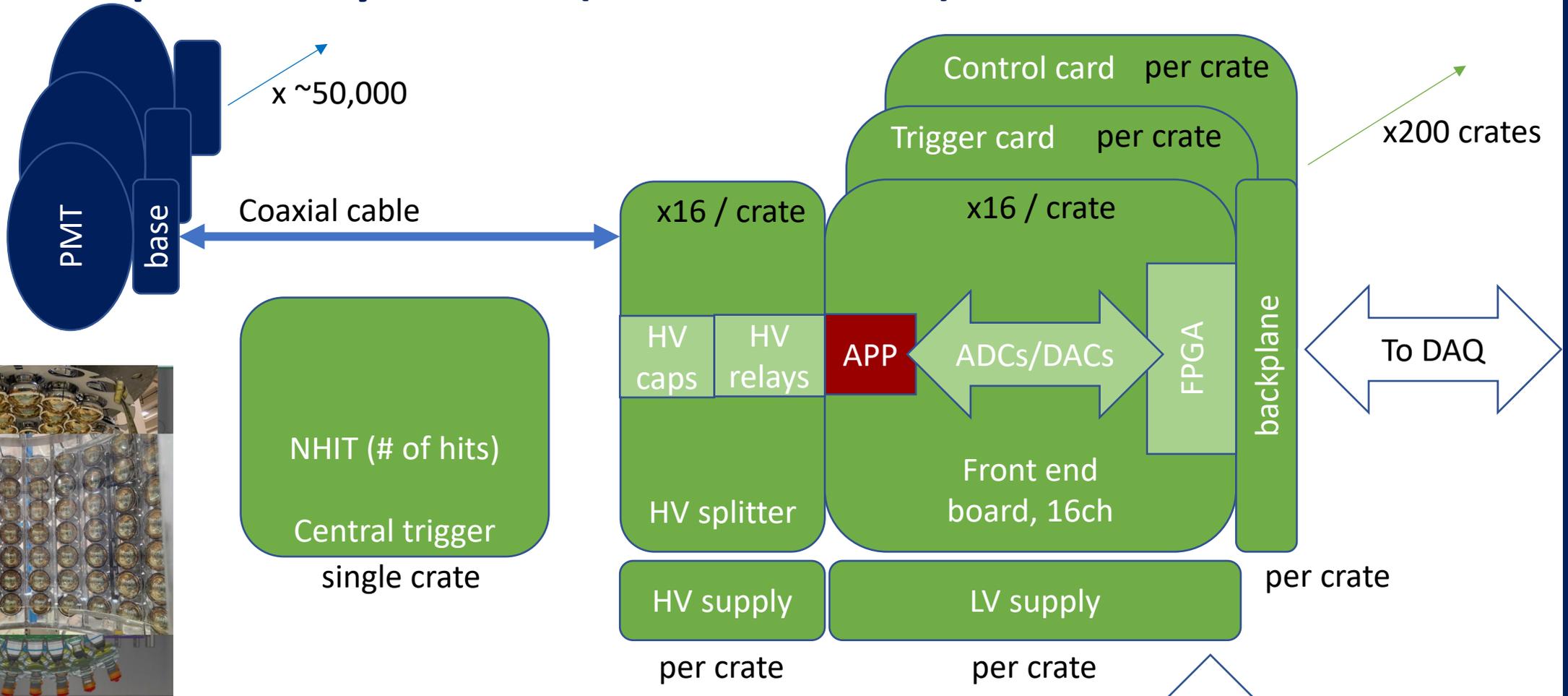- Support: calibration, analog sum, trigger, etc.

PMT inputs →

Ethernet readout →

Conceptual system (a few channels)

x # ch.

PMT

base

Coaxial cable
Signal and HV supply

HV divider (gain)

Pulse decoupled from HV supply

HV caps

HV relays

APP

ADCs/DACs

FPGA

HV splitter

Front end board

HV supply

LV supply

Commercial readout
Low cost commercial ADCs (several $ per channel)

Conceptual system (a detector)

x ~50,000

Coaxial cable

Control card   per crate

Trigger card   per crate

x16 / crate

x16 / crate

x200 crates

HV caps | HV relays | APP | ADCs/DACs | FPGA | backplane

To DAQ

NHIT (# of hits)

Central trigger

single crate

HV splitter

Front end board, 16ch

per crate

HV supply

LV supply

per crate

per crate

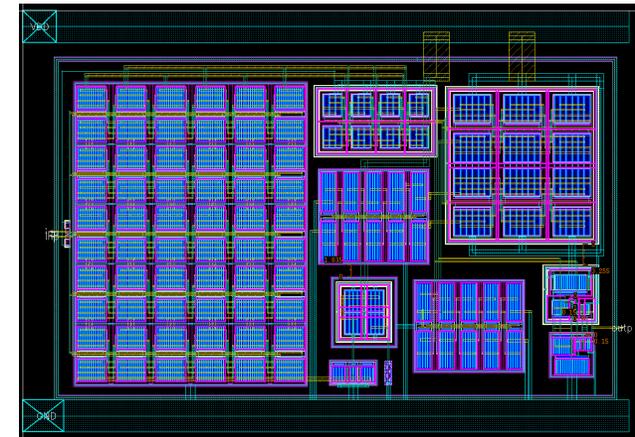per crate

power
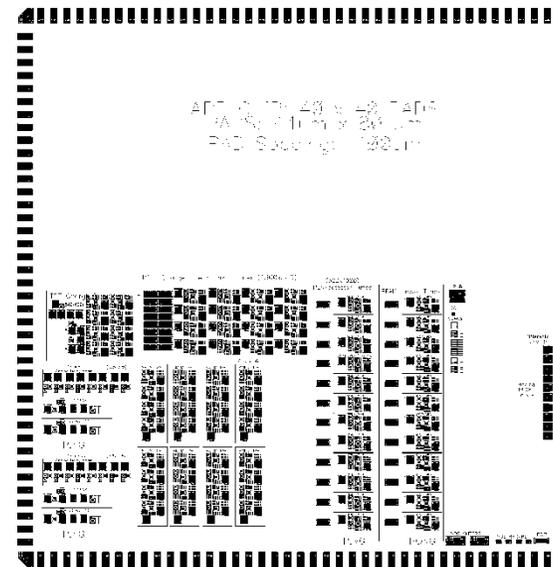
- Example: data rates for a large system O(50k PMT)
  - Untriggered WFD v. untriggered feature extraction: 7.5 EB v. 44 PB / year
  - Triggered WFD v. triggered feature extraction: 4 PB v. 160 TB / year
  - Best case: order(s) of magnitude reduction in data volume

18

Summary

- The Analog Photon Processor is an analog feature extraction chip for future detectors

- Many APP analog blocks are complete or nearly complete

- Digital logic being written/simulated

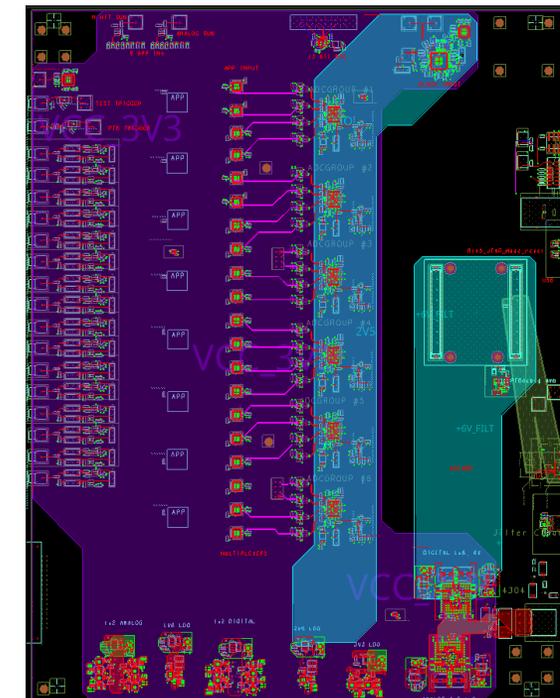- We are designing a test structure/demonstrator for APP

Example fast comparator layout

Chip floorplan

PCB layout

Thank you!

- Current APP team: Nandor Dressnandt[2], Carl Grace[8], Paul Keener[2], Josh Klein[1], Max Malakhovets[5], Godwin Mayers[2], Mitch Newcomer[2], Adrian Nikolica[2], Ravi Pitelka[3], Rick Van Berg[2], Jihao Yang[4]

- Past contributors: Yiming He[4], Bill Heintzelman[7], Ben Land[6], Chengjun Li[4], Xiaokai Ma[4], Meijun Tian[4], Hao Yan[4]

[1]Principal investigator

[2]Instrumentation group

Physics [6]postdocs, [3]PhD students, [7]visiting scholars
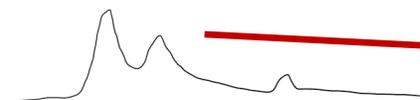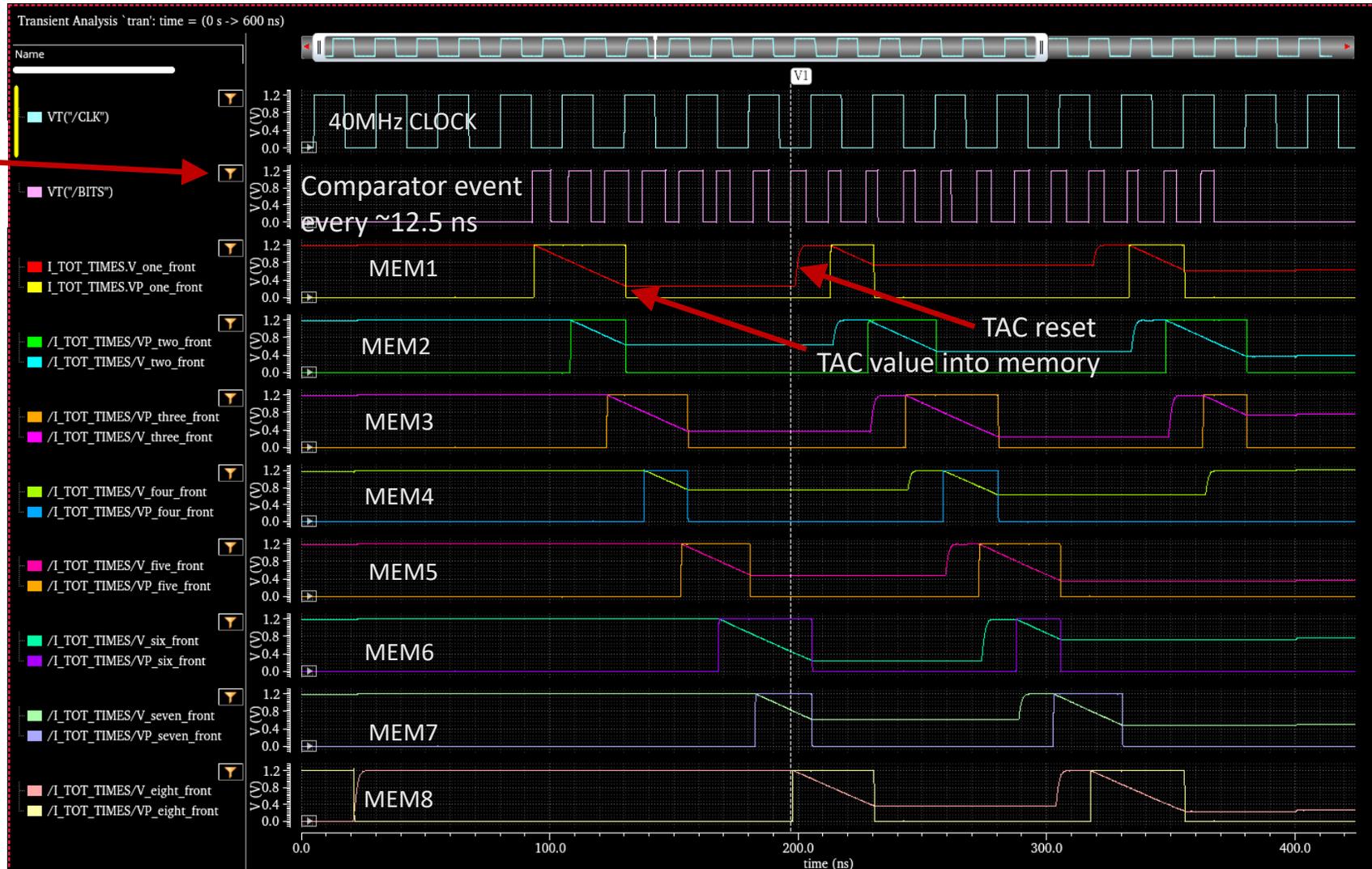
Electrical Engineering [4]Master's students, [5]undergraduate students

Collaborators[8]

Backup

Full channel analog simulation

8 memories filled in circular buffer mode

(Only leading edge time measurements shown)